MITSUBISHI ELECTRIC

< DIPIPM >

1200V LARGE DIPIPM Ver.6 Series APPLICATION NOTE

PSS**SA2FT

Table of contents

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CHAPTER 1 INTRODUCTION

1.1 Target Applications

Motor drives for industrial use, such as packaged air conditioners, general-purpose inverter, servo, except for automotive applications.

1.2 Product Line-up

Table 1-1 Line-up

Type Name	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage
PSS05SA2FT	5A/1200V	0.75kW / 440V_{AC}	V_{iso} = 2500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PSS10SA2FT	10A/1200V	1.5kW / 440V_{AC}	
PSS15SA2FT	15A/1200V	2.2kW / 440V_{AC}	
PSS25SA2FT	25A/1200V	3.7kW / 440V_{AC}	
PSS35SA2FT	35A/1200V	5.5kW / 440V_{AC}	
PSS50SA2FT	50A/1200V	7.5kW / 440V_{AC}	
PSS75SA2FT	75A/1200V	10kW / 440V_{AC}	

Note 1: These motor ratings are general ratings, so those may be changed by conditions.

1.3 Functions and Features

1200V Large DIPIPM Ver.6 is a compact intelligent power module with transfer molding package favorable for larger mass production. And it includes power chips, drive and protection circuits.

This series apply same package, which has high thermal radiation performance by the insulated sheet structure, and pin compatibility with current Large DIPIPM Ver.4 series. In addition, this series newly integrate low loss 6th generation IGBT optimized for DIPIPM and 1200V bootstrap diodes for generating P-side driver 15V supply.

This series has newly expanded lineup 75A/1200V model with 7th generation IGBT, in addition to the conventional 5~50A/1200V models .

Large DIPIPM Ver.6 will contribute to improve system efficiency, cost and also design time.

Outline photograph and internal cross-section structure are described in Fig.1-1 and Fig.1-2.

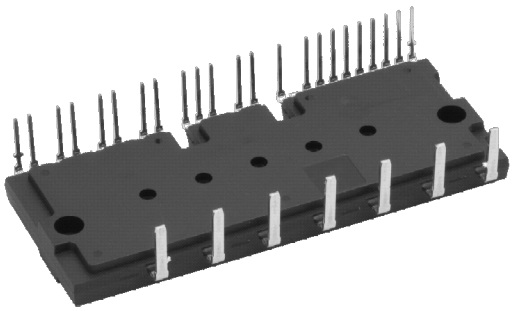


Fig.1-1 Package outline

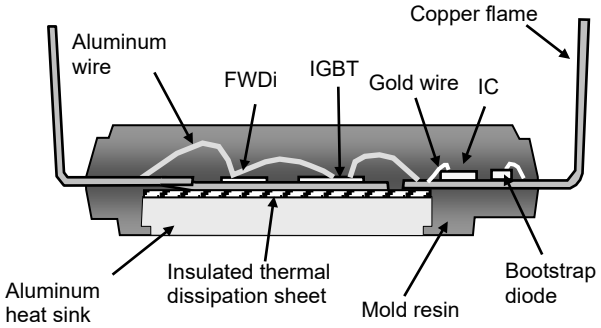


Fig.1-2 Internal cross-section structure

Features:

- For P-side IGBTs
  -Drive circuit
  -High voltage level shift circuit
  -Control supply under voltage (UV) protection circuit (without fault signal output)
  -Built-in bootstrap diode with current limiting resistor

- For N-side IGBTs
  -Drive circuit
  -Short circuit (SC) protection circuit (by detecting sense current divided at N-side IGBT with external sense resistor)
  -Control supply under voltage (UV) protection circuit (with fault signal output)
  -Analog output of LVIC temperature

- Fault Signal Output
  -Corresponding to SC protection and N-side UV protection

- IGBT Drive Supply
  -Single DC15V power supply

- Control Input Interface
  -High active logic

- UL recognized
  -UL1557 File E80276

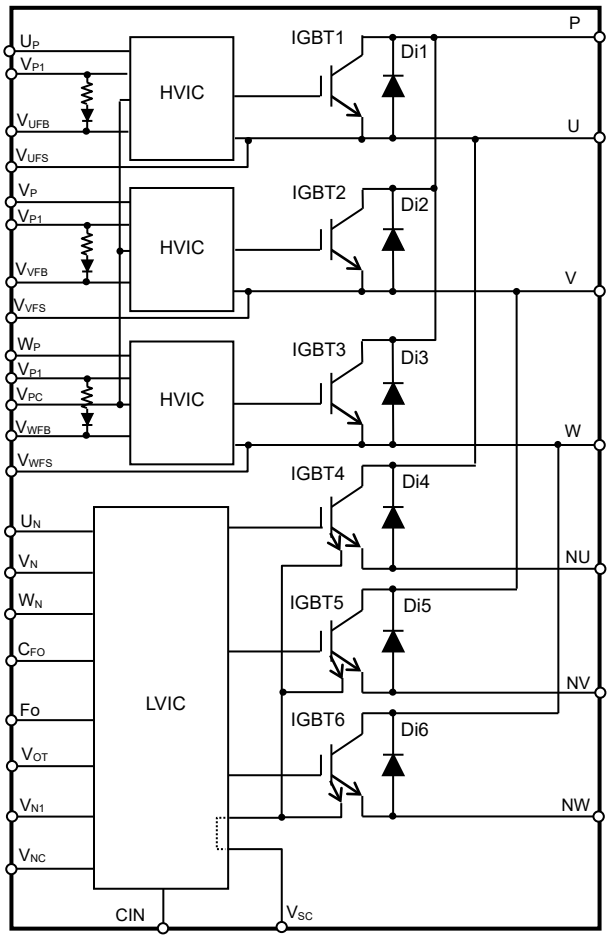


Fig.1-3 Internal circuit schematic

1.4 The Differences of Previous Series (1200V Large DIPIPM Ver.4) and This Series

There are some differences between this Ver.6 series and former Ver.4 series (PS22A7*) as below Table 1-2.

Table 1-2 Differences of specifications

Item	Ver.4		Ver.6		Ref.
	PS22A72~PS22A78-E	PS22A79	PSS05~50SA2FT	PSS75SA2FT	
	5A~35A	50A	5A~50A	75A	
Built-in IGBT	5th generation IGBT (LPT-CSTBT)	6th generation IGBT (LPT-CSTBT)	6th generation IGBT (LPT-CSTBT)	7th generation IGBT (LPT-CSTBT)	-
Bootstrap Di	Nothing	←	Built-in (with current limit R typ. 20Ω)		-
Temperature output (V_{OT} Output)	typ. 3.63V (at LVIC temp. = 85°C)	typ. 2.38V (at LVIC temp. = 75°C) with pull down resistor	← (Same with PS22A79)		Section 2.2.3
Fault output current I_{FO}	max. 1mA	←	max. 5mA (Direct coupler drive is available)		Section 3.1.4
Arm shoot through blocking time	Min. 3.0μs	Min. 3.3μs	Min. 3.0μs		
Tj	-20°C ~150°C	←	-30°C ~150°C		
Recommended Control supply voltage conditions	13.5≤V_D≤16.5V, 13.0≤V_{DB}≤18.5V (For SC trip level ≥ 1.7 times of rated current)	←	←	**14.0**≤V_D≤16.5V, 13.5≤V_{DB}≤18.5V (For SC trip level ≥ 1.7 times of rated current)	Section 2.2.1

There are other differences. (e.g. electric characteristics, sense resistance for SC protection, allowable minimum pulse width, electrical potential of dummy terminals and thermal resistance) Please refer each datasheet for more detail.

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Specifications

The specifications are described below by using PSS35SA2FT (35A/1200V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PSS35SA2FT are shown in Table 2-1.

Table 2-1 Maximum Ratings of PSS35SA2FT

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	900	V	(1)
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	1000	V	(2)
V_{CES}	Collector-emitter voltage		1200	V	(3)
$\pm I_C$	Each IGBT collector current	T_C= 25°C (Note 1)	35	A	(4)
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, up to 1ms	70	A	
P_C	Collector dissipation	T_C= 25°C, per 1 chip	117.6	W	
T_j	Junction temperature		-30~+150	°C	(5)

Note 1: Pulse width and period are limited due to junction temperature.

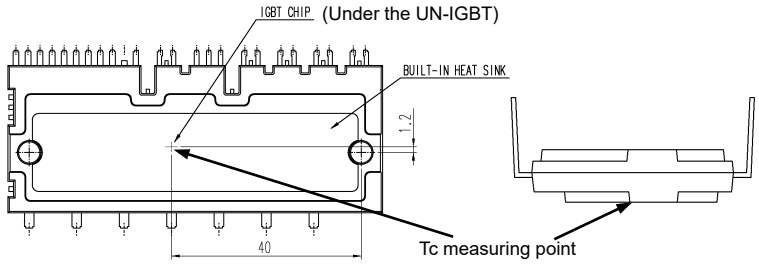
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	5	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 125°C, non-repetitive, up to 2μs	800	V	(6)
T_C	Module case operation temperature	(Note 2)	-30~+100	°C	
T_{stg}	Storage temperature		-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}	

Note 2: Tc measurement point



(7)

[Item explanation]

(1) Vcc — The maximum P-N voltage in no switching state. Voltage suppressing circuit such as a brake circuit is necessary if the voltage exceeds this value.

(2) Vcc(surge) — The maximum P-N surge voltage in switching state. snubber circuit is necessary if the voltage exceeds Vcc(surge).

(3) V_{CES} — The maximum sustained collector-emitter voltage of built-in IGBT.

(4) $\pm I_C$ — The allowable current flowing into collect electrode (@Tc=25°C).Pulse width and period are limited due to junction temperature Tj.

(5) Tj — The maximum junction temperature rating is 150°C.But for safe operation, it is recommended to limit the average junction temperature up to 125°C. Repetitive temperature variation ΔTj affects the life time of power cycle, so refer life time curves (Section 3.1.10) for safety design.

(6) Vcc(prot) — The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.

(7) Tc position — Tc (case temperature) is defined as the temperature just underneath the specified power chip. Please mount a thermocouple on the heat sink surface at above position to get proper temperature. Due to the control schemes (e.g. Different control between P and N-side like two phase modulation, high-side chopping), the highest Tc point may be different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip. (Refer Section 2.3.2)

2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance.

Table 2-2 Thermal resistance of PSS35SA2FT

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 1)	Inverter IGBT part (per 1/6 module)	-	-	0.85	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	1.25	K/W

Note 1: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.2K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10s. The thermal resistance under 10s is called as transient thermal impedance which is shown in Fig.2-1. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max) For example, the IGBT transient thermal impedance of PSS35SA2FT in 0.1s is 0.85×0.53=0.45K/W.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (E.g. In the cases at motor starting, at motor lock…)

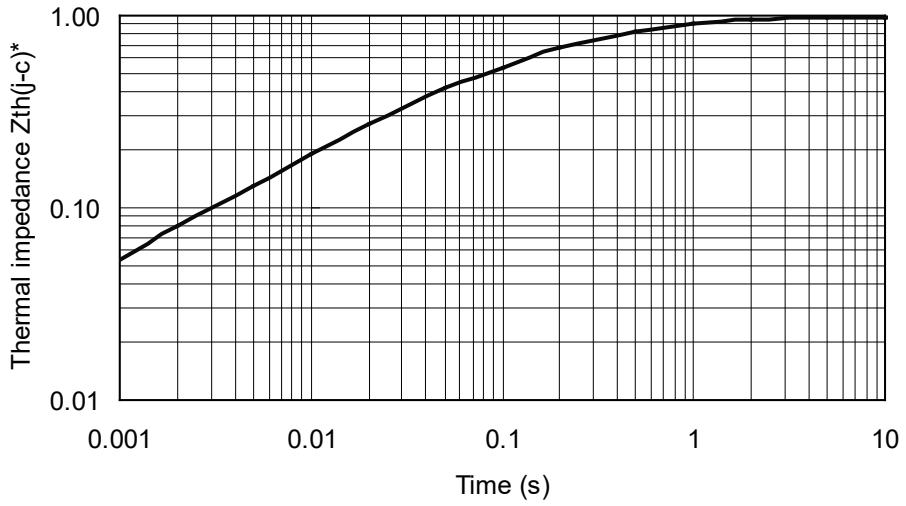


Fig.2-1 Typical transient thermal impedance

2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics.

Table 2-3 Static characteristics and switching characteristics of PSS35SA2FT

Inverter Part

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB} = 15V, V_{IN}= 5V, I_C= 35A	T_j= 25°C	-	1.50	2.20	V
			T_j= 125°C	-	1.70	2.40	
V_{EC}	FWDi forward voltage	V_{IN}= 0V, -I_C= 35A		-	2.20	2.80	V
t_{on}	Switching times	V_{CC}= 600V, V_D= V_{DB}= 15V I_C= 35A, T_j= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		1.20	1.90	2.60	μs
$t_{C(on)}$				-	0.50	0.80	μs
t_{off}				-	2.40	3.60	μs
$t_{C(off)}$				-	0.50	0.90	μs
t_{rr}				-	0.50	-	μs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}	T_j= 25°C	-	-	1	mA
			T_j= 125°C	-	-	10	

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

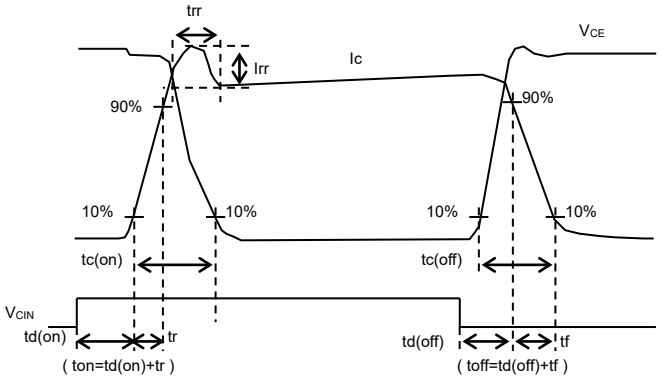
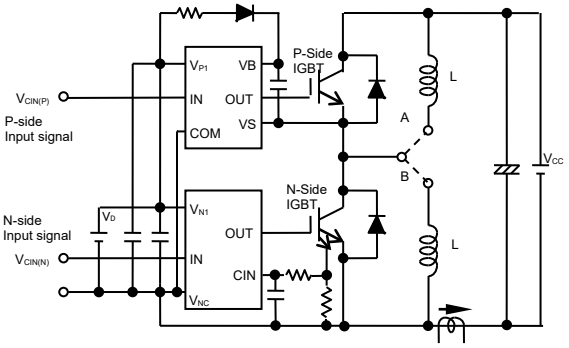
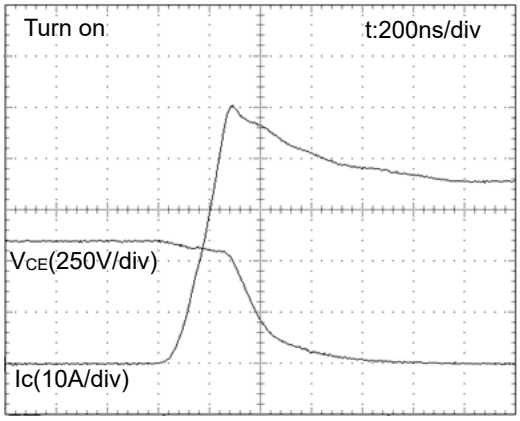


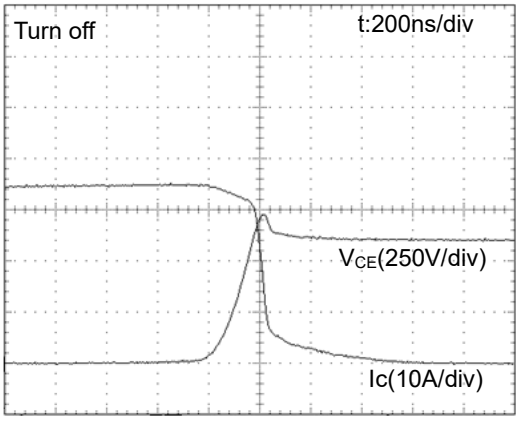
Fig.2-2 Switching time definition



Short A for N-side IGBT, and short B for P-side IGBT evaluation

Fig.2-3 Evaluation circuit (inductive load)





Conditions: V_{CC}=600V, V_D=V_{DB}=15V, Tj=125°C, Ic=35A, Inductive load half-bridge circuit

Fig.2-4 Typical switching waveform

2.1.4 Electric Characteristics (Control Part)

Table 2-4 Control (Protection) characteristics of PSS35SA2FT

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{PC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	5.60	mA
			V_D=15V, V_{IN}=5V	-	-	5.60	
I_{DB}		Each part of V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	1.10	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	1.10	
I_{SC}	Short circuit trip level	-30°C≤Tj≤125°C, Rs= 48.7Ω (±1%), Without outer shunt resistors to NU,NV,NW terminals (Note 1)		59.5	-	-	A
UV_{DBt}	P-side Control supply under-voltage protection(UV)	T_j ≤125°C	Trip level	10.0	-	12.0	V
UV_{DBr}			Reset level	10.5	-	12.5	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)	T_j ≤125°C	Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	C_{FO}=22nF (Note 2)		1.6	2.4	-	ms
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	-	3.5	V
$V_{th(off)}$	OFF threshold voltage			0.8	-	-	
V_{OT}	Temperature output	LVIC temperature=75°C,Pull down R=5.1kΩ (Note 3)		2.26	2.38	2.51	V
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor		0.5	0.9	1.3	V
R	Built-in limiting resistance	Included in bootstrap Di		16	20	24	Ω

Note 1: Short circuit protection detects sense current divided from main current at N-side IGBT and works for N-side IGBT only. In the case that outer shunt resistor is inserted into main current path, protection current level I_{SC} changes. For details, please refer the section about SC protection in this document.

2: Fault signal is output when short circuit or N-side control supply under-voltage protection works. The fault output pulse-width t_{FO} depends on the capacitance of C_{FO}. (C_{FO} (typ.) = t_{FO} x (9.1 x 10^{-6}) [F])

3: DIPIPM doesn't shut down IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM immediately.

) Some specifications differs according to its rated current. For more details, please refer to the datasheet for each product.

2.1.5 Recommended Operating Conditions

The recommended operating conditions are described in Table 2-5. Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

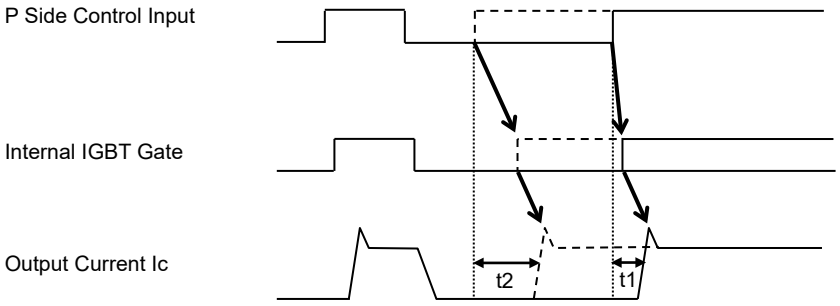
Table 2-5 Recommended operating conditions of PSS35SA2FT

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW		350	600	800	V
V_D	Control supply voltage	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal		3.0	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 100°C$, $T_j \leq 125°C$		-	-	20	kHz
I_O	Allowable r.m.s. current	V_{CC} = 600V, V_D = 15V, P.F = 0.8, Sinusoidal PWM, $T_C \leq 100°C$, $T_j \leq 125°C$ (Note 4)	f_{PWM}= 5kHz	-	-	19.1	Arms
			f_{PWM}= 15kHz	-	-	12.8	
PWIN(on)	Minimum input pulse width	(Note 5)		1.5	-	-	μs
PWIN(off)		350≤ V_{CC} ≤ 800V, 13.5≤ V_D ≤ 16.5V, 13.0≤ V_{DB} ≤ 18.5V, -20°C ≤ T_C ≤ 100°C, N line wiring inductance less than 10nH (Note 6)	$I_C \leq 35A$	3.0	-	-	
			35A<$I_C \leq$59.5A	3.5	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)		-5.0	-	+5.0	V
T_j	Junction temperature			-20	-	+125	°C

Note 4: The allowable r.m.s. current value depends on the actual application conditions.
5: DIPIPM might not make response to the input on signal with pulse width less than PWIN (on).
6: DIPIPM might make no response or delayed response (P-side IGBT only) for the input signal with off pulse width less than PWIN(off). Refer below about delayed response.

Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



Real line: off pulse width>PWIN(off); turn on time t1
Broken line: off pulse width<PWIN(off); turn on time t2
(t1:Normal switching time)

) Some specifications differs according to its rated current. For more details, please refer to the datasheet for each product.
For PSS75SA2FT, please also refer the following Short Circuit Protection section (Section 2.2.1) about its short circuit trip level and its recommended operation condition of control supply voltage.

2.1.6 Mechanical Characteristics and Ratings

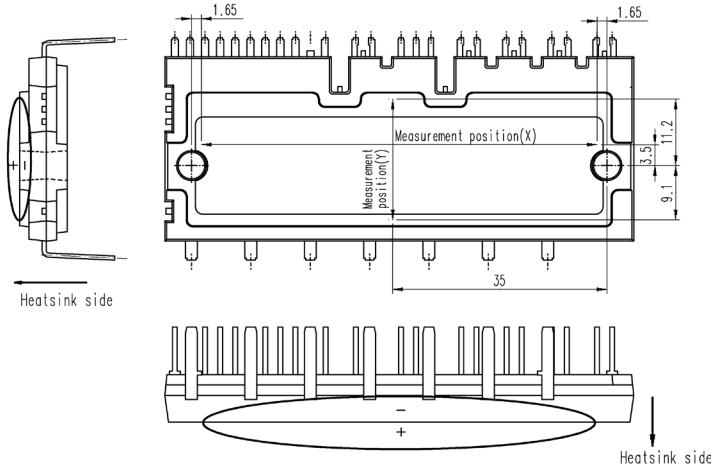
The mechanical characteristics and ratings are shown in Table 2-6
Please refer to Section 2.4 for the detailed mounting instruction.

Table 2-6 Mechanical characteristics and ratings of PSS35SA2FT

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended 1.18N·m	0.98	1.18	1.47	N·m
Terminal pulling strength	Load 19.6N	JEITA-ED-4701	10	-	-	s
Terminal bending strength	Load 9.8N, 90deg. bend	JEITA-ED-4701	2	-	-	times
Weight			-	46	-	g
Heat radiation part flatness			-50	-	100	μm

Measurement point of heat-sink flatness

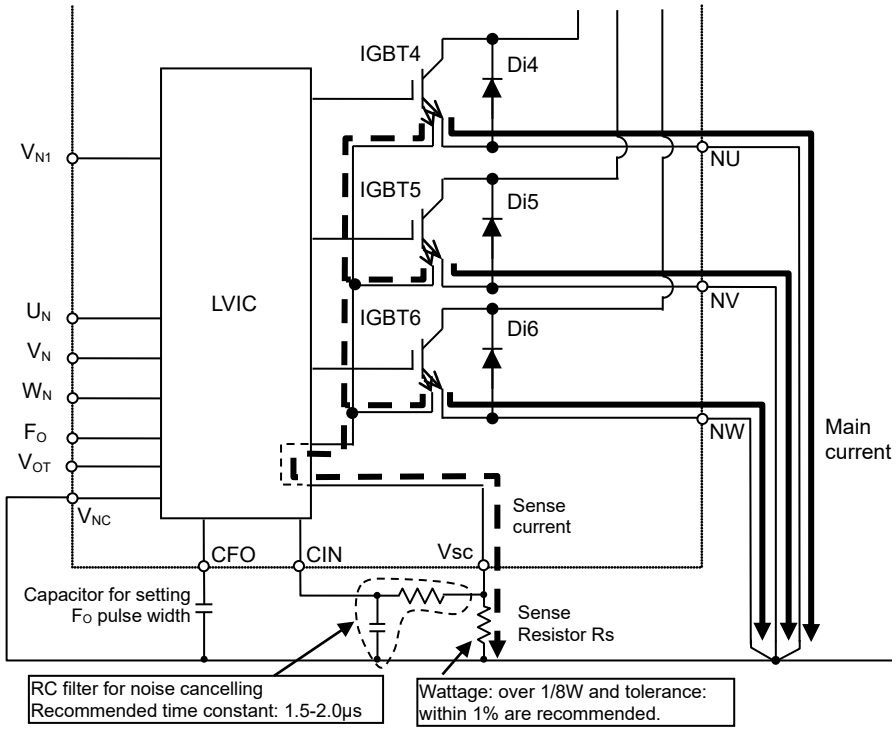


2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and outputting LVIC temperature function in this series.
The detailed information is described below.

2.2.1 Short Circuit Protection

This series apply the detection method of small sense current, which is divided at N-side IGBT, to SC protection. So high wattage type shunt resistor isn't necessary for SC protection. (Fig.2-5)



*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

Fig.2-5 SC protection circuit

SC protection works by inputting the potential, which is generated by sense current flowing into the sense resistor, to the CIN terminal. Tabel 2-7 describes specified sense resistance and minimum SC protection current in that case for each products. For PSS75SA2FT, it is necessary to use under the condition of control supply voltage range $14V \leq V_D \leq 16.5V$ and $13.5V \leq V_{DB} \leq 18.5V$ for assuring minimum trip current level 127A (1.7 times of rated current).

When SC ptotection works, DIPIPM shuts down all N-side IGBTs hardly and outputs Fo signal. Its pulse width(t_{Fo}) is set by C_{FO} capacitor ($C_{FO} = t_{FO} \times 9.1 \times 10^{-6}$ [F]).

To prvent malfunction, it is recommended to insert RC filter before inputting to CIN terminal and set the time constant to shut down withiin 2μs when short circuit occurs. (Time constant 1.5μ-2.0μs is recommended.) Also it is necessary to set the resistance of RC filter to ten or more times of the sense resistor Rs.(Hundred times is recommended.)

Table 2-7 SC protection trip level (Condition: Tj=-30°C~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals.)

Type name	Rs	Min.	Recommended operaton condition
PSS75SA2FT	21.0Ω	127A	$14.0 \leq V_D \leq 16.5V$, $13.5 \leq V_{DB} \leq 18.5V$
	24.3Ω	110A	$13.5 \leq V_D \leq 16.5V$, $13.0 \leq V_{DB} \leq 18.5V$
PSS50SA2FT	34Ω	85.0A	
PSS35SA2FT	48.7Ω	59.5A	
PSS25SA2FT	75Ω	42.5A	
PSS15SA2FT	100Ω	25.5A	
PSS10SA2FT	130Ω	17.0A	
PSS05SA2FT	261Ω	8.5A	

For sense resistor, its large fluctuation leads to large fluctuation of SC trip level. So it is necessary to select small variation and good temperature characteristic type (within +/-1% is recommended).

Wattage of the sense resistor can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 4000:1. (In this case maximum sense current flows.)

The estimation example for PSS35SA2FT is described as below.

[Estimation example]

(1) Normal operation state

It is assumed that the maximum main current for normal operation is 35A (rated current, for keeping a margin) and the sense resistance is 48.7Ω.

In this case, The maximum sense current flows through the sense resistor is calculated as below.

35A / 4000 = 8.8mA

And the loss at the sense resistor is

$P=I^2 \cdot R \cdot t=(8.8mA)^2 \times 48.7\Omega = \underline{3.8mW}$

(2) Short circuit state

When short circuit occures, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current =350A) flows. So the sense current is

350A / 4000 = 87.5mA

But this current shut down within 2μs by SC protection. And the average loss at the sense resistor is

$P=I^2 \cdot R \cdot t= (87.5mA)^2 \times 48.7\Omega \times 2\mu s / 1s = \underline{0.0007mW}$

And drop voltage of this sense resistor is

V= 87.5mA x 48.7Ω= 4.3V

As explained above, over 0.03W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

[Remarks]

It takes more time (Table 2-8) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC's transfer delay)

Table 2-8 Internal time delay of IC

Item	typ	max	Unit
IC transfer delay time	0.5	1.0	μs

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and this IC delay.

[SC protection (N-side only)]

a1. Normal operation: IGBT ON and outputs current.
a2. Short circuit current detection (SC trigger) (It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
a3. All N-side IGBTs' gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. Fo outputs with a fixed pulse width determined by the external capacitance C_{FO}.
a6. Input "L": IGBT off.
a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: IGBT ON and outputs current.

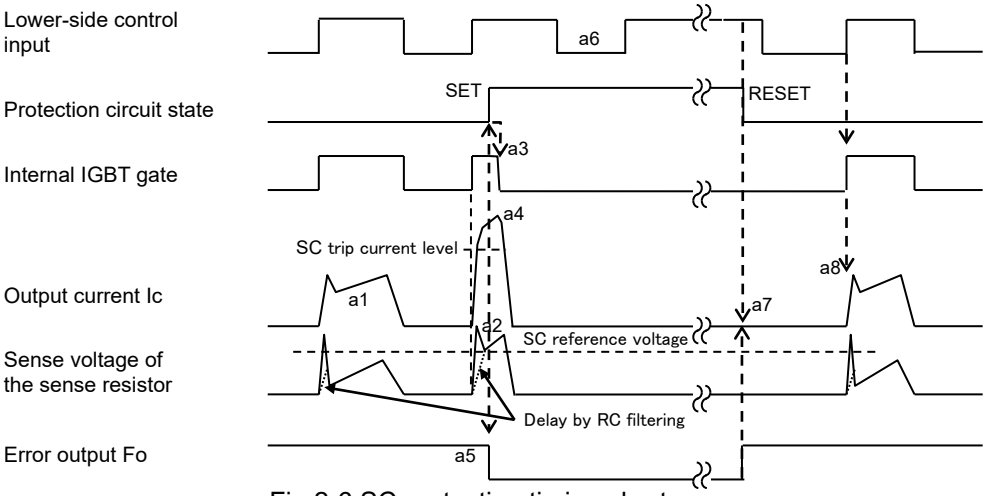


Fig.2-6 SC protection timing chart

[About Short Circuit Protection by Sense IGBT]

This function aims to protect from Short Circuit like arm short or load short. If high accuracy of protection current level (e.g. protection for demagnetizing motor) is necessary, it is recommended to apply the method by detecting the voltage at outer shunt resistors into main current path. In that case, the current split ratio between main and sense currents varies, thus minimum SC protection trip level changes from the value in Table 2-7. Therefore, adjustment of the sense resistance will be needed. The example of minimum SC trip level with outer shunt resistor is described in Table 2-9. (PSS35SA2FT, at sense resistance 48.7Ω) Please contact us about selecting sense resistance in the case of inserting outer shunt resistors.

Table 2-9 SC protection trip level (PSS35SA2FT, sense resistance 48.7Ω)

Outer shunt resistance	Minimum SC trip level
Nothing	59.5A
2mΩ	49.8A

It is recommended to set outer shunt resistance to the value as shown in Table 2-10 or less because too large shunt resistance causes decrease of IGBT saturation current by decreasing gate voltage at large current. (Large current makes large voltage drop at shunt resistor.) For shunt resistor, select low parasitic inductance resistor like surface mounted device type and pattern the wiring from the N-side emitter (NU, NV, NW) terminals as short as possible because of reducing surge by shutdown at large short circuit current.

Table 2-10 Recommended maximum outer shunt resistance

Type name	Rs
PSS75SA2FT	5mΩ
PSS50SA2FT	7mΩ
PSS35SA2FT	10mΩ
PSS25SA2FT	14mΩ
PSS15SA2FT	23mΩ
PSS10SA2FT	34mΩ
PSS05SA2FT	67mΩ

As a method that combines short circuit and over current protection function, there is a method which doesn't use sense resistor too. It is the same method as former DIPIPM Ver.3 and the example of protection circuit is described in Fig.2-7.

The SC protection trip level is needed to set to double the rated current or less. And it is recommended to set the reference voltage of comparators to about 0.5V and select the shunt resistance in order that the SC trip level becomes double the rated current or less. (e.g. In the case that the protection level is set to double the rated current for PSS35SA2FT, R=0.5V/70A=7.2mΩ or more)

When this protection method is applied, the rated sense resistor Rs should be connected between Vsc terminal and GND for protecting from surge too. (Don't leave it open.)

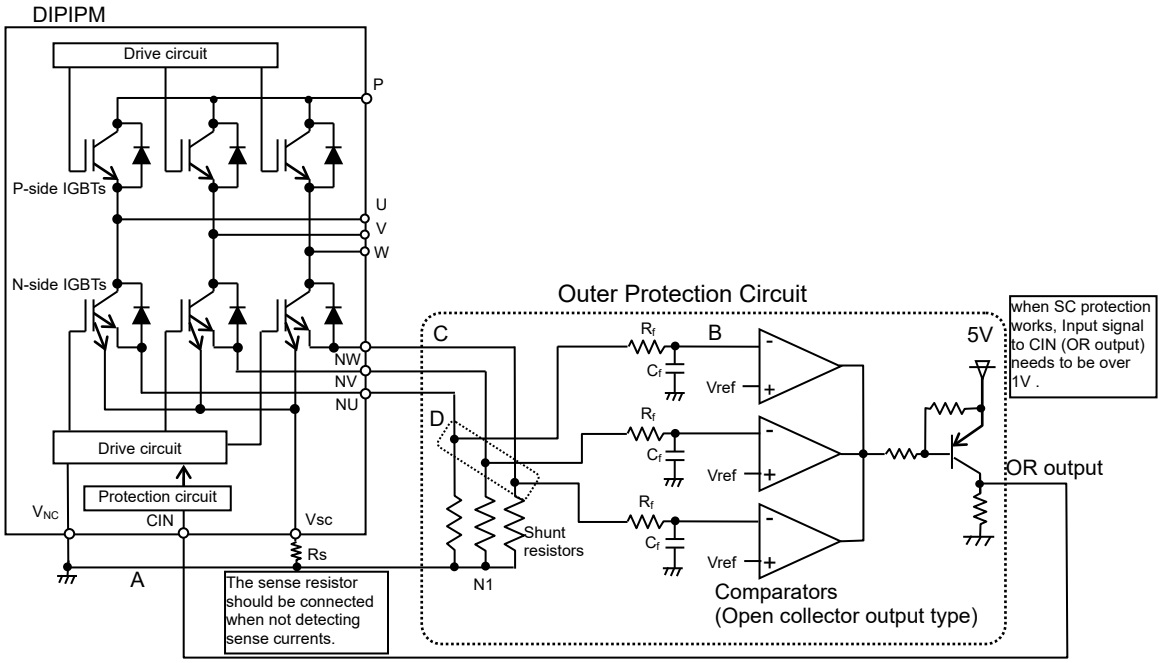


Fig.2-7 Example of SC protection circuit without detecting sense current.

Note:

- It is necessary to set the time constant R_fC_f of external comparator input so that IGBT can stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on. If additional RC filter is inserted into OR output, it is necessary to consider its delay too.
- The threshold voltage Vref is recommended to set about 0.5V.
- Select the shunt resistance so that SC trip-level is less than double the rated current.
- To avoid malfunction, the wiring A, B, C should be as short as possible.
- The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- OR output high level should be over 1V at all temperature range.

2.2.2 Control Supply UV Protection

The UV protection is designed for preventing unexpected operating behavior as described in Table 2-11.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-11 DIPIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on. (Avoid inputting ON-signals to DIPIPM before the control supply coming up to 13.5V)
4.0-UV trip level (P, N)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV trip level-13.5V(N),13.0V(P)	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N), 13.0-18.5V (P)	Recommended conditions. (Normal operation)
16.5-20.0V (N),18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	Over maximum voltage rating. The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency precipitous noise is superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

Recommended condition for PSS75SA2FT

It is necessary to use on the condition of control supply voltage range $14V \leq V_D \leq 16.5V$ and $13.5V \leq V_{DB} \leq 18.5V$ for assuring minimum trip current level 127A (1.7 times of rated current). For more details, please refer Short Circuit Protection section (Section 2.2.1) or its datasheet for its product.

N-side UV Protection Sequence

a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON when inputting next ON signal (L→H).(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a2. Normal operation: IGBT turn on and carry current.
a3. V_D level drops to under voltage trip level. (UV_{Dt}).
a4. All N-side IGBTs turn OFF in spite of control input condition.
a5. Fo outputs for the period determined by the capacitance $C_{FO,}$ but output is extended during V_D keeps below UV_{Dr}.
a6. V_D level reaches UV_{Dr}.
a7. Normal operation: IGBT ON and carry current.

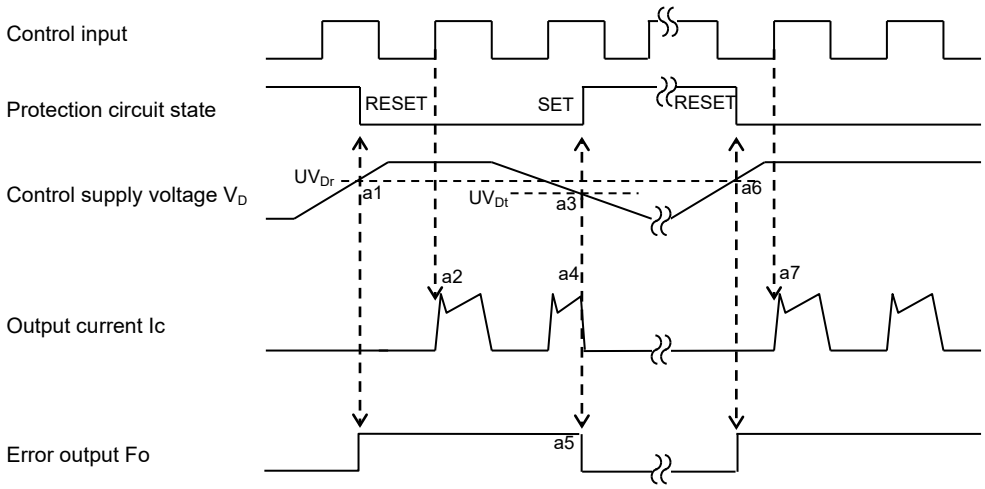


Fig.2-8 Timing chart of N-side UV protection

P-side UV Protection Sequence

b1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, IGBT can turn on when inputting next ON signal (L→H).
b2. Normal operation: IGBT ON and outputs current.
b3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
b4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
b5. V_{DB} level reaches UV_{DBr}.
b6. Normal operation: IGBT ON and carry current.

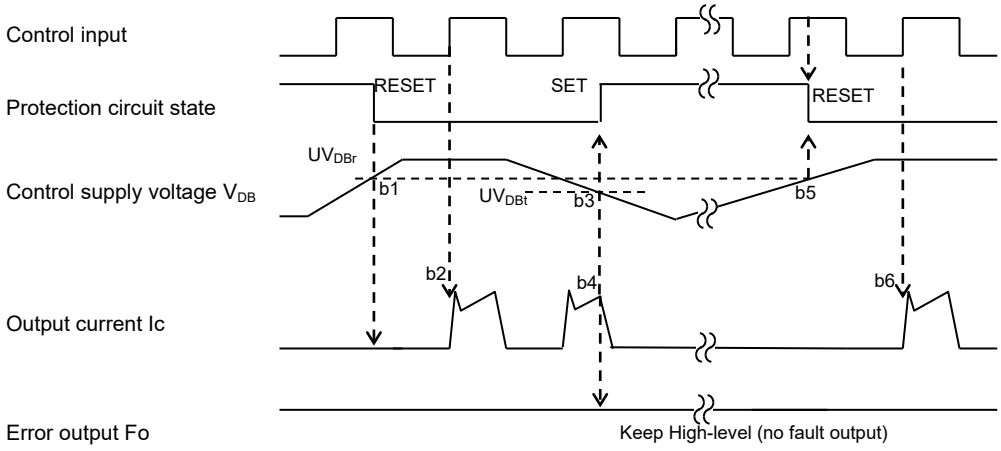


Fig.2-9 Timing Chart of P-side UV protection

2.2.3 Temperature Output Function

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through mold package and inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of power chips effectively. (e.g. motor lock, short current) It is recommended to use this function for protecting from excessive temperature rise by such cooling system down and continuance of overload operation.（Replacement from the thermistor which has been set on outer heat sink currently）

Also DIPIPM cannot shutdown IGBT and output fault signal automatically when temperature rises excessively. When temperature exceeds the defined protect level, controller (MCU) should stop the DIPIPM.

(1) V_{OT} terminal circuit and outer additional circuit

V_{OT} output circuit, which is described in Fig.2-10, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-12. Refer Fig.2-19 about output characteristics.

Table 2-12 Output capability
(Tc=-20°C ~100°C)

	min.
Source	1.7mA
Sink	0.1mA

Source : Current flow from V_{OT} to outside.
Sink : Current flow from outside to V_{OT}.

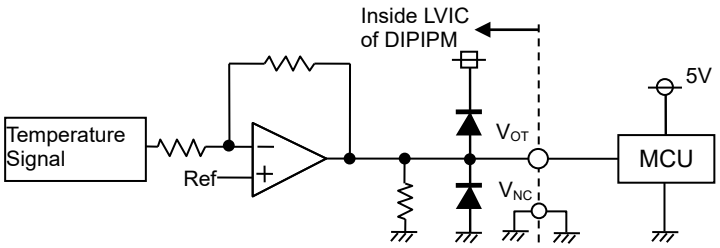


Fig.2-10 Inner circuit of V_{OT} terminal

- In the case of detecting lower temperature than room temperature

It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

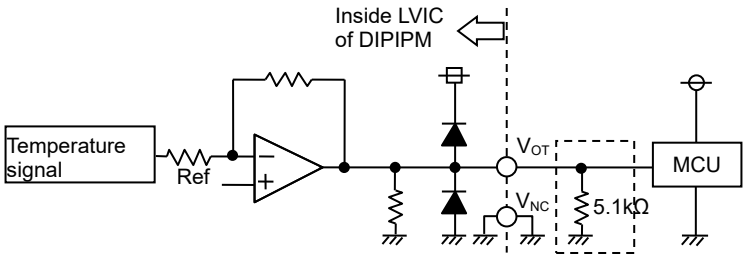


Fig.2-11 V_{OT} output circuit in the case of detecting low temperature

- In the case of using with low voltage controller(MCU)

  In the case that V_{OT} output will be input to a low voltage controller (e.g. 3.3V MCU), V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage. (Pay attention that the allowable PWM input logic of this DIPIPM series is 5V logic.)

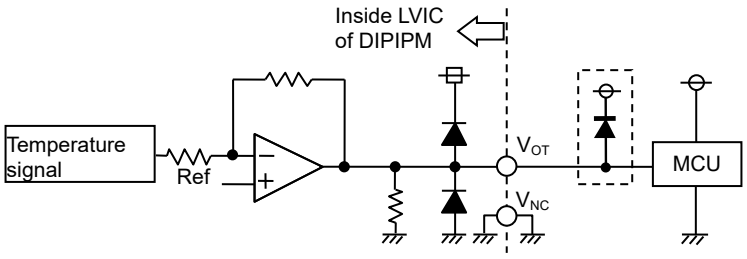


Fig.2-12 V_{OT} output circuit in the case of using with low voltage controller

And if it is needed to set the trip level of V_{OT} output to the control supply voltage (e.g. 3.3V) or more, there is the method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-13). In that case, sum of the resistances of divider circuit should be 5.1kΩ. About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clump diode. But it should be judged by the divided output level finally.

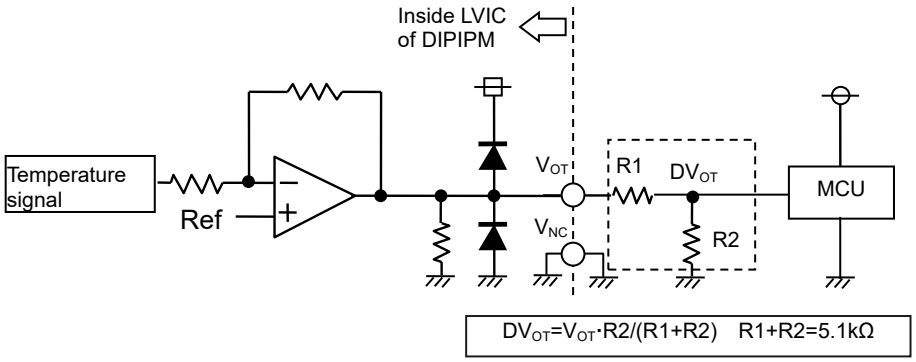


Fig.2-13 V_{OT} output circuit in the case with high protection level

(2) V_{OT} output characteristics

The characteristics of V_{OT} output vs. LVIC temperature is described as Fig.2-14. Please handle the following characteristics as reference data to set over temperature protection. These curves are based on theoretical designed value excluding specified value in the target specification.

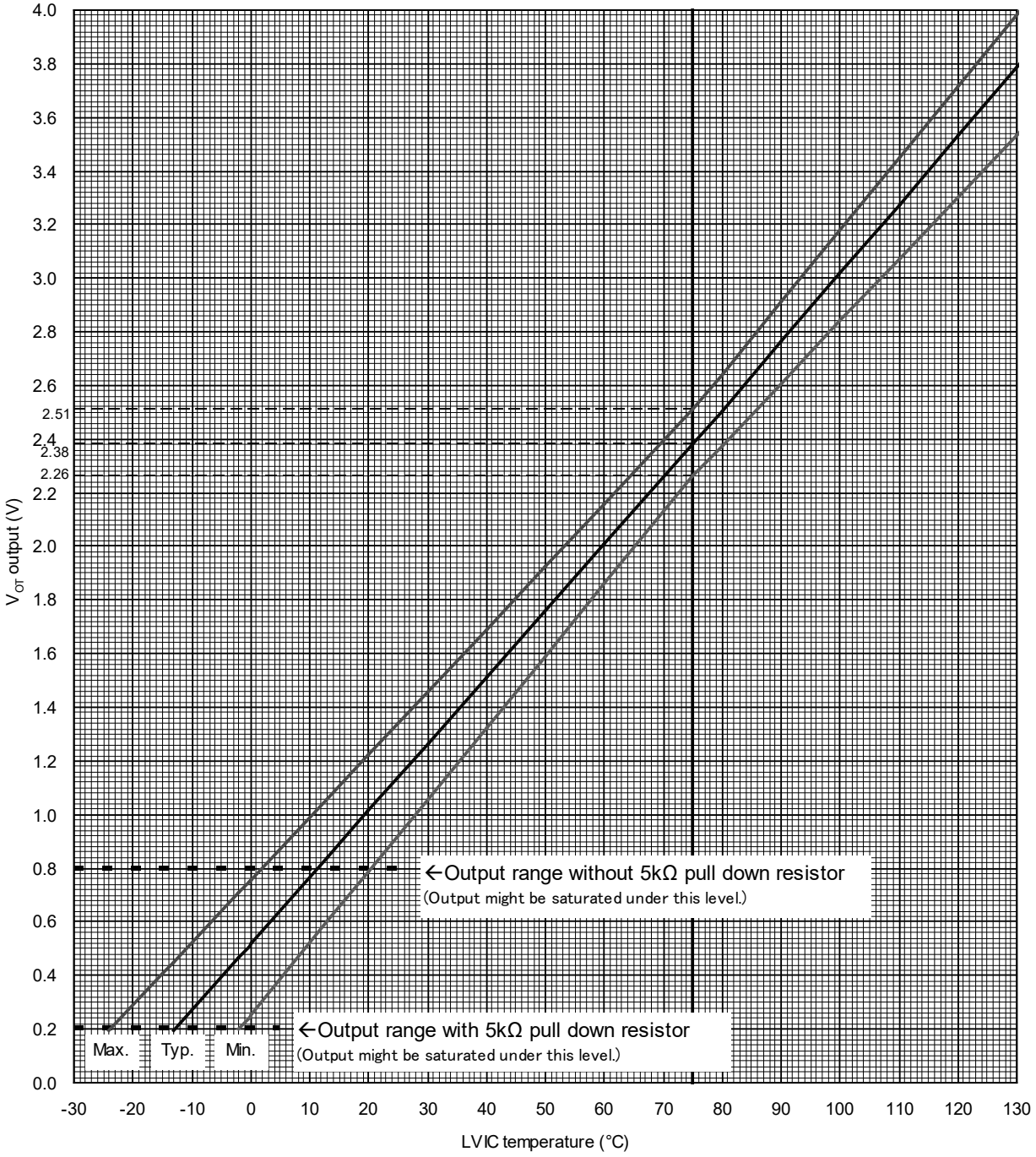


Fig.2-14 V_{OT} output vs. LVIC temperature

(3) How to use V_{OT} output

As mentioned above, the heat of power chips transfers to LVIC through the package and heat sink, and the relationship between LVIC temperature: Tic(=V_{OT} output), case temperature: Tc(measuring point is defined on the datasheet), and junction temperature: Tj depend on the system cooling condition, heat sink, control strategy, etc.

For example, the evaluation result about the relationship between IGBT loss and these temperature is described as Fig.2-15. This relationship may be different due to the cooling conditions. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system and consider the protection temperature keeps Tj ≤150°C.

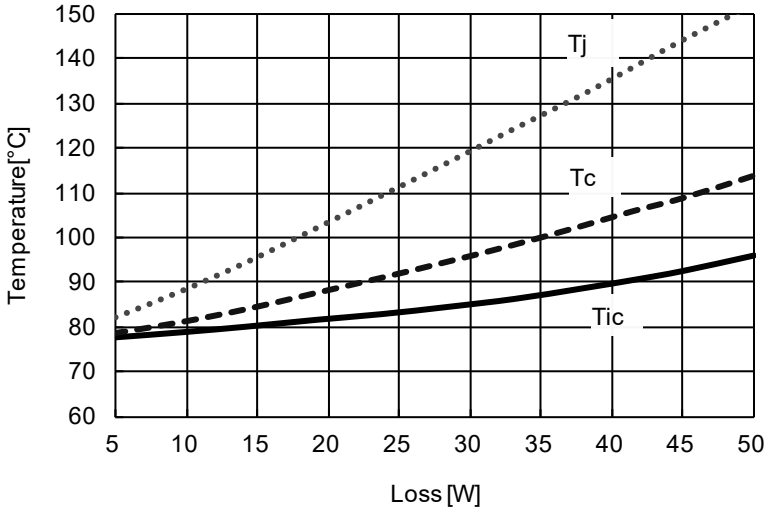


Fig.2-15 IGBT loss vs. Tj, Tc, Tic(Typical) (Ta=80°C)

Procedure about setting the protection level by using Fig.2-15 is described as below.

Table 2-13 Procedure for setting protection level

	Procedure	Setting value example
1)	Set the protection Tj temperature	Set Tj to 130°C as protection level.
2)	Get LVIC temperature Tic that matches to above Tj of the protection level from the relationship of Tj-Tic in Fig.2-16.	Tic=87.5°C (@Tj=130°C)
3)	Get V_{OT} value from the VOT output characteristics in Fig.2-17 and the Tic value which was obtained at 2) .	V_{OT}=2.70V (@Tic=87.5°C) is decided as the protection level.

As above procedure, the setting value for V_{OT} output is decided to 2.70V. But V_{OT} output has some data spread, so it is important to confirm whether the protection temperature fluctuation of Tj is not Tj>150°C due to the data spread of V_{OT} output. Procedure about the confirmation of temperature fluctuation is described in Table 2-14.

Table 2-14 Procedure for confirmation of temperature fluctuation

	Procedure	Confirmation example
4)	Confirm the region of Tic fluctuation at above V_{OT} from Fig.2-17.	Tic=82°C~94°C (@V_{OT}=2.70V)
5)	Confirm the region of Tj fluctuation at above region of Tic from Fig.2-16.	Tj=106°C~147°C (≤150°C, No problem) In this case, fluctuation of Tc is Tc=90°C~111°C

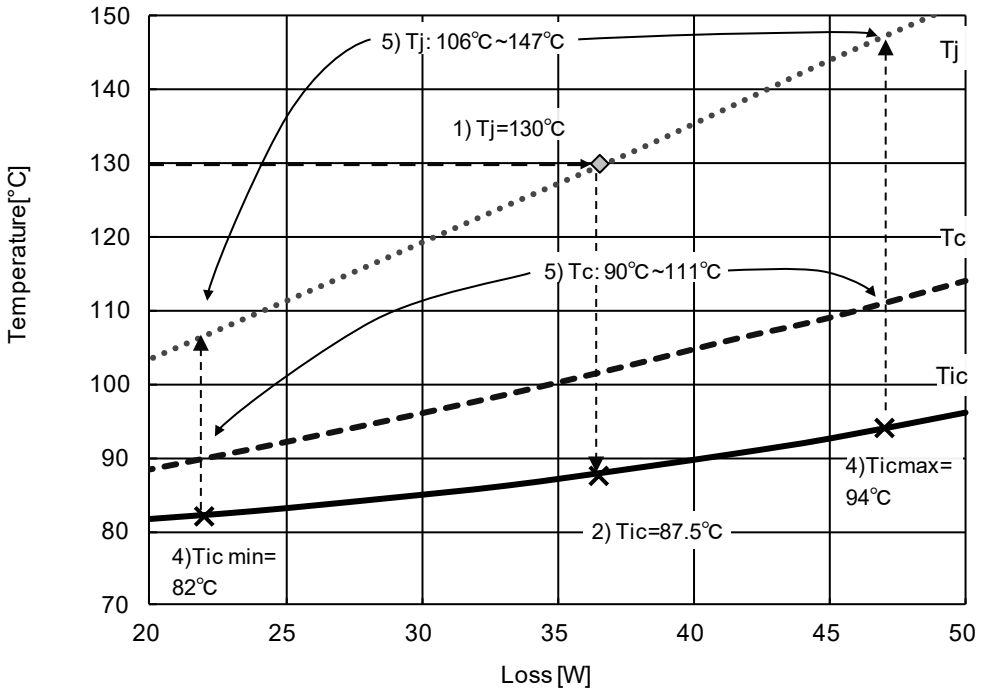


Fig.2-16 Relationship of Tj, Tc, Tic(Enlarged graph of Fig.2-15)

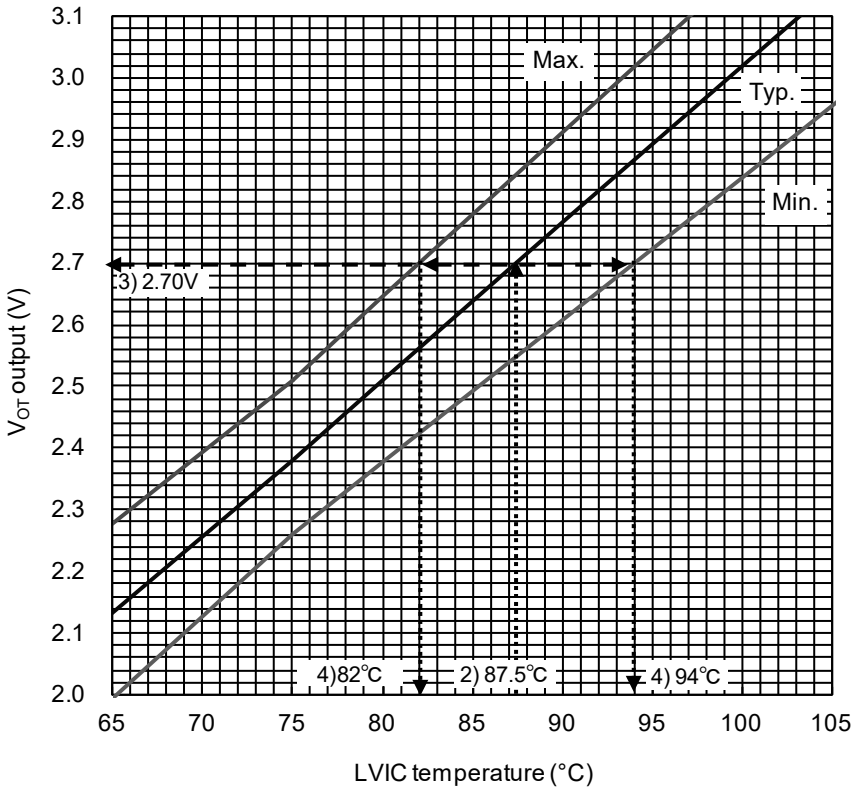


Fig.2-17 V_{OT} output vs. LVIC temperature (Enlarged graph of Fig.2-14)

The relationship between Tic, Tc(measuring) and Tj(calculated by loss) depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.
If necessary, it is available to prepare the sample with the individual data of V_{OT} vs. LVIC temperature.

2.3 Package Outlines

2.3.1 Outline Drawing

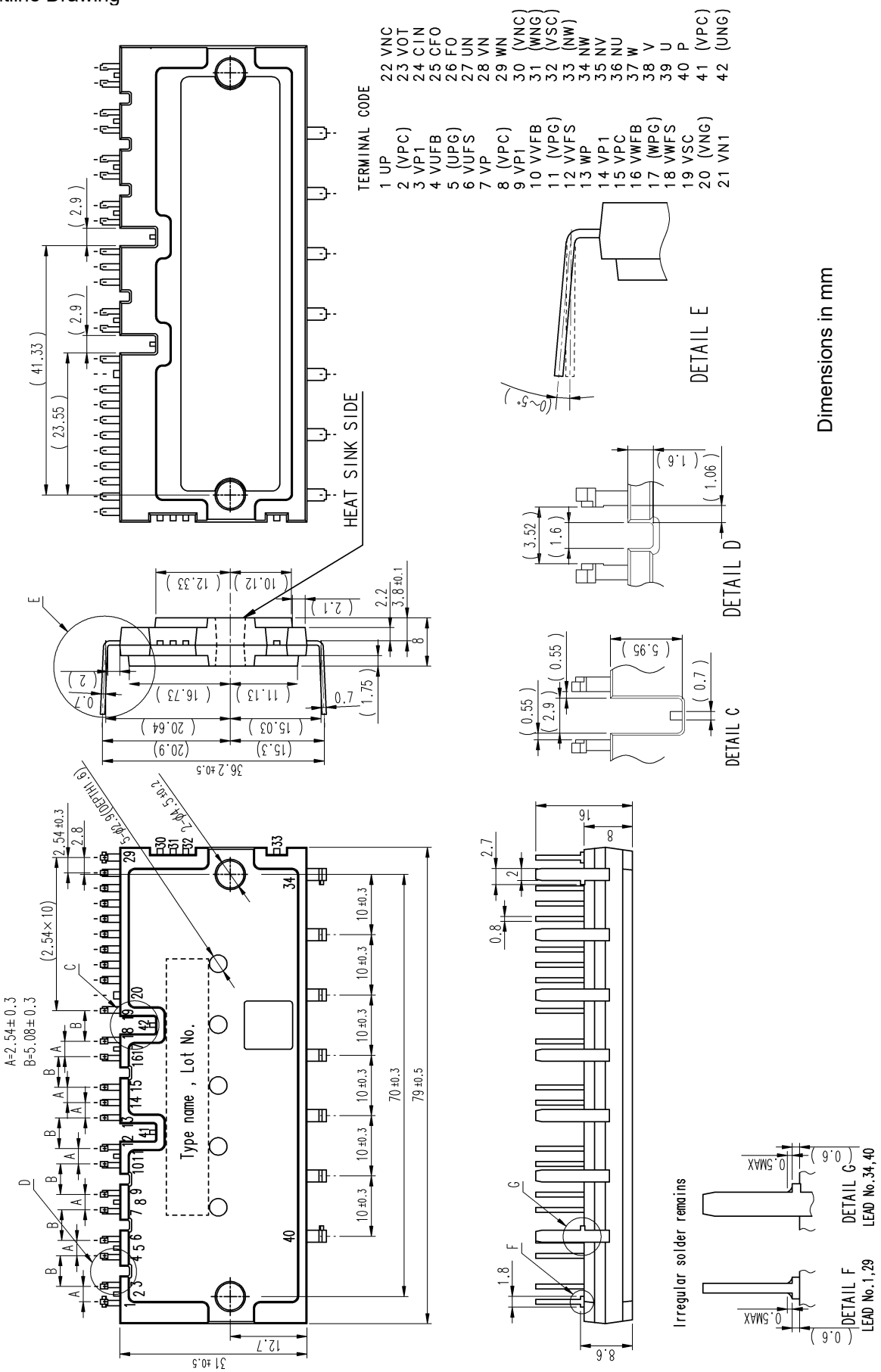


Fig.2-18 Outline drawing

2.3.2 Power Chip Position

Fig.2-19 indicates the center position of the each power chips.
(This figure is the view from laser marked side.)

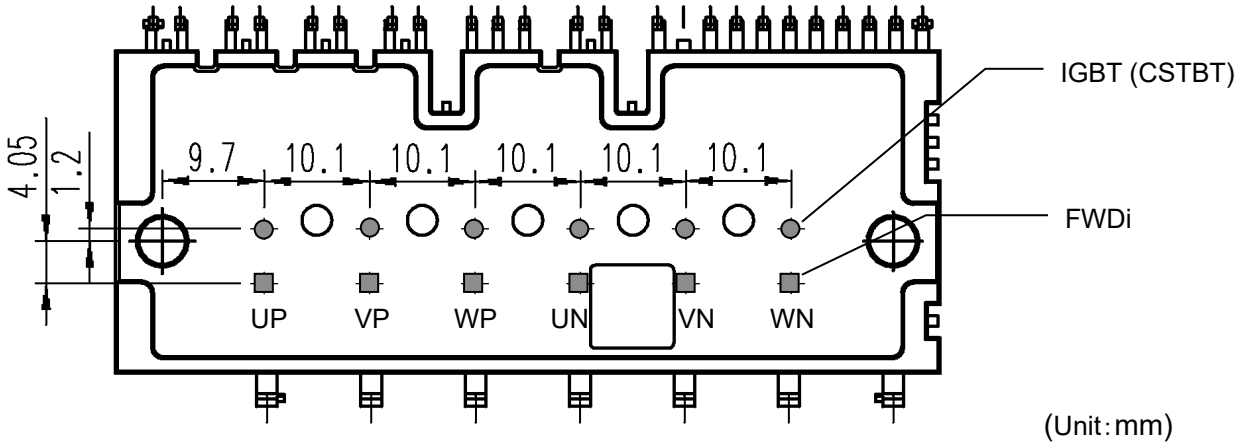


Fig.2-19 Power chip position

2.3.3 Marking Position

The laser marking specification is described in Fig.2-20.
Company name, Contry of origin, Type name, Lot number, and 2D code are marked in the upper side of module.

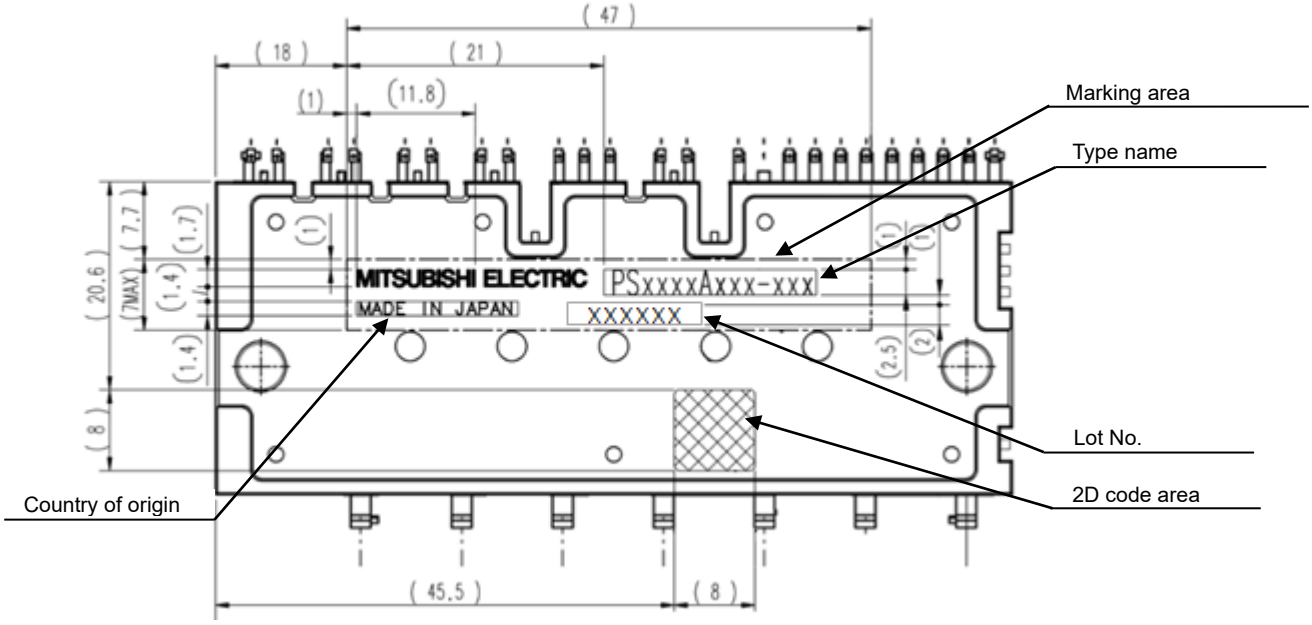


Fig.2-20 Laser marking view

The Lot number indicates production year, month, running number and country of origin.
The detailed is described as below.

(Example) H95AA1

- Running number
- Product month (however O: October, N: November, D: December)
- Last figure of Product year (e.g. 2019)
- Factory identification
  H : Manufactured at the factory in China

2.3.4 Terminal Description

Table 2-15 Terminal description

No.	Name	Description
1	U_P	U-phase P-side control input terminal
3	V_{P1}	U-phase P-side control supply positive terminal
4	V_{UFB}	U-phase P-side drive supply positive terminal
6	V_{UFS}	U-phase P-side drive supply GND terminal
7	V_P	V-phase P-side control input terminal
9	V_{P1}	V-phase P-side control supply positive terminal
10	V_{VFB}	V-phase P-side drive supply positive terminal
12	V_{VFS}	V-phase P-side drive supply GND terminal
13	W_P	W-phase P-side control input terminal
14	V_{P1}	W-phase P-side control supply positive terminal
15	V_{PC}	P-side control supply GND terminal
16	V_{WFB}	W-phase P-side drive supply positive terminal
18	V_{WFS}	W-phase P-side drive supply GND terminal
19	V_{SC}	Sense current detecting terminal
21	V_{N1}	N-side control supply positive terminal
22	V_{NC}	N-side control supply GND terminal
23	V_{OT}	LVIC temperature output terminal
24	CIN	SC trip voltage detect terminal
25	CFO	Fault pulse output width set terminal
26	F_O	Fault signal output terminal
27	U_N	U-phase N-side control input terminal
28	V_N	V-phase N-side control input terminal
29	W_N	W-phase N-side control input terminal
34	NW	W-phase N-side IGBT emitter terminal
35	NV	V-phase N-side IGBT emitter terminal
36	NU	U-phase N-side IGBT emitter terminal
37	W	W-phase output terminal
38	V	V-phase output terminal
39	U	U-phase output terminal
40	P	Inverter DC-link positive terminal

No.	Name	Description
2	V_{PC}	Internal use (Dummy pin) Don't connect all dummy pins to any other terminals or PCB pattern. (Leave no connect)
5	U_{PG}	
8	V_{PC}	
11	V_{PG}	
17	W_{PG}	
20	V_{NG}	
30	V_{NC}	
31	W_{NG}	
32	V_{SC}	
33	NW	
41	V_{PC}	
42	U_{NG}	

Table 2-16 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}- V_{UFS} V_{VFB}- V_{VFS} V_{WFB}- V_{WFS}	• Drive supply terminals for P-side IGBTs. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{PC} V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals. • Voltage input type. These are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Use RC coupling in case of signal oscillation.(Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ))
Sense current detect terminal	V_{SC}	• The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.
Short-circuit trip voltage detecting terminal	CIN	• Input the potential of Vsc terminal (with sense resisteor) to CIN terminal for SC protection through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal for N-side abnormal state(SC or UV). • This output is open drain type. It is recommended to pull up F_O signal line to the 5V supply by 10kΩ when Fo signal is input to MCU directly (Check whether the V_{FO} satisies the threshold level of input of MCU when selecting resistance). • In the case of directly driving opto coupler by Fo output it is needed to set the pull-up resistance so that I_{FO} becomes under 5mA(maximum rating). And pulled up to 15V supplyis recommended.(V_{FO} increases in propotion to increasing $I_{FO.}$)
Fault pulse output width setting terminal	CFO	• The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and V_{NC}. • When 22nF capacitor is connected, then the Fo pulse width becomes 2.4ms. $C_{FO} = t_{FO} \times 9.1 \times 10^{-6}$ (F)
Temperature output terminal	V_{OT}	• LVIC temperature is ouput by analog signal. It is ouput of OP amplifer internally. • It is recommended to connect 5.1kΩ pulldown resistor if output linearlity is necessary under room temperature.
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU,NV,NW	• Open emitter terminal of each N-side IGBT • If usage of common emitter is needed, connect these terminals together at the point as close from the package as possible.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.

Note: Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

2.4 Mounting Method

This section shows the electric spacing and mounting precautions.

2.4.1 Electric Spacing

The electric spacing specification is shown in Table 2-17

Table 2-17 Minimum insulation distance

	Clearance (mm)	Creepage (mm)
Between live power terminals with high potential	7.1	7.8
Between live control terminals with high potential	3.1	5.6
Between terminals and heat sink	3.7	5.6

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-21. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention to the foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test(e.g. insulation inspection) on the final product after fixing the DIPIPM with the heatsink.

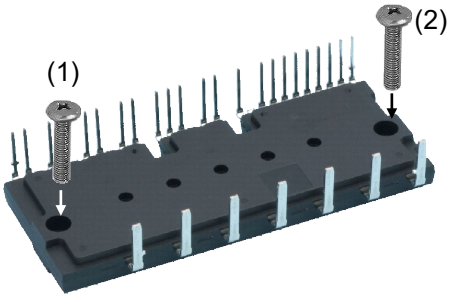


Fig.2-21 Recommended screw fastening order

Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Table 2-18 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 1.18N·m, Screw : M4	0.98	-	1.47	N·m
Flatness of outer heat sink	Refer Fig.2-22	-50	-	+100	μm

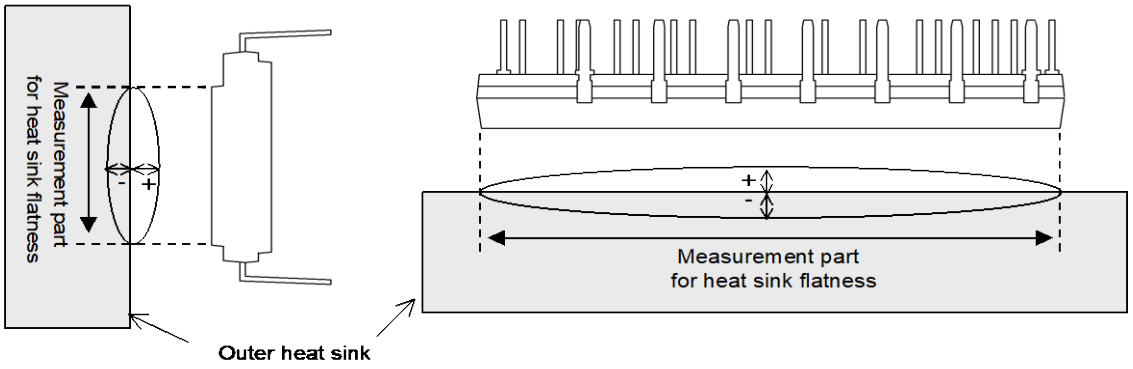


Fig.2-22 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.2K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

Pay attenction to the selection of thermal conductiove grease. The grease thickness after fixing the heatsink may increase due to the properties of the grease (contained filler diameter, viscosity, amount of application and so on). And it may cause increase of contact thermal resistance or package crack. Please contact thermal conductive grease manufacturer for its detailed characteristics.

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in Table 2-19 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s. However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, and the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-19 Reliability test specification

Item	Condition
Soldering Thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, we cannot suggest the recommended temperature condition for hand soldering.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept lower than 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample: Large DIPIPM Ver.6

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe. (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

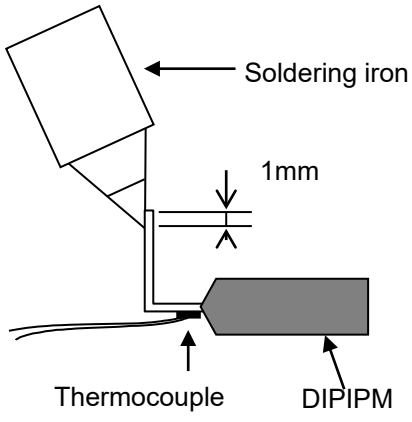


Fig.2-23 Heating and measuring point

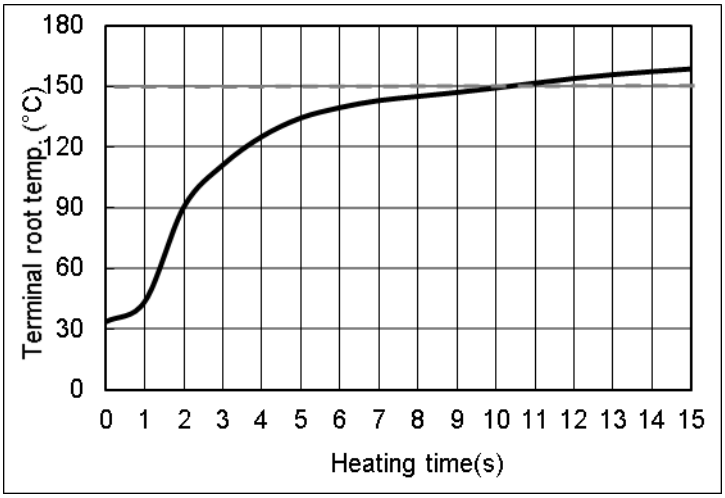


Fig.2-24 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

CHAPTER 3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance

This chapter states usage and interface circuit design hints.

3.1.1 System Connection

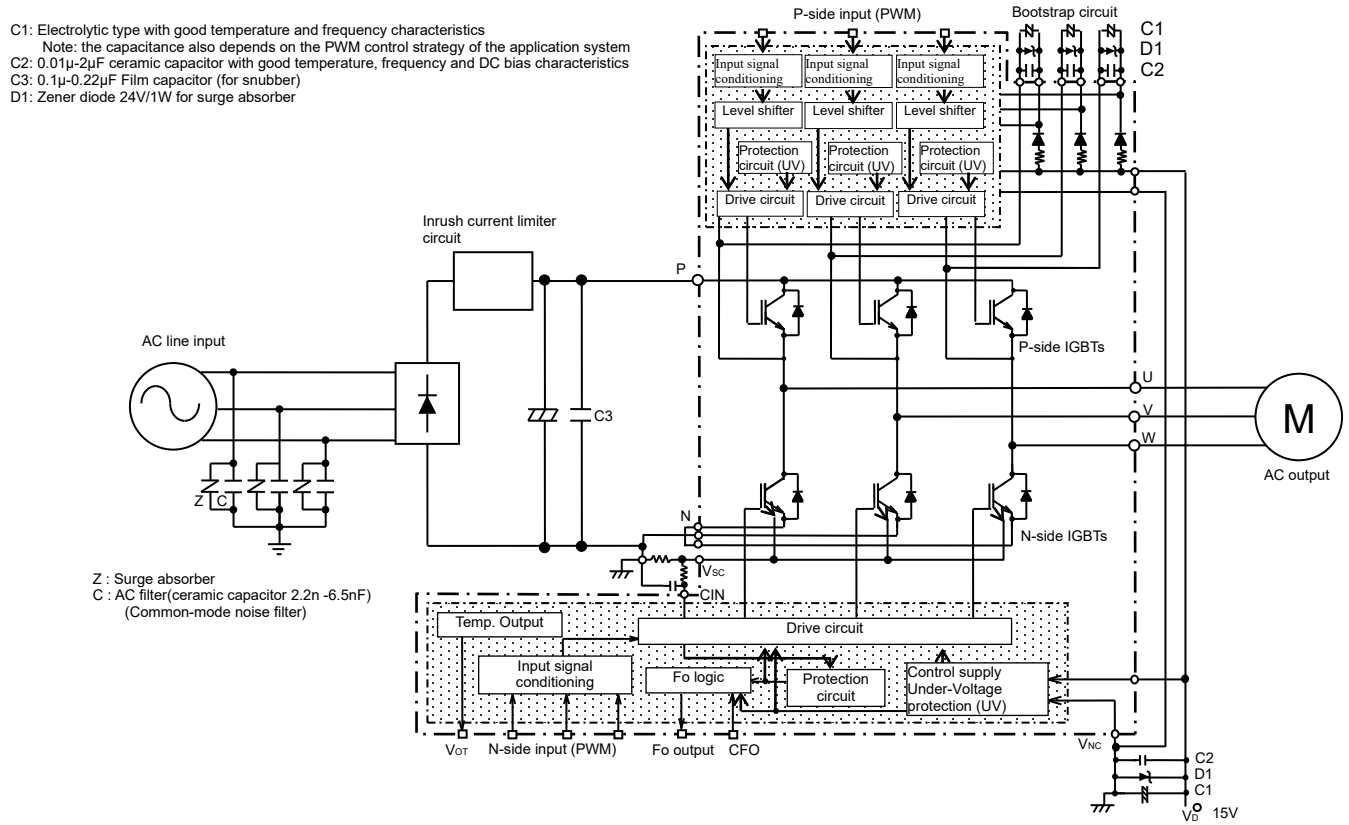


Fig.3-1 Application System block diagram

3.1.2 Interface Circuit (Direct Coupling Interface example)

Fig.3-2 shows a typical application circuit of connecting with MCU or DSP directly.

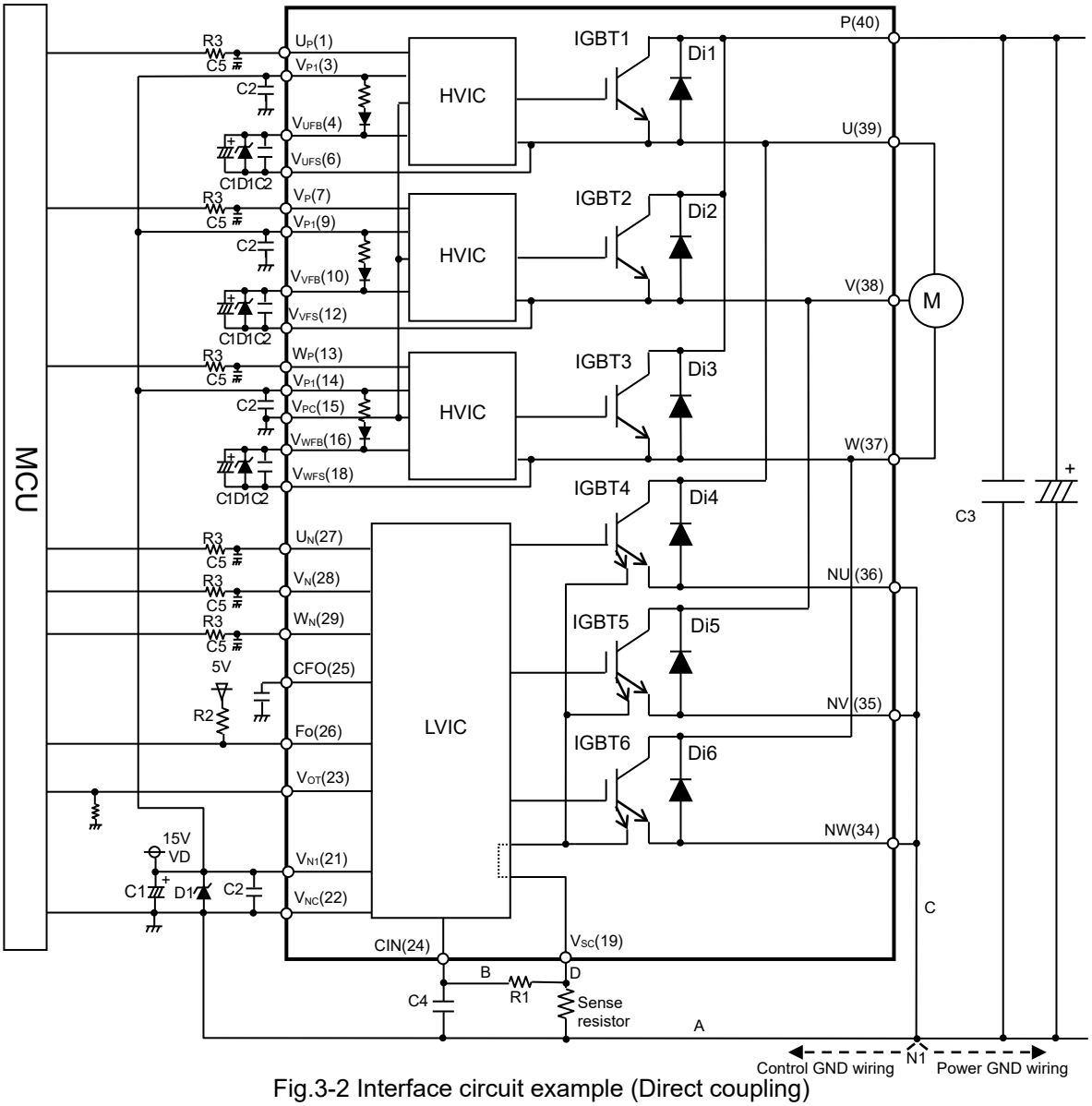


Fig.3-2 Interface circuit example (Direct coupling)

Note

1 :If control GND and power GND are patterned by common wiring, it may cause malfunction by fluctuation of power GND level. It is recommended to connect control GND and power GND at only a N1 point at which NU, NV, NW are connected to power GND line.

2 :It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.

3 :To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally inserting a 0.1μ~0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

4 :R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is recommended. If R1 is too small, it may leads to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (100 times is recommended.)

5 :To prevent erroneous operation, the wiring of A, B, C should be as short as possible.

6 :For sense resistor, the variation within 1%(including temperature characteristics), low inductance type is recommended. And the over 0.03W is recommended, but it is necessary to evaluate in your real system finally.

7 :To prevent erroneous SC protection, the wiring from V_{SC} terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.

8 :All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.01μ~2.0μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)

9 :Input drive is High-active type. There is a min. 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. And it is recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

10 :Fo output is open drain type. Fo output will be max 0.95V(@I_{FO}=1mA,25°C), so it should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (In the case of pulled up to 5V, 10kΩ is recommended.)

11 :Error signal output width (t_{Fo}) can be set by the capacitor connected to C_{FO} terminal. C_{FO}(typ.) = t_{Fo} x (9.1 x 10^{-6}) (F)

12 :If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.

13 :For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.

3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

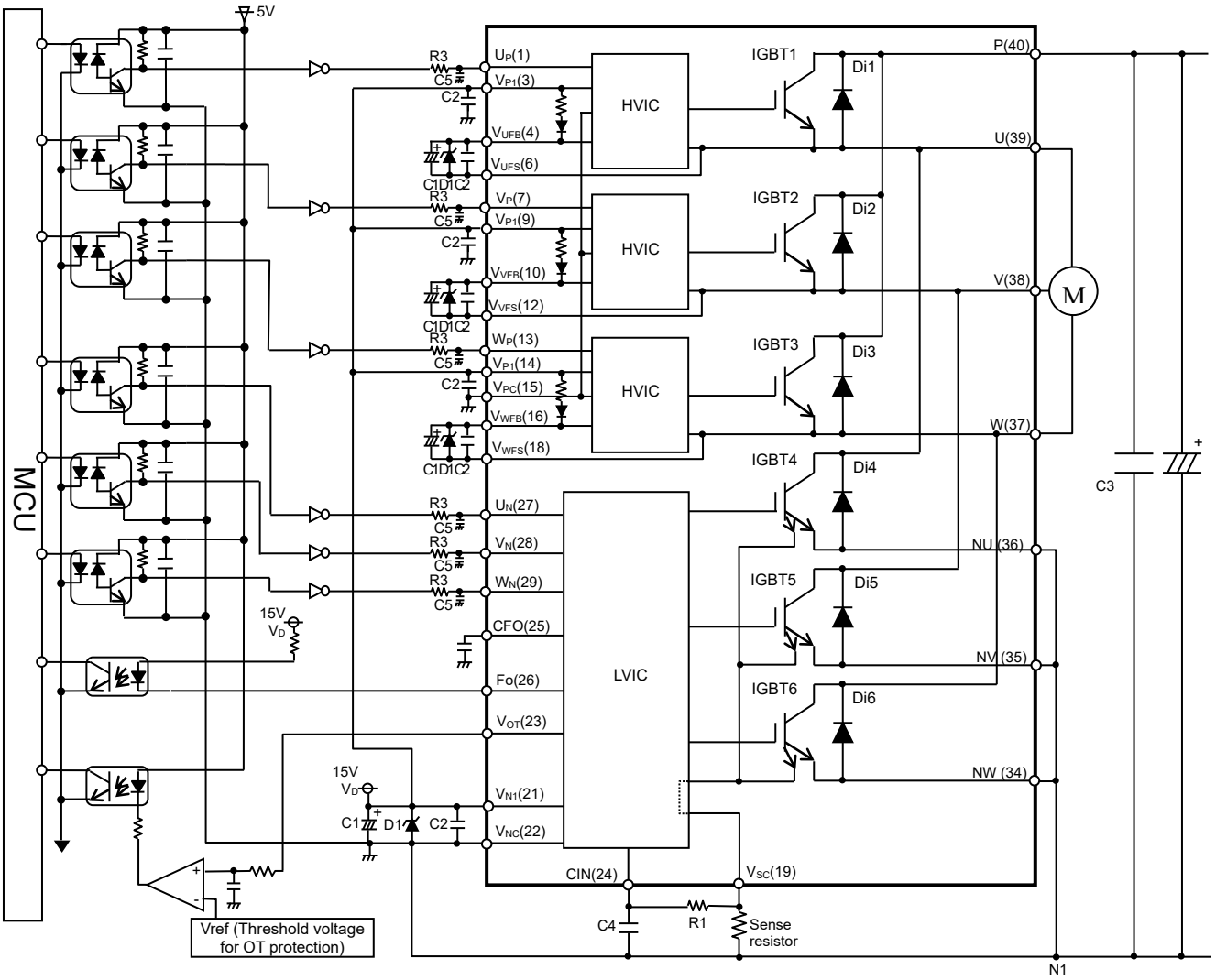


Fig.3-3 Interface circuit example with opto-coupler

Note:

(1) High speed (high CMR) opto-coupler is recommended.
(2) Set the current limiting resistance to make Fo sink current I_{FO}= 5mA or less when the opto-coupler is driven by Fo output directly. To assure I_{FO}=5mA, it will be needed to pull up to 15V supply since Fo output may be max 4.75V(@I_{FO}=5mA, 25℃).
(3) To prevent malfunction, it is strongly recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet turn-on and turn-off threshold voltage.
(4) About comparator circuit at V_{OT} output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

3.1.4 Circuits of Signal Input terminals and Fo Terminal

Input logic is high-active. A 3.3kΩ(min) pull-down resistor is built-in each input circuit of the DIPIPM as shown in Fig.3-4, so external pull-down resistor is not needed.

When using same PCB for 600V large DIPIPM Ver.4 PS21A7* series and this series which have same package, it needs to give attention to the difference of input threshold voltage.

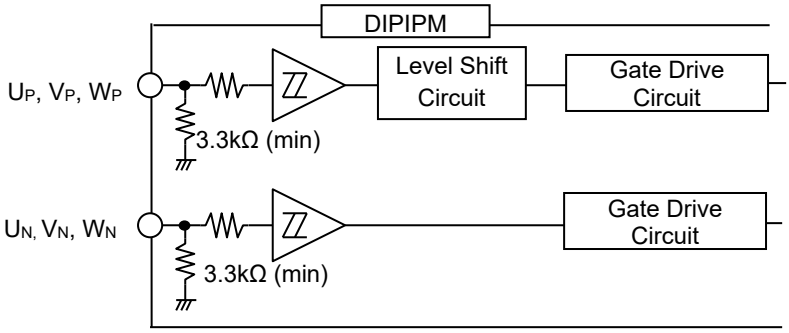


Fig.3-4 Internal structure of control input terminals

Table 3-1 Input threshold voltage ratings (Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{PC} U_N,V_N,W_N-V_{NC}	-	-	3.5	V
Turn-off threshold voltage	Vth(off)		0.8	-	-	

The wiring of each input should be patterned as short as possible and it is recommended to insert RC filter. There are limits for the minimum input pulse width in the DIPIPM. DIPIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Refer Table 3-2)

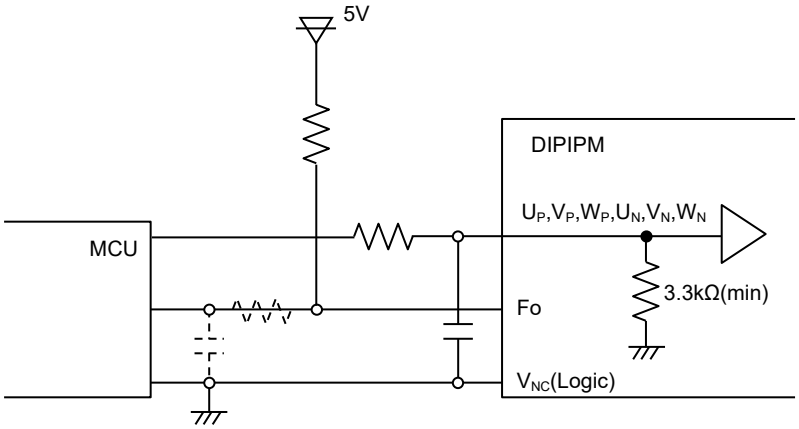


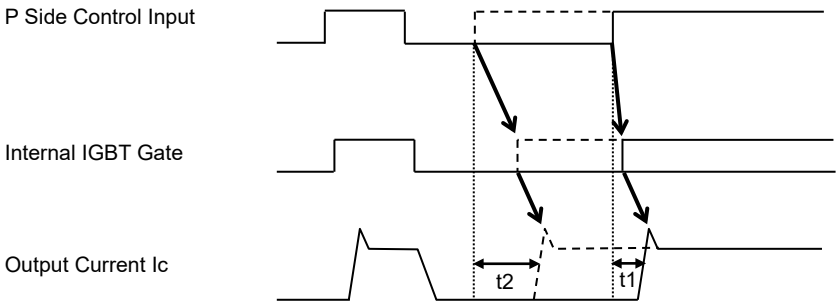
Fig.3-5 Control input connection in the case of direct connection with MCU

Note: Design for input RC filter depends on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. It is recommended to insert RC filter. (Time constant: over 100ns. e.g. 100Ω, 1000pF)
DIPIPM input signal interface integrates a 3.3kΩ(min.) pull-down resistor. Therefore, when using RC filter, be careful to satisfy the turn-on threshold voltage requirement.

Table 3-2 Allowable minimum input pulse width

	Symbol	Condition		Type Name	Minimum value	Unit
On signal	PWIN(on)			PSS05SA2FT	1.5	μs
				PSS10SA2FT		
				PSS15SA2FT		
				PSS25SA2FT		
				PSS35SA2FT		
				PSS50SA2FT		
				PSS75SA2FT		
Off signal	PWIN(off)	$350 \leq V_{CC} \leq 800V$, $13.5 \leq V_D \leq 16.5V$, $13.5 \leq V_{DB} \leq 18.5V$, $-20 \leq T_C \leq 100°C$, N line wiring inductance less than 10nH	Up to rated current	PSS05SA2FT	3.0	
				PSS10SA2FT		
				PSS15SA2FT		
				PSS25SA2FT		
				PSS35SA2FT		
				PSS50SA2FT		
				PSS75SA2FT		
			From rated current to 1.7x rated current	PSS05SA2FT	3.5	
				PSS10SA2FT		
				PSS15SA2FT		
				PSS25SA2FT		
				PSS35SA2FT		
				PSS50SA2FT		
				PSS75SA2FT		

*) Input signal with ON pulse width less than PWIN(on) might make no response.
IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).
Refer Fig.3-6 about delayed response .



Real line: off pulse width>PWIN(off); turn on time t1
Broken line: off pulse width<PWIN(off); turn on time t2
(t1:Normal switching time)

Fig.3-6 Delayed response with shorter input off (P-side only)

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type. When Fo output is input into MCU(controller) directly, it is necessary to note the dependency of V_{FO} on I_{FO} (V_{FO}=max0.95V @I_{FO}=1mA, 25°C) and set pull up resistance so that Fo signal level fits to the input threshold voltage of MCU. In the case of pulling up to 5V supply, it is recommended to pull up by 10kΩ resistor.

When the opto-coupler is driven by Fo output directly, the maximum Fo sink current becomes 5mA or less. To assure I_{FO}=5mA, it will be needed to pull up to 15V supply since Fo output may be max 4.75V (@I_{FO}=5mA, 25°C).

If max 5mA coupler driving current is not enough, it is necessary to apply buffer circuit for increasing driving current.

Fig.3-7 shows the typical V-I characteristics of Fo terminal.

Table 3-3 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V,Fo=10kΩ, 5V pulled-up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V,Fo=1mA	-	-	0.95	V

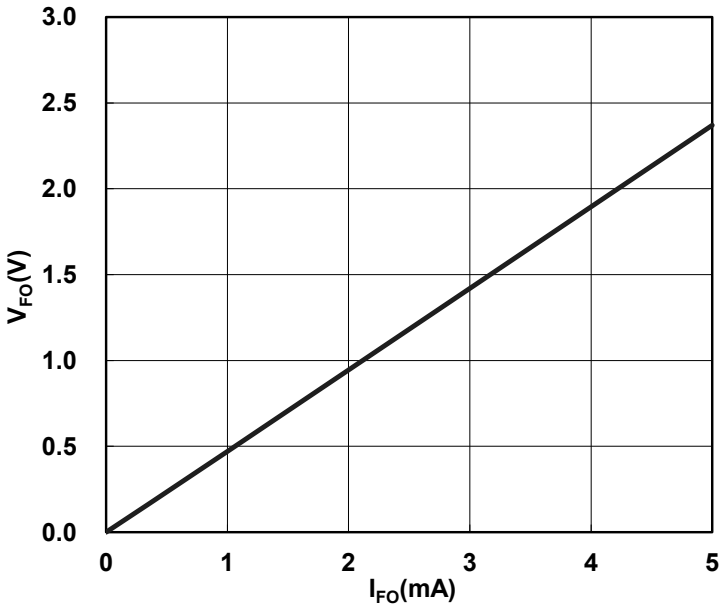


Fig.3-7 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.5 Snubber Circuit

In order to prevent DIPIPM from the surge destruction, the wiring length between the smoothing capacitor and DIPIPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible as Fig.3-8.

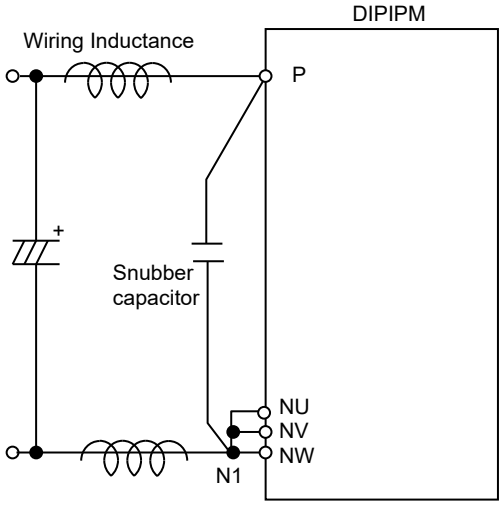


Fig.3-8 Recommended snubber circuit position

3.1.6 Influence of Wiring

Influence of pattern wiring around the sense resistor for SC protection and GND is shown below.

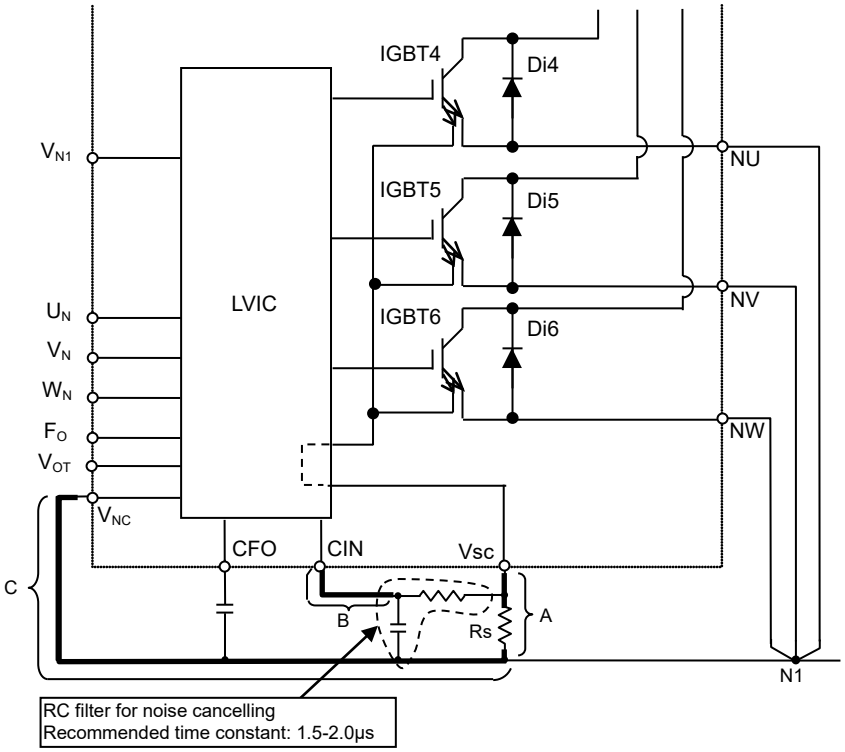


Fig.3-9 External protection circuit

(1) Influence of the part-A wiring

The part-A wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-A wiring is too long, extra surge voltage generated by the wiring inductance will lead to fluctuation of SC protection level. This wiring should be as short as possible for limiting the surge voltage.

(2) Influence of the part-B wiring pattern

RC filter is added to remove noise influence occurring on the sense resistor. Filter effect will dropdown and noise will easily superimpose on the wiring, if part-B wiring (=after filtering part) is too long. Please install the RC filter near CIN, VNC terminals as close as possible.

(3) Influence of the part-D wiring pattern

Part-C wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

3.1.7 Precaution for Wiring on PCB

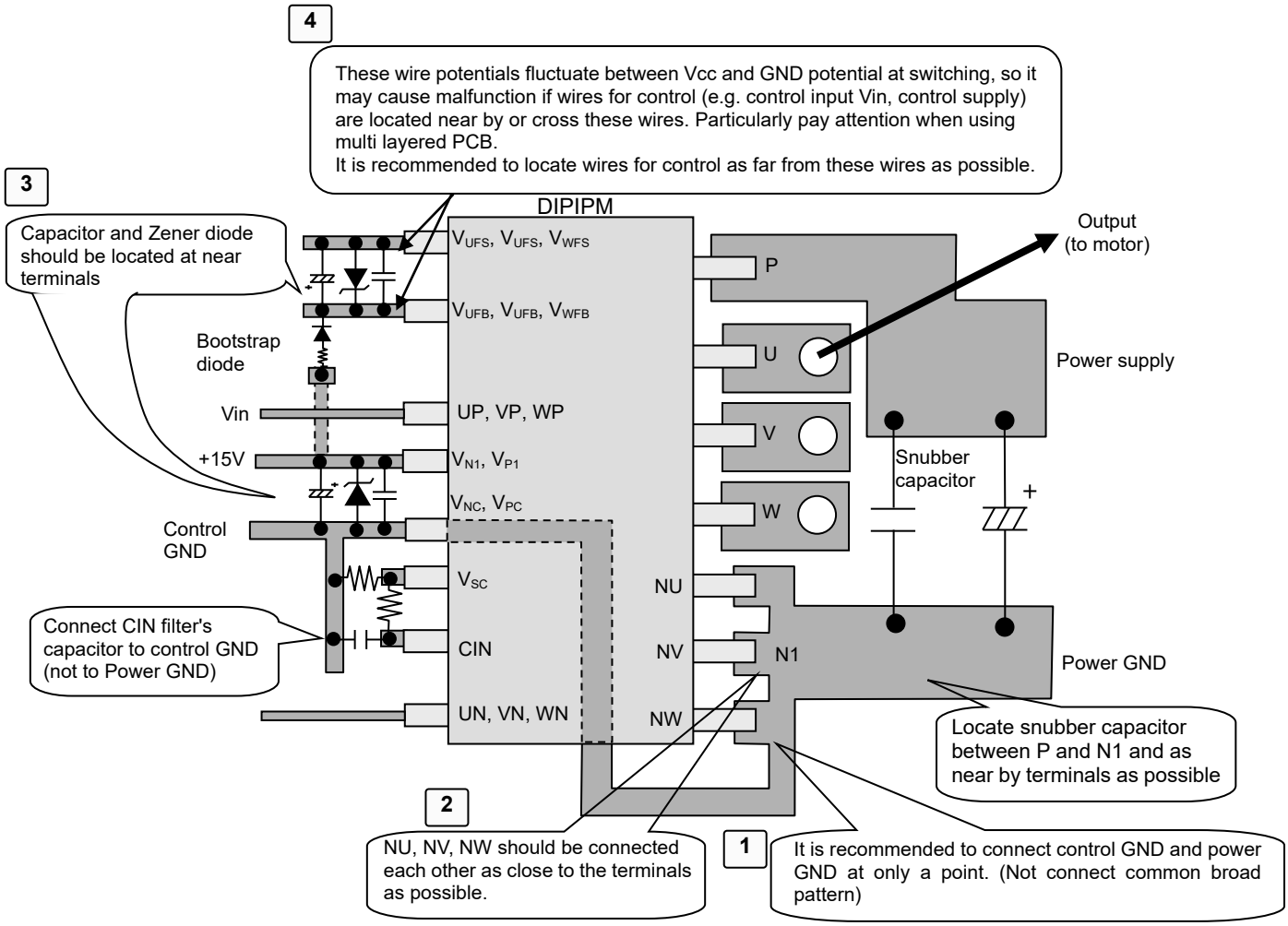


Fig.3-10 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. it causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short occurs.
2	•Long pattern between NU, NV, NW terminals and N1	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction occurs.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then incorrect signals are input to DIPIPM input, and arm short (short circuit) might occur.

3.1.8 SOA of DIPIPM

The following describes the SOA (Safety Operating Area) of DIPIPM.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: The total amount of V_{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(PROT)}$: DC-link voltage that DIPIPM can protect itself.

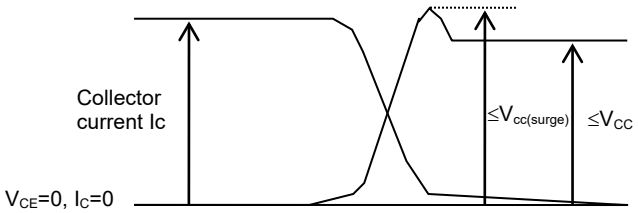


Fig.3-11 SOA at switching mode

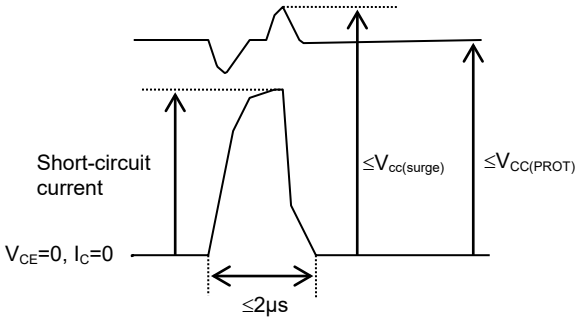


Fig.3-12 SOA at short-circuit mode

In case of switching

V_{CES} represents the maximum voltage rating (1200V) of the IGBT. By subtracting the surge voltage (200V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 1000V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC}, that is 900V.

In case of Short-circuit

V_{CES} represents the maximum voltage rating (1200V) of the IGBT . By Subtracting the surge voltage (200V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 1000V. Furthermore, by subtracting the surge voltage (200V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC}, that is, 800V.

3.1.9 SCSOA

Fig.3-13 ~ Fig.3-19 show the typical SCSOA performance curves

.

Conditions: Vcc=800V, Tj=125°C at initial state, Vcc(surge)≤1000V(surge included), non-repetitive, 2m load.

In the case of PSS05SA2FT (5A rating) it means DIPIPM can shutdown maximum 71A(@V_D=16.5V) short circuit current safely if IGBT turn on period is within 4.6μs(typical).

Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

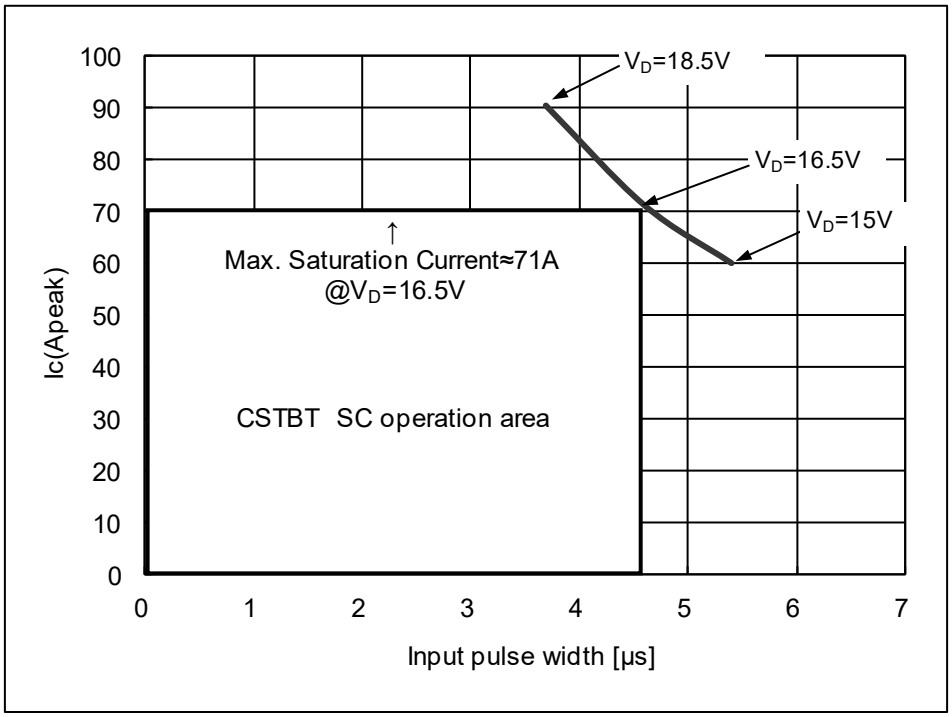


Fig.3-13 PSS05SA2FT typical SCSOA curve

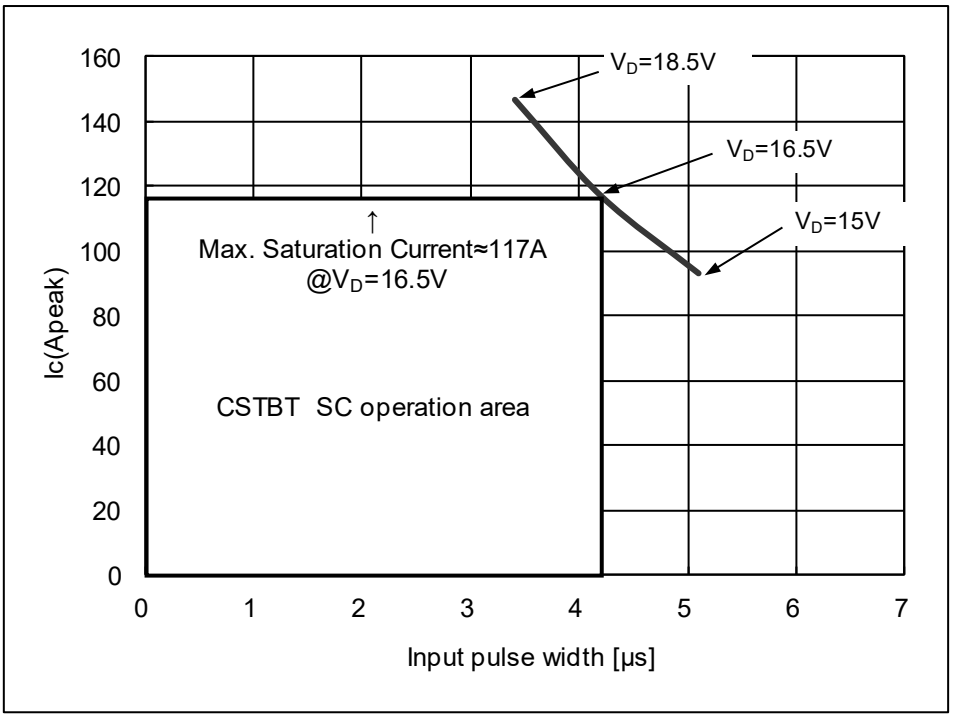


Fig.3-14 PSS10SA2FT typical SCSOA curve

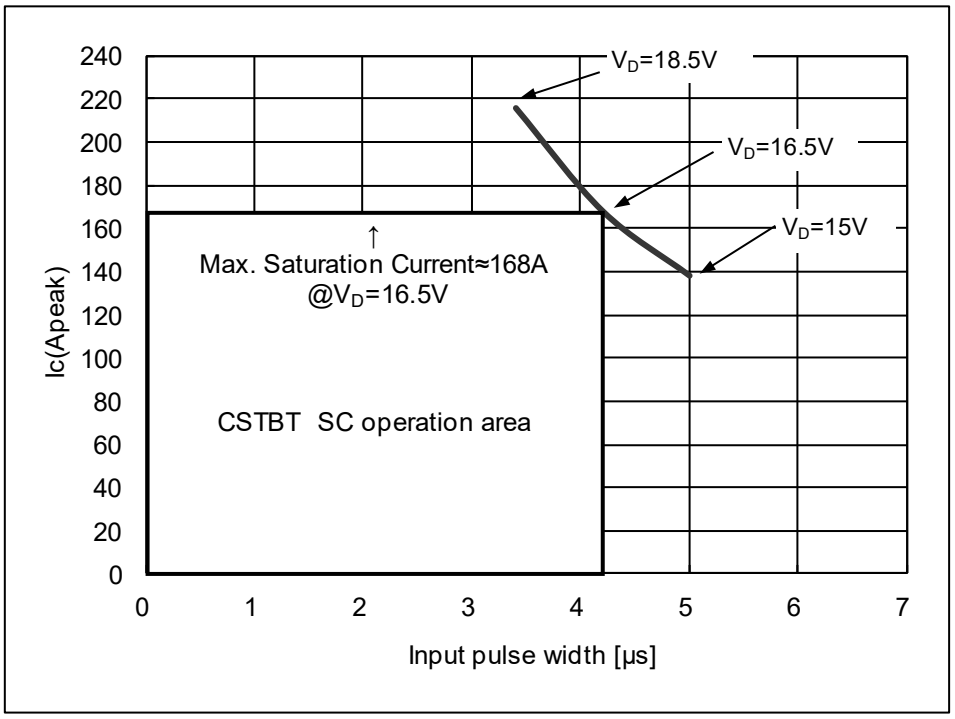


Fig.3-15 PSS15SA2FT typical SCSOA curve

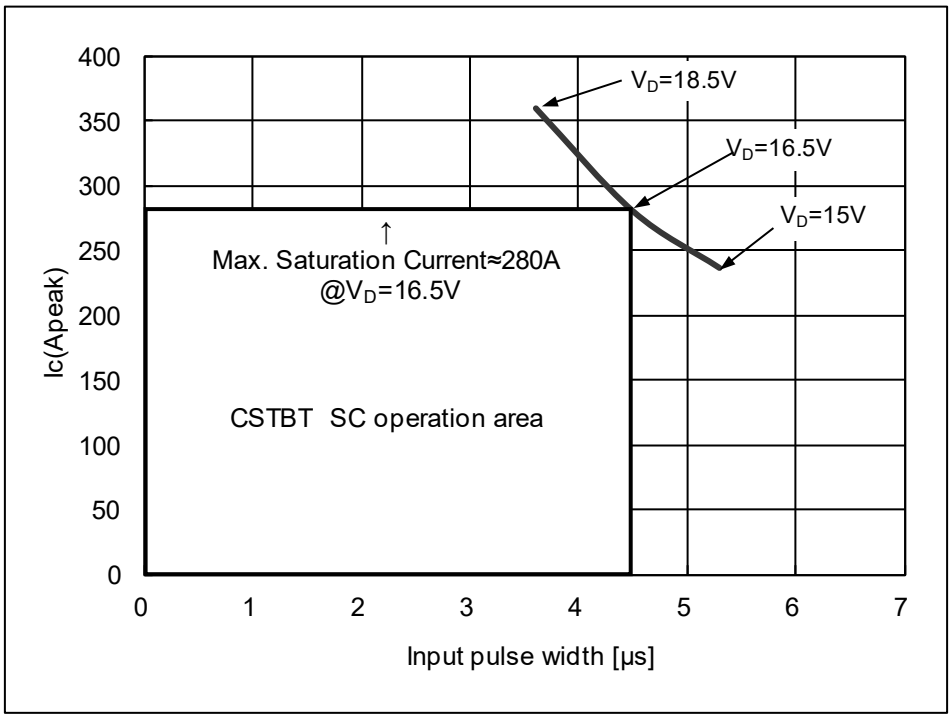


Fig.3-16 PSS25SA2FT typical SCSOA curve

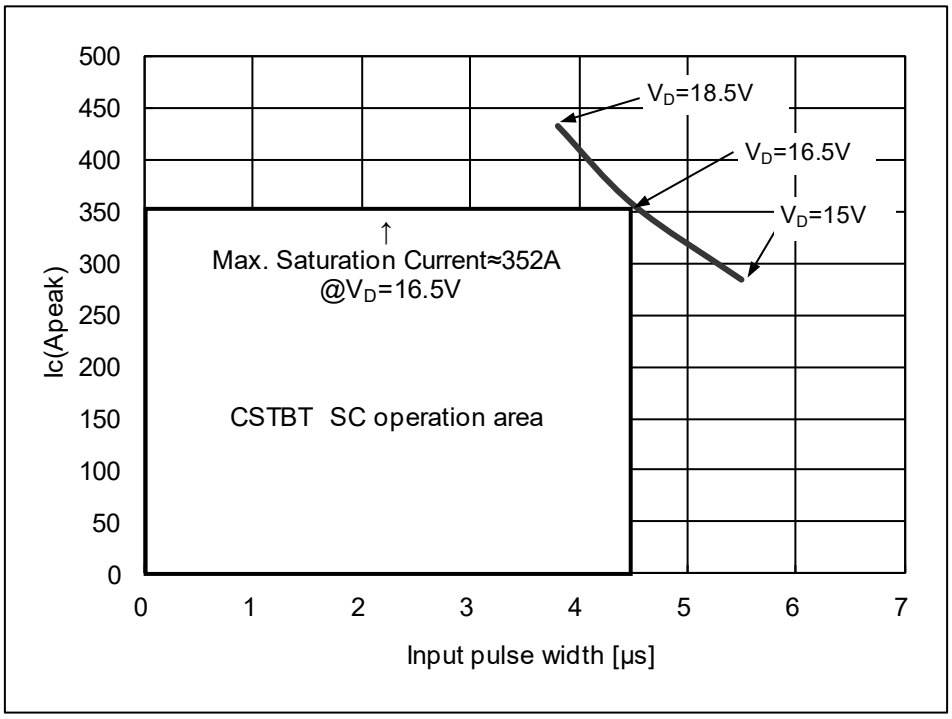


Fig.3-17 PSS35SA2FT typical SCSOA curve

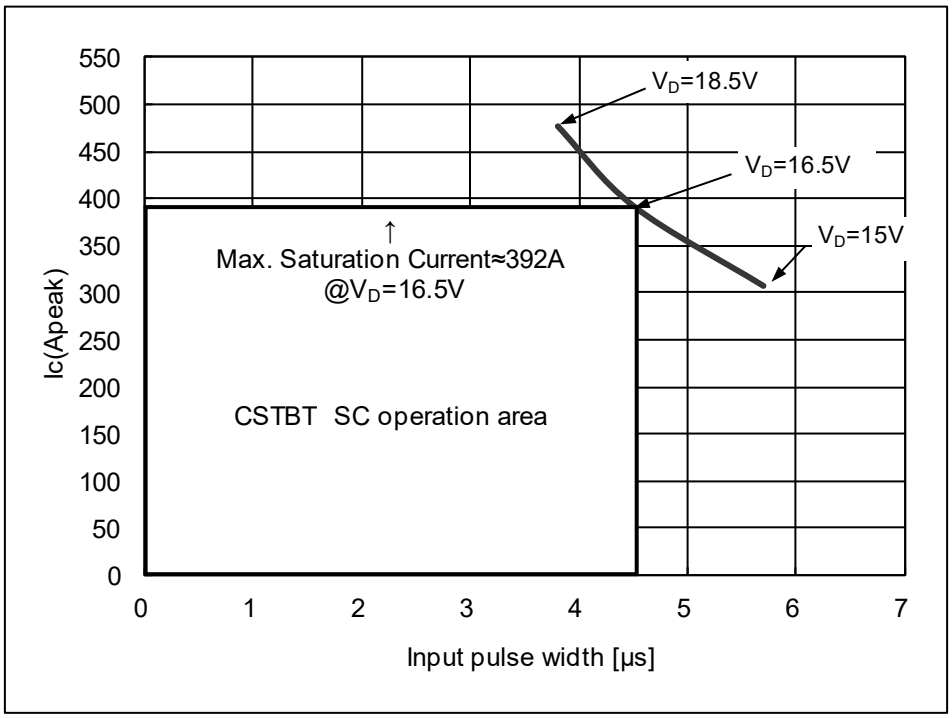


Fig.3-18 PSS50SA2FT typical SCSOA curve

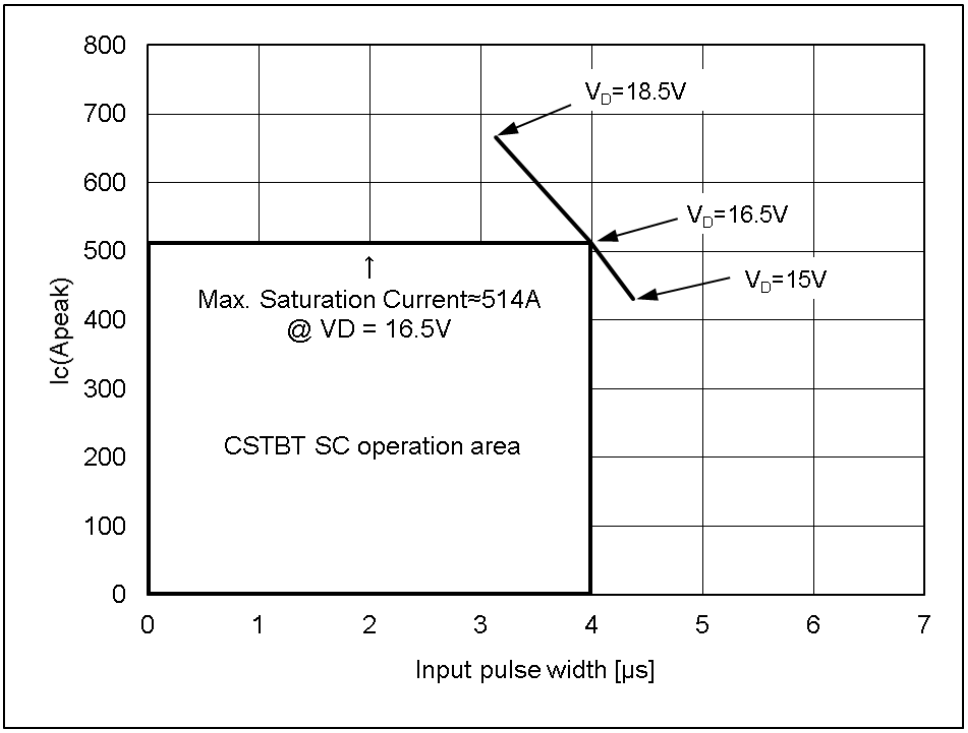


Fig.3-19 PSS75SA2FT typical SCSOA curve

3.1.10 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happens on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-20 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj).

(The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

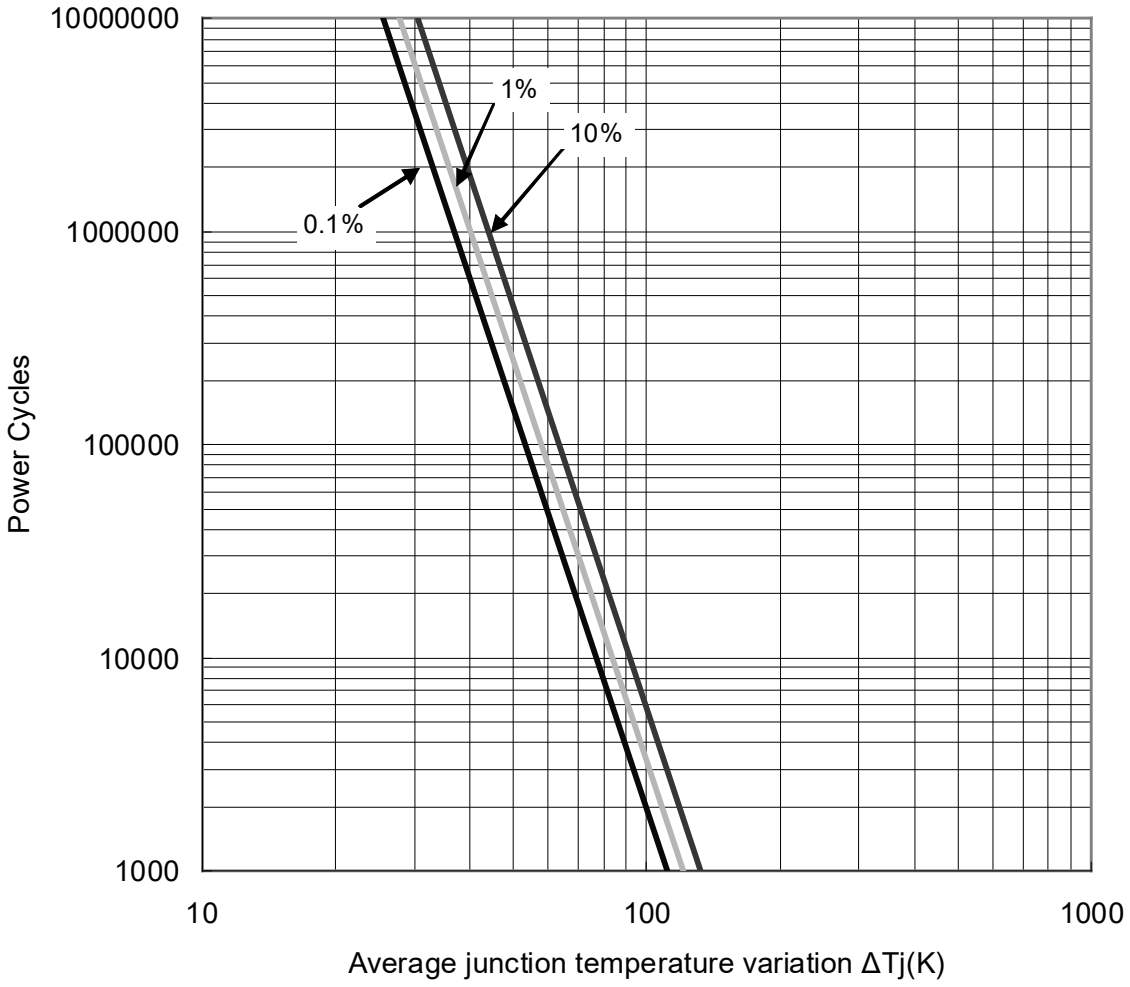


Fig.3-20 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Simulation

For calculating power loss and temperature rising, the power loss simulator "Melcosim" is prepared in our WEB site. This simulator can make the calculation of inverter loss and temperature rise easy.

The 'Melcosim' can be downloaded from http://www.mitsubishielectric.com/semiconductors/

Simple expressions for calculating average power loss are given below:

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$
$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\, Icp \times \sin x)$$
$$Vec = (-1) \times Vec(@\, Iecp(= Icp) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Icp \times \sin x) \times Vce(sat)(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} ((-1) \times Icp \times \sin x)((-1) \times Vec(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Psw(on)(@\, Icp \times \sin x) + Psw(off)(@\, Icp \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-21, and its dynamic loss can be calculated by the following expression:

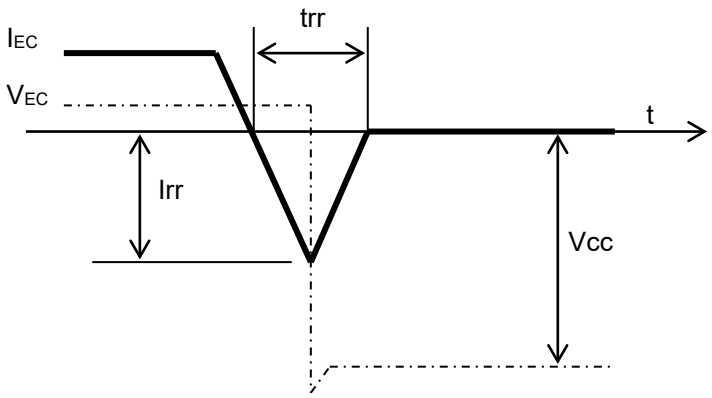


Fig.3-21 Ideal FWDi recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@Icp \times \sin x) \times Vcc \times trr(@Icp \times \sin x)}{4} \times fc \bullet dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@Icp \times \sin x) \times Vcc \times trr(@Icp \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at Tj=125°C.

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-22 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{CC}=600V, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., P.F=0.8, Switching loss=Typ., Tj=125°C, Tc=100°C,
Rth(j-c)=Max., 3-phase PWM modulation, 60Hz sine waveform output

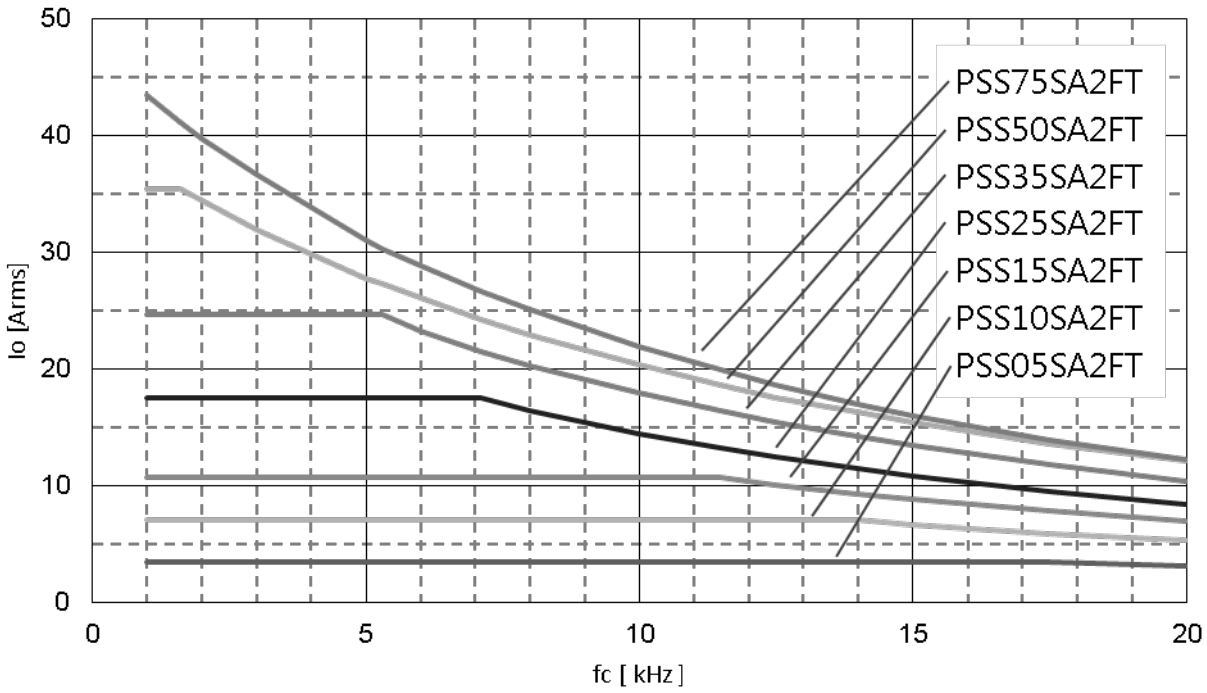


Fig.3-22 Effective current-carrier frequency characteristic

Fig.3-22 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tc=100°C and Tj=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.
The inverter loss can be calculated by the free power loss simulation software can be downloaded from the Mitsubishi Electric web site. (URL: http://www.mitsubishielectric.com/semiconductors/)

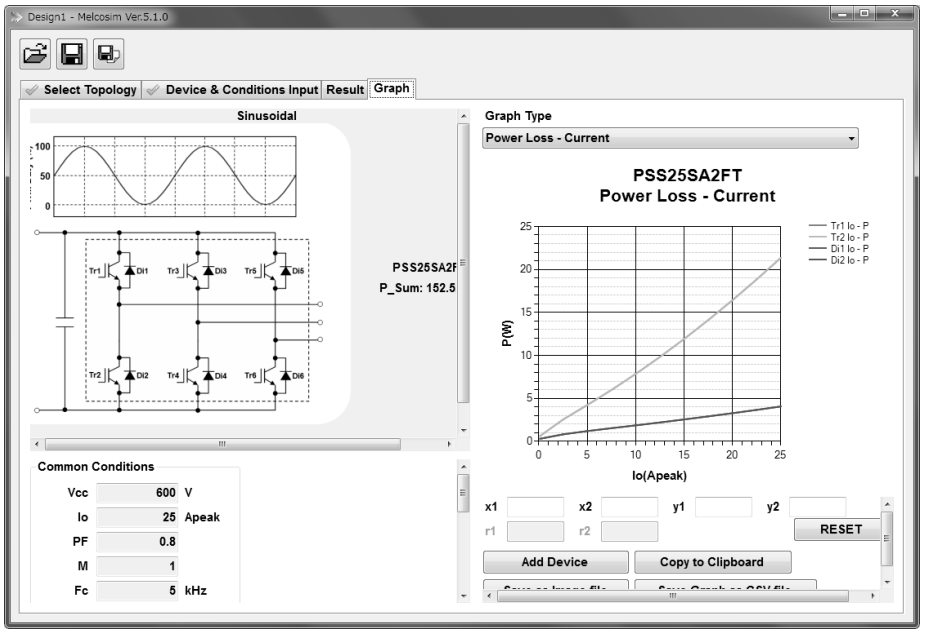


Fig.3-23 Loss simulator screen image

3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

DIPIPM have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-24. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors, an additional confirmation on prototype is necessary.

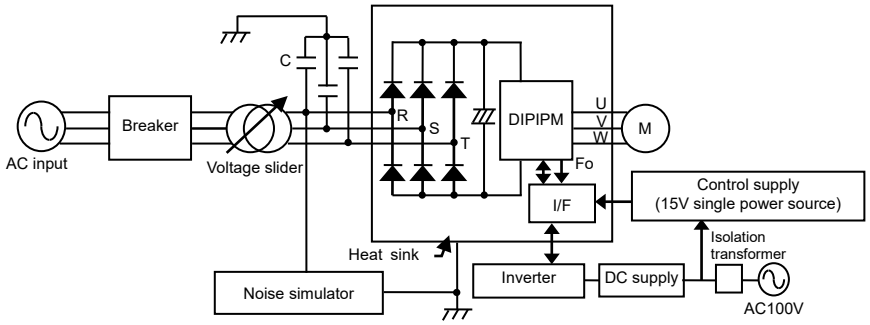


Fig.3-24 Noise withstand capability evaluation circuit

Note: C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

Test conditions

V_{CC}=600V, V_D=15V, Ta=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

3.3.2 Countermeasures and Precautions

DIPIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to no good wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, the countermeasures are recommended.

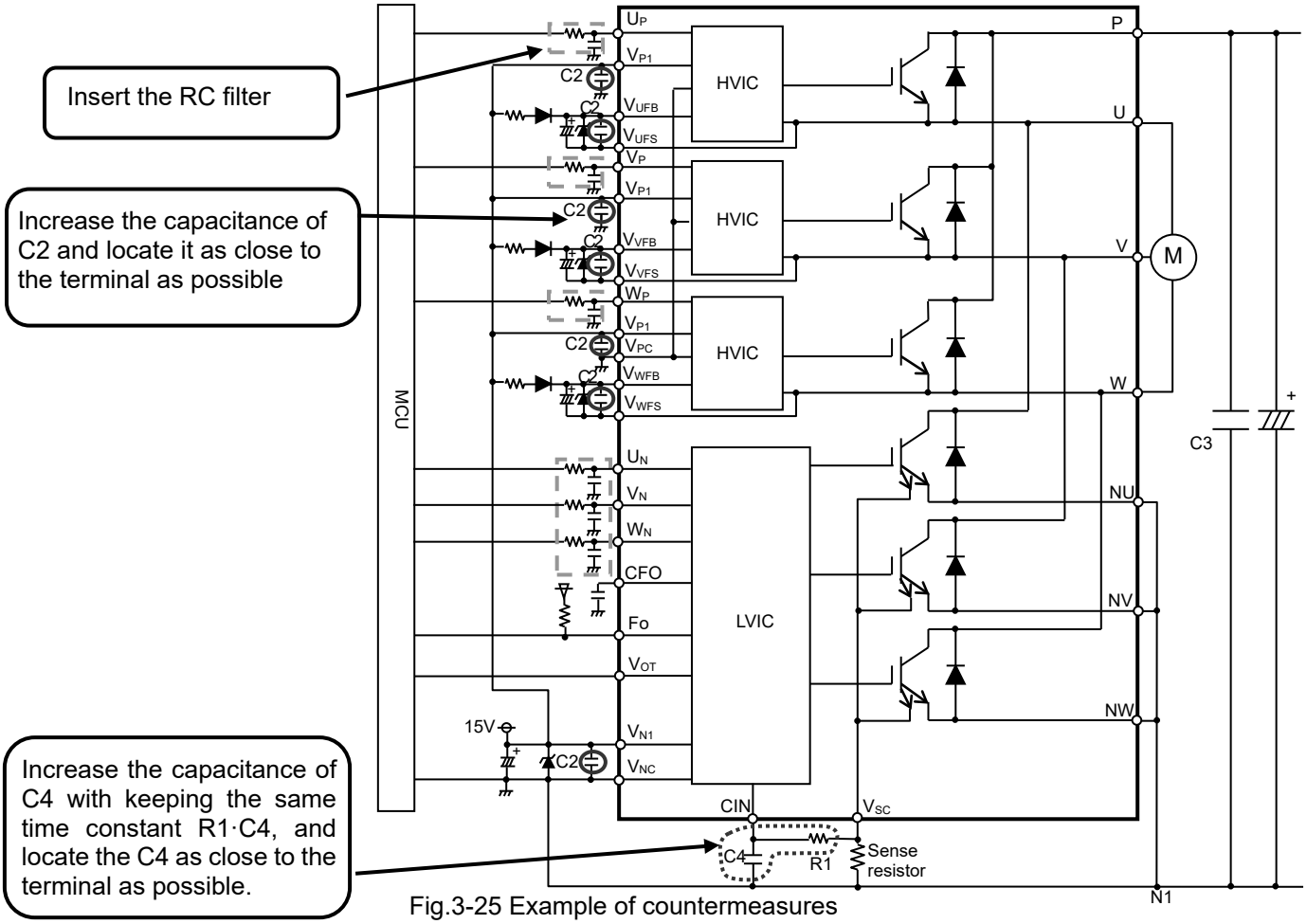


Fig.3-25 Example of countermeasures

3.3.3 Static Electricity Withstand Capability

Typical static electricity withstand capability by HBM(R=1.5kΩ, C=100pF) and MM(R=0Ω, C=200pF) are described as below.

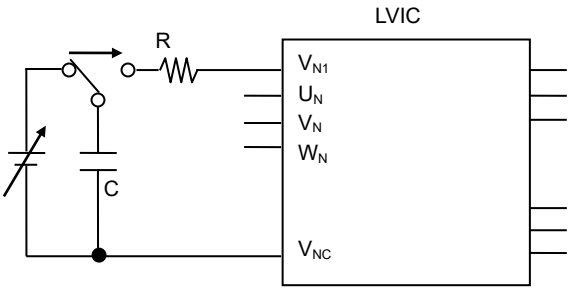


Fig.3-26 Surge test circuit example(V_{N1} terminal)

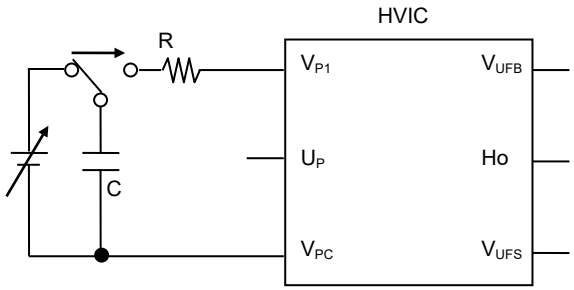


Fig.3-27 Surge test circuit example(V_{P1} terminal)

(1) Human Body Model

Conditions: Surge voltage increases by degree and three surge pulses are impressed at each surge voltage.
(Limit voltage of surge simulator: ±4.0kV, Judged by change in V-I characteristic)

Table 3-4 ESD capability (typical data)

[Control terminal part]

For control part, since all models have same interface circuit on the control IC, they have same capability.

Terminals	+	-	Unit
UP, VP, WP-V_{PC}	4.0 or more	4.0 or more	kV
V_{P1} - V_{NC}	4.0 or more	4.0 or more	
V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	4.0 or more	4.0 or more	
UN, VN, WN-V_{NC}	3.9	4.0 or more	
V_{N1}-V_{NC}	4.0 or more	4.0 or more	
CIN-V_{NC}	4.0 or more	4.0 or more	
Fo-V_{NC}	4.0 or more	4.0 or more	
CFO-V_{NC}	4.0 or more	4.0 or more	
V_{OT}-V_{NC}	4.0 or more	4.0 or more	

[Power terminal part for all models]

Terminals	+	-	Unit
V_{SC}-V_{NC}	4.0 or more	4.0 or more	kV
P-NU, NV, NW	4.0 or more	4.0 or more	
U-NU, V-NV, W-NW	4.0 or more	4.0 or more	

(2) Machine Model

Conditions: Surge voltage increases by degree and one surge pulse is impressed at each surge voltage.
(Limit voltage of surge simulator: ±4.0kV, Judged by change in V-I characteristic)

Table 3-5 ESD capability (typical data)

[Control terminal part]
For control part, since all models have same interface circuit on the control IC, they have same capability.

Terminals	+	-	Unit
UP, VP, WP-V_{PC}	1.1	1.0	kV
V_{P1} - V_{NC}	1.3	1.3	
V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	2.2	2.1	
UN, VN, WN-V_{NC}	0.6	0.5	
V_{N1}-V_{NC}	4.0 or more	4.0 or more	
CIN-V_{NC}	0.9	0.9	
Fo-V_{NC}	0.7	0.7	
CFO-V_{NC}	1.0	1.0	
V_{OT}-V_{NC}	1.1	1.1	

[Power terminal part for all models]

Terminals	+	-	Unit
V_{SC}-V_{NC}	0.7	0.7	kV
P-NU, NV, NW	4.0 or more	4.0 or more	
U-NU, V-NV, W-NW	4.0 or more	4.0 or more	

CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor.

It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC, limiting resistance and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*".

The built-in BSD characteristics of this series and the circuit current characteristics in switching situation of P-side IGBT are described as below.

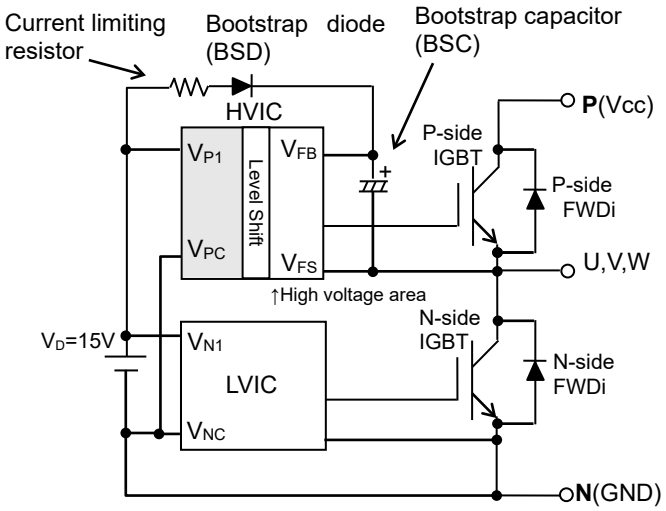


Fig.4-1 Bootstrap Circuit Diagram

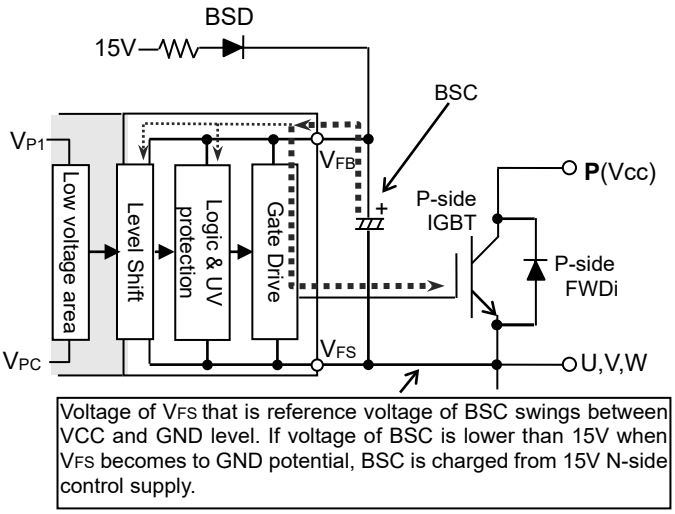


Fig.4-2 Bootstrap Circuit Diagram

4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 1.1mA for this series. But at switching state, because gate charge and discharge are repeated by switching, the circuit current will exceed 1.1mA and increases proportional to carrier frequency. For reference, Fig.4-3~4-9 show the circuit current I_{DB} for P-side IGBT driving supply - carrier frequency fc typical characteristics for each products. (Conditions: V_D=V_{DB}=15V, Tj=125℃)

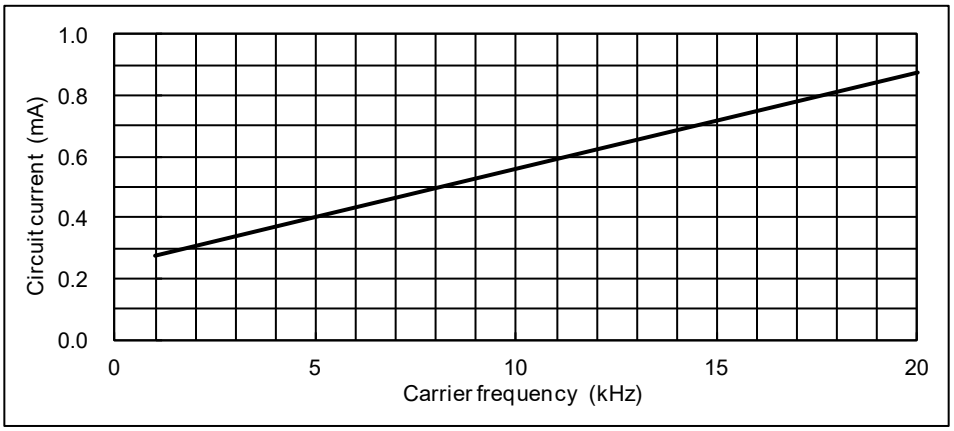


Fig.4-3 I_{DB} vs. Carrier frequency for PSS05SA2FT

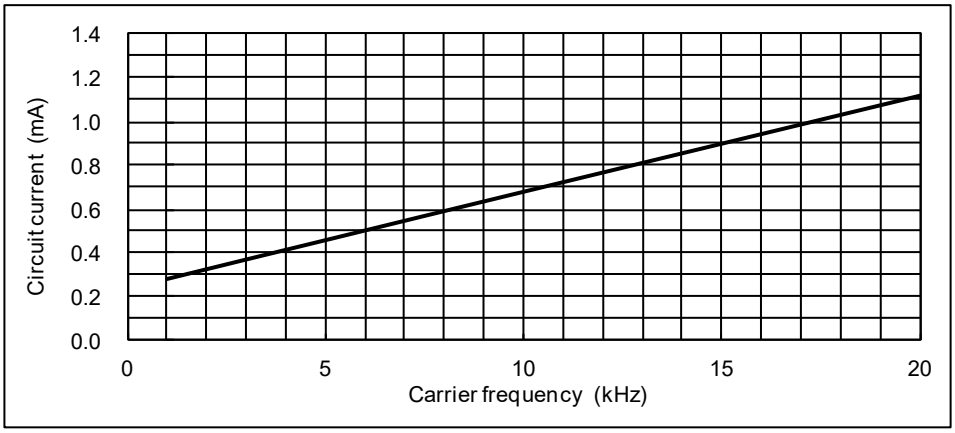


Fig.4-4 I_{DB} vs. Carrier frequency for PSS10SA2FT

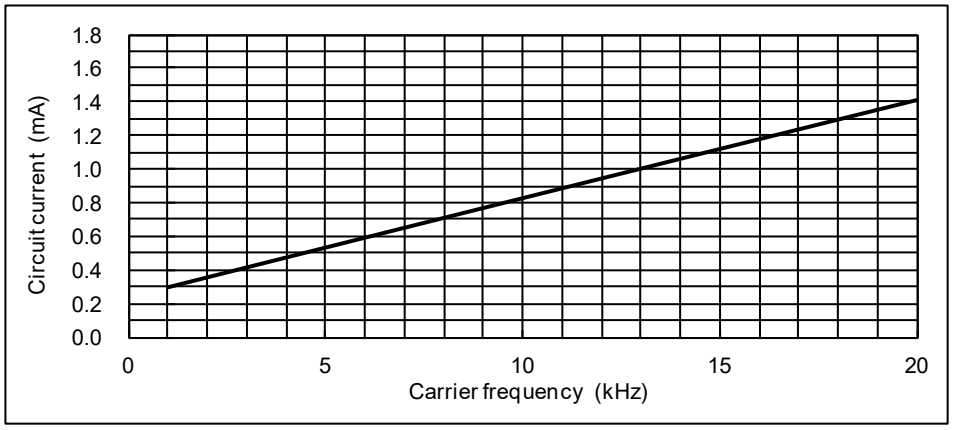


Fig.4-5 I_{DB} vs. Carrier frequency for PSS15SA2FT

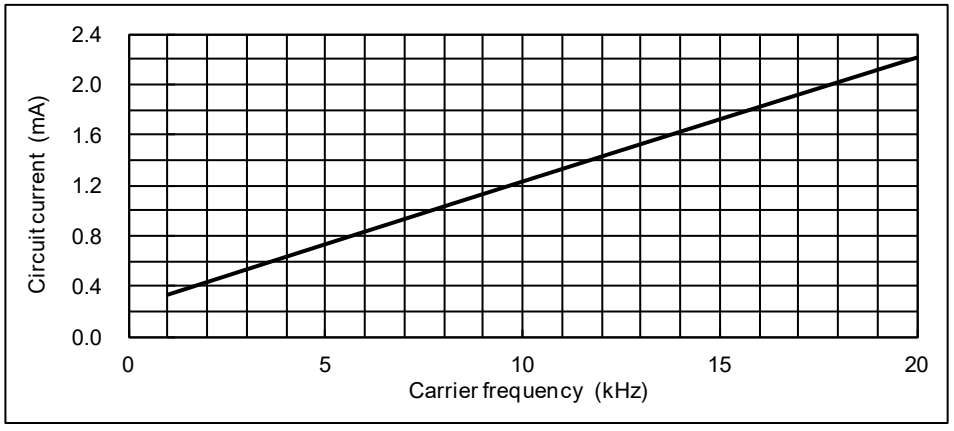


Fig.4-6 I_{DB} vs. Carrier frequency for PSS25SA2FT

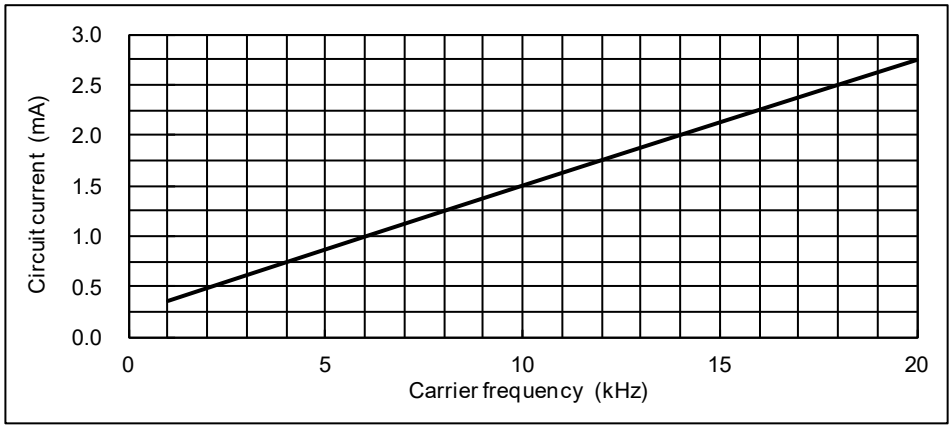


Fig.4-7 I_{DB} vs. Carrier frequency for PSS35SA2FT

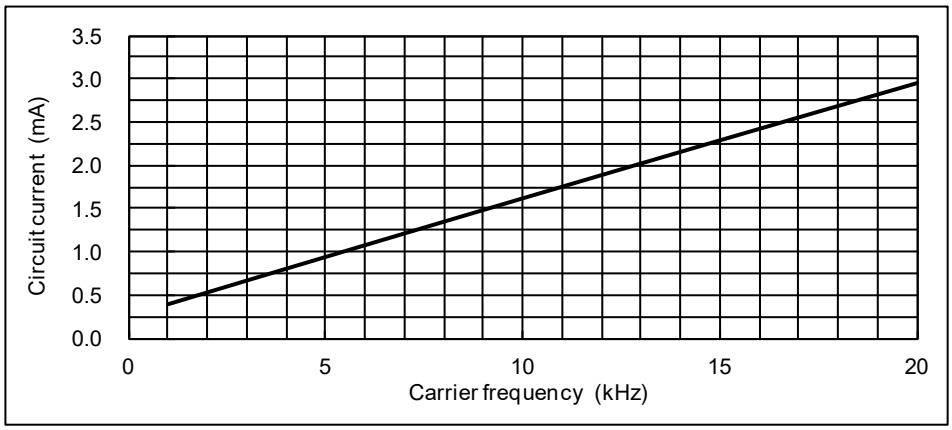


Fig.4-8 I_{DB} vs. Carrier frequency for PSS50SA2FT

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

(1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-1.

Table 4-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	• Aluminum type: Low temp.: -10% High temp: +10% • Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on **-70%**~-15%

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

This series integrate bootstrap diodes for P-side driving supply. This BSD incorporates current limiting resistor (typ. 20Ω). The V_F-I_F characteristics (including voltage drop by built-in current limiting resistor) is shown in Fig.4-10 and Table 4-2.

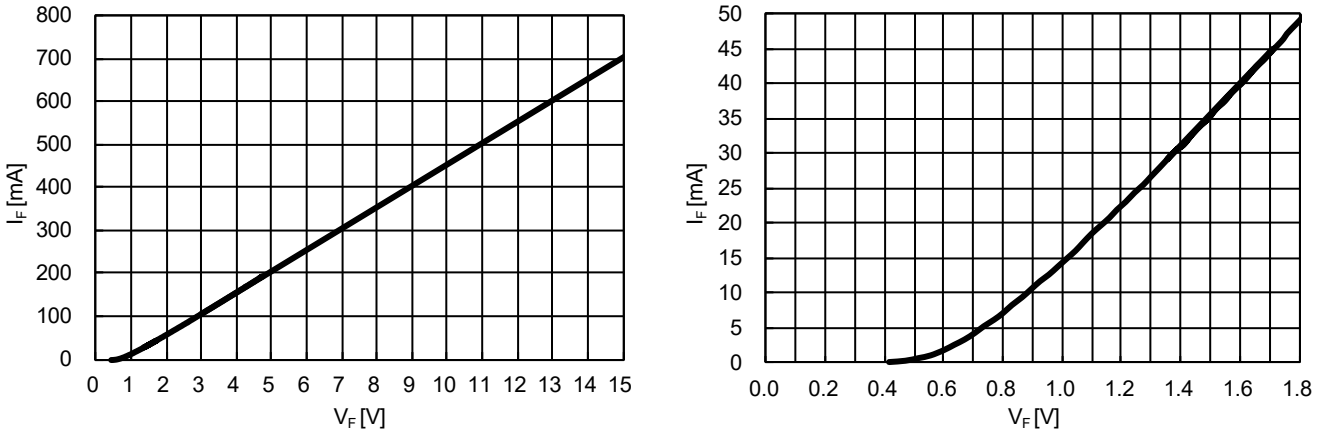


Fig.4-10 V_F-I_F curve for bootstrap Diode (The right figure is enlarged view)

Table 4-2 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	I_F=10mA including voltage drop by limiting resistor	0.5	0.9	1.3	V
Built-in limiting resistance	R	Included in bootstrap Di	16	20	24	Ω

4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIPIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and so on.

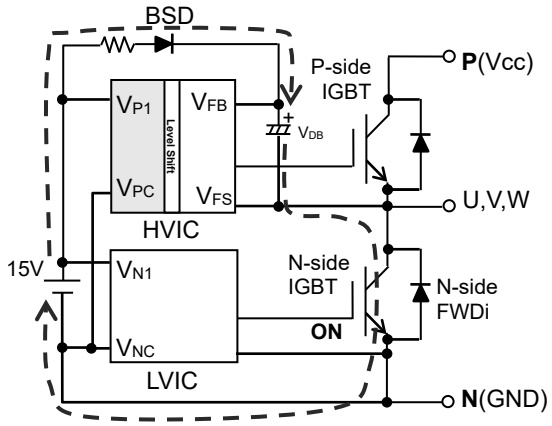


Fig.4-11 Initial charging root

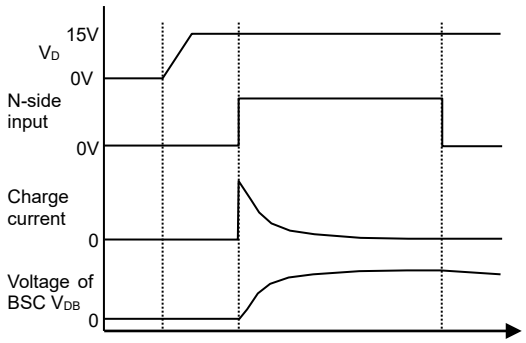


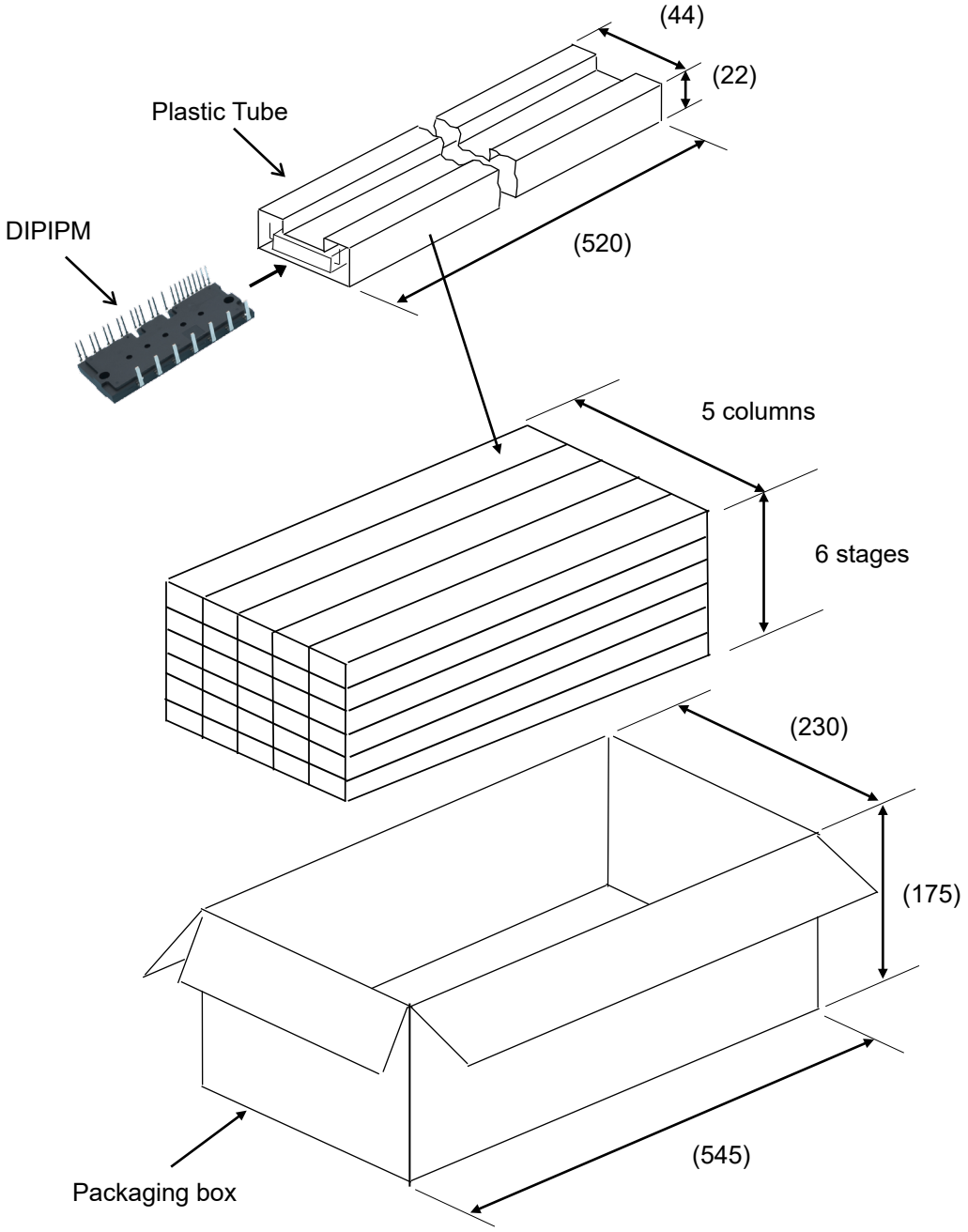
Fig.4-12 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (e.g. 1.5μs)

CHAPTER 5 PACKAGE HANDLING

5.1 Packaging Specification



Quantity:
6pcs per 1 tube

Total amount in one box (max):
Tube Quantity: 5 × 6=30pcs
IPM Quantity: 30 × 6=180pcs

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.

Weight (max):
About 46g per 1pcs
About 380g per 1tube
About 13kg per 1box

Spacers are inserted into the top and bottom of the box.
If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

5.2 Handling Precautions

⚠ Cautions	
Transportation	・Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ・Throwing or dropping the packaging boxes might cause the devices to be damaged. ・Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	・We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	・When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	・Keep modules away from places where water(including dew condensation) or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	・The epoxy resin of case material is flame-resistant type (UL standard 94V-0), but they are not noninflammable.
Anti-electrostatic Measures	・ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1) Precautions against the device destruction caused by the ESD When the ESD of human bodies, packaging and etc. are applied to terminal, it may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. *Containers that charge static electricity easily should not be used for transit and for storage. *Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. *Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands. *During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. *When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. *If using a soldering iron, earth its tip. (2)Notice when the control terminals are open *When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. *Short the terminals before taking a module off.
Anti-overvoltage Measures	・Precautions for overvoltage destruction. It should be noted that overvoltage destruction of DIPIPM might be caused by applying surges to inner chips (power chips and ICs) when surges are impressed to DIPIPM package directly or indirectly via the circuit board by surge discharging due to mis-operation on the in-circuit inspection process (e.g. plug off the connector of test board before discharging its capacitor, imperfect contact of the connector, and so on).

Important Notice

The information contained in this datasheet shall in no event be regarded as a guarantee of conditions or characteristics. This product has to be used within its specified maximum ratings, and is subject to customer's compliance with any applicable legal requirement, norms and standards.

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Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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