<Full SiC Power Module>

Industrial Full-SiC Power Module NX Type Application Note

Index

Note) Numerical values and data described in this document are provided for reference purposes only.
These values and data are not guaranteed.

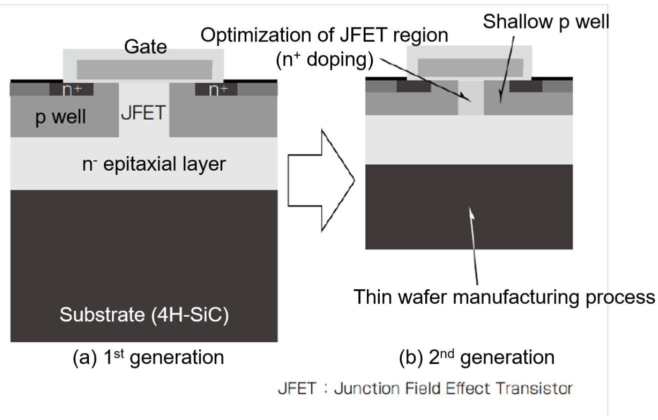
1. Introduction

1.1. Features of Industrial Full SiC Power Modules

Full SiC power modules are equipped with the latest 2nd generation SiC- MOSFET and SiC-SBD chips which have low loss characteristics that are difficult to achieve with Si devices. Mitsubishi Electric Corporation has a lineup centered on medium-capacity and large-capacity products, which contributes not only to higher efficiency and higher density of equipment, but also to miniaturization and weight reduction by simplifying peripheral parts.

Main characteristics

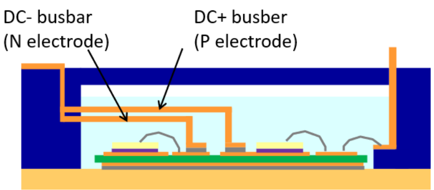
(1) Low loss characteristics and high carrier frequency driving contribute to higher efficiency, smaller size and lighter weight of equipment.
Full SiC power modules have low on-resistance characteristics due to high cell density and high concentration doping of MOSFET chips. In addition, by optimizing the structure, higher speed switching is possible and low switching loss is realized.
Full SiC power modules take advantage of low loss characteristics that are difficult to achieve with Si products, and contribute to higher efficiency, smaller size, and lighter weight of equipment.



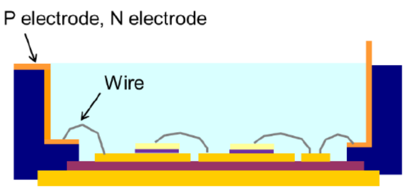
(2) The 2nd generation SiC chips achieve both high gate threshold voltage and low loss characteristics
Increasing the gate threshold voltage improves the malfunction tolerance but increases the turn-on switching loss. In the 2nd generation SiC power module, the chip structure has been optimized to achieve both malfunction capability and low loss characteristics in the used gate voltage range.

Features of NX Type

(1) Reduced package inductance for lower losses
In the NX type package used in conventional Si-IGBTs, the internal Ls≒17 nH , but the internal Ls≒9 nH was achieved by adopting the optimal internal arrangement of the chip and the internal laminate structure. By lowering the internal inductance, the surge voltage is suppressed, and even lower loss operation is possible, contributing to the higher efficiency of the equipment



Internal structure（Ls≒9nH)



Internal structure of conventional (Ls≒17nH)

(2)Product Lineup

Type name	Rated current	Rated voltage	Connection
FMF600DXE-24BN	600A	1200V	2in1
FMF600DXE-34BN	600A	1700V	2in1

Package appearance

1.2. Structure

Figure 1-1 shows the cross-sectional structure of the NX type package of the full-SiC power module (image diagram). It has a structure in which the copper base plate to the insulating substrate and the insulating substrate to the semiconductor chip are joined with solder and sealed with gel.

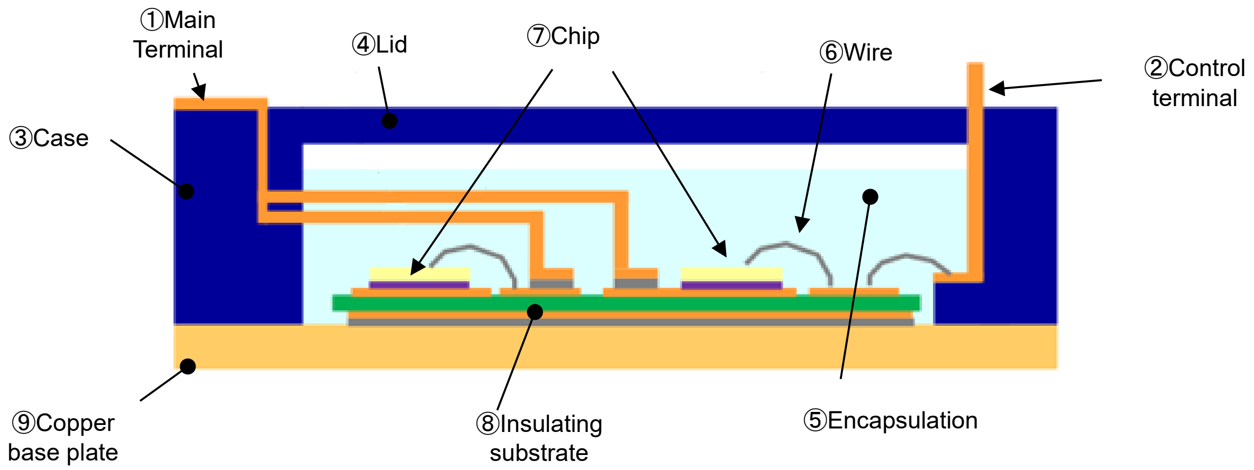


Figure 1-1. Cross-sectional structure

Table 1-1. Components

No	Parts	Material	Flame Retardance
①	Main terminal	Main material：Copper Plating：Nickel	-
②	Control terminal	Main material：Copper Plating：Nickel + Tin	-
③	Case	PPS	UL94V-0
④	Lid	PPS	UL94V-0
⑤	Encapsulation	Silicon gel	-
⑥	Wire	Aluminum	-
⑦	Chip	Silicon carbide	-
⑧	Insulated substrate	Aluminum nitride	-
⑨	Copper base plate	Copper	-

1.3. Configuration of the part number

F M F 6 0 0 D X E - 2 4 B N

Series name BN：2nd generation MOSFET only (body diode use)

Withstand voltage class（50 times the number rated V_{DSX}）
24:1200V, 34:1700V

Package outline

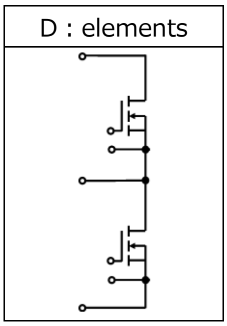
Connection
D:2in1

Current rating
600：600A

SiC element configuration
F: Full-SiC

Module type
FM : MOSFET

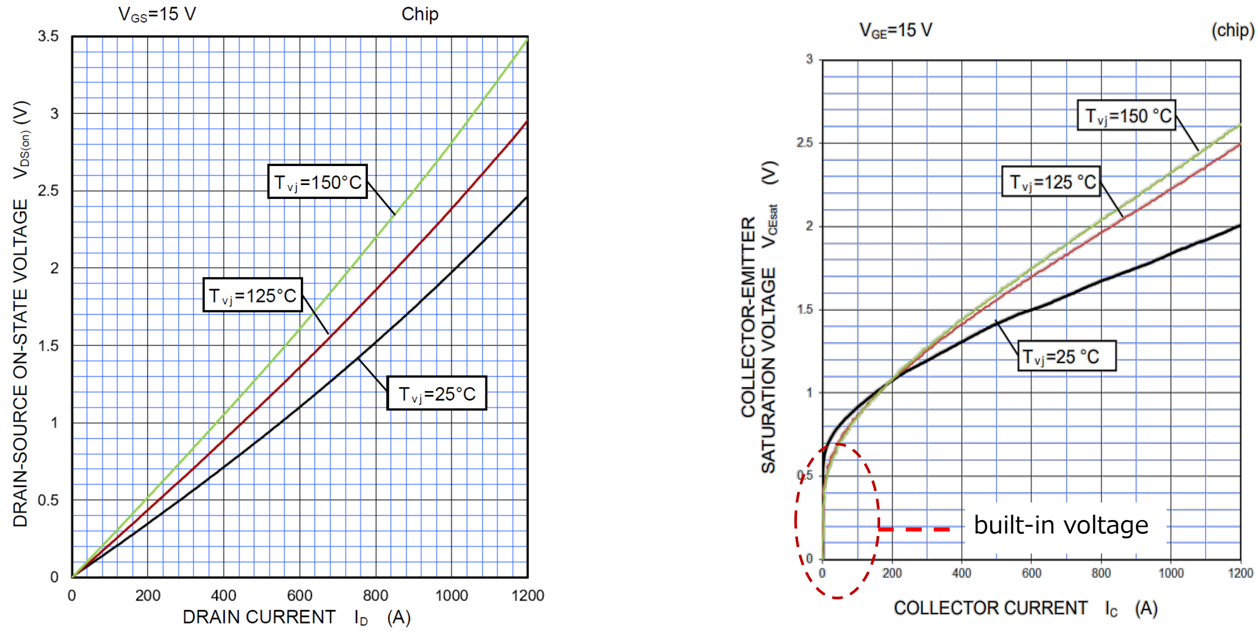
Connection



1.4. Feature of SIC-MOSFET

1.4.1 On-voltage characteristics

The on-voltage (ID-VDS) characteristics of SiC-MOSFETs are shown as below. MOSFET is unipolar devices, MOSFET do not have a built-in voltage, and current flows from the point of low on-voltage. In the low-current range, SiC-MOSFET have significantly lower on-voltage than Si-IGBT with the same rated current, and can be expected to have a loss-reducing effect by reducing DC losses. The temperature characteristics of SiC-MOSFET have a minimum value around 25°C, and the on-voltage increases with temperature changes.



SiC-MOSFET (FMF600DXE-24BN)

(b) Comparison of Si-IGBT and SiC- MOSFET（CM600DX-24T）

Figure 1-2. On-voltage characteristics

1.4.2 IS-VSD characteristics

NX-type full-SiC power modules do not have a diode chip that functions as an FWD. Reverse conduction of the MOSFET part (channel conduction) or a body diode formed inside the MOSFET chip functions as an FWD. When used as a diode, use channel conduction with as good characteristics as possible to reduce losses. However, since the body diode is energized during the dead time period, switching loss (Err) occurs when the diode is turned off. When calculating the loss, the switching loss (Err) of the diode should also be taken into consideration, different the product with SBD.

1.4.3 MOSFET reverse conduction (channel conduction)

When a gate positive bias is applied to the MOSFET, conduction is possible from the source to the drain direction through the channel section. MOSFET reverse conduction described in this section is different from MOSFET parasitic diode (body diode) energization. The current and voltage during reverse conduction of the MOS channel are proportional in the same way as when the MOSFET is forward-energized. Since the voltage between the source and drain is smaller than that of a body diode, conduction loss can be reduced by applying a positive bias to the gate during reverse conduction and conducting the MOS channel.

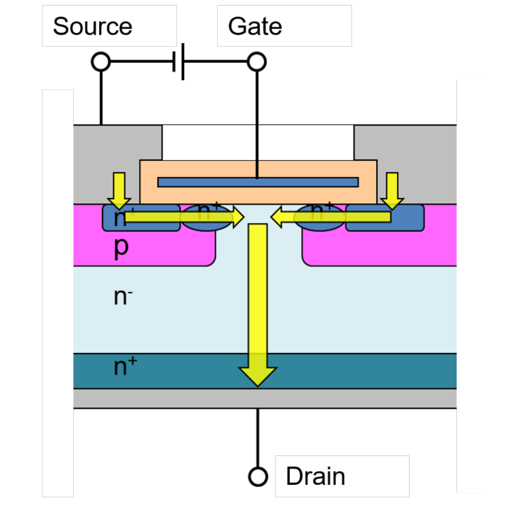


Figure 1-3. Schematic cross section of MOSFET

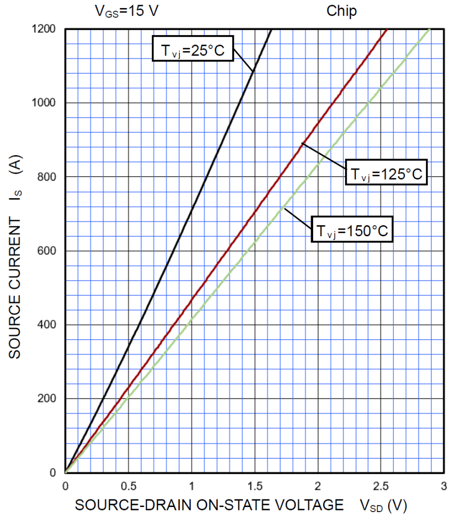


Figure 1-4. Characteristics of source-drain voltage（FMF600DXE-24BN）

MOSFET reverse conduction (body diode)

Due to the structure of the MOSFET, a pn junction is formed in the source-drain direction of the MOSFET, and this point is called the body diode. Then, it is possible to energize in the source-drain direction by applying higher voltage than the built-in potential of the pn junction. However, it has been confirmed that the on-voltage increases during energization due to the expansion of SiC crystal defects if the body diode is continuously energized. The full SiC power module is designed that the body diode is not energized by connecting a SBD diode in anti-parallel to the MOSFET.

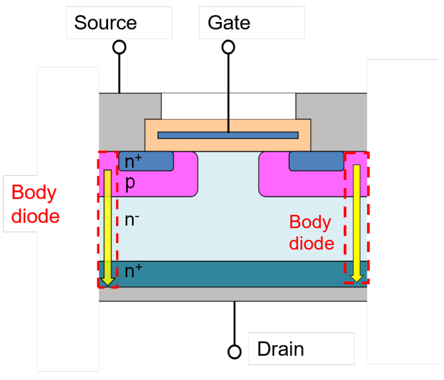


Figure 1-5. MOSFET body diode

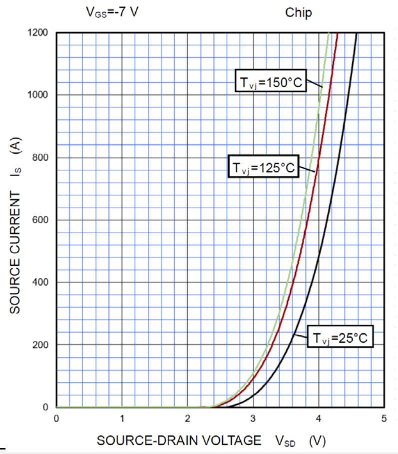


Figure 1-6. Characteristics of source-drain voltage（FMF600DXE-24BN）

1.4.4 Switching behavior

It shows the current and voltage behavior when the body diode changes from an energized state to a de-energized state. The body diode formed in the MOSFET continues to flow current (reverse recovery current) until the charge is recombined even after the diode is turned off, and it takes a certain amount of time until it reaches 0A. When calculating the loss, consider the recovery loss of the diode.

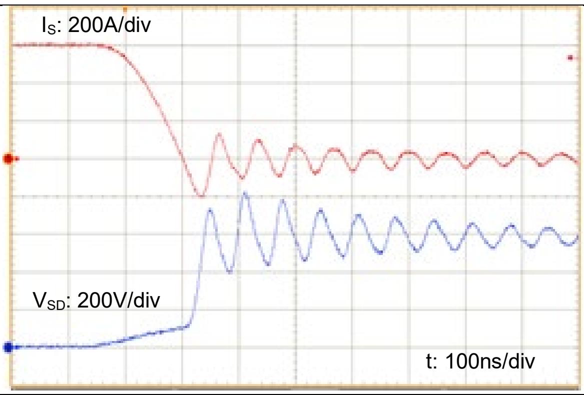


Figure 1-7. Recovery waveform
FMF600DXE-24BN T_{vj}=25℃, V_{GS}=+15V/-7V, $R_{G(on)}$=1.6Ω, $R_{G(off)}$=1.0Ω,V_{DD}=600V, I_D=600A

1.4.5 Gate-source threshold voltage

The Gate-source threshold voltage (VGS(th)) of SiC-MOSFET is lower than that of Si-IGBT products, and it is necessary to care to gate negative bias and control circuit wiring to prevent malfunction due to noise. In addition, the VGS(th) tends to decrease as the temperature increases, it is recommended to check whether there are any abnormalities during operation, including operation at high temperatures.

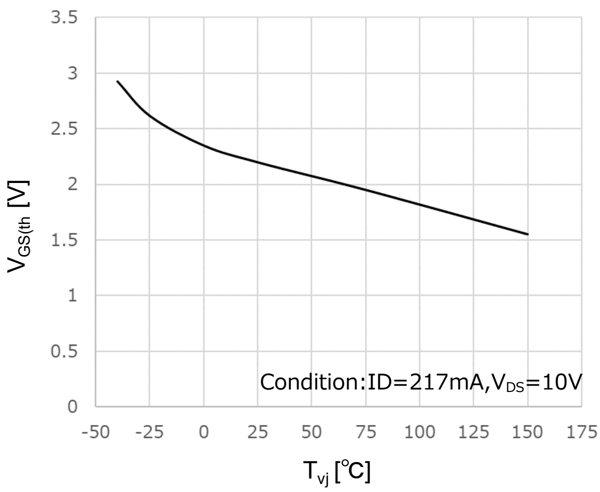
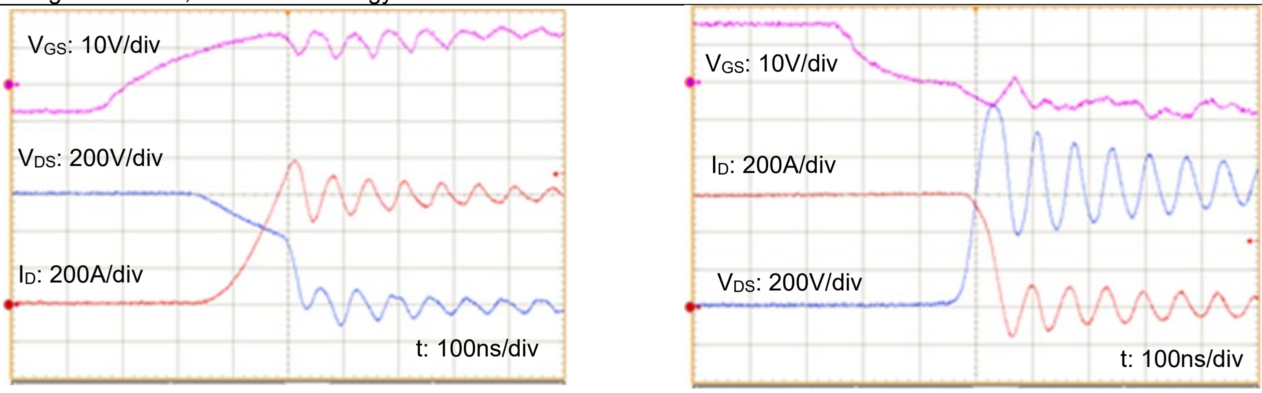


Figure1-8. Temp. dependency of VGSth（FMF600DXE-24BN）

Figure 1-9 shows the switching waveform of a full SiC power module. Since the SiC-MOSFET does not have tail current due to residual charge at turn-off, the turn-off energy is small.



(a)Turn on (b)Turn off

Figure 1-9. Switching waveform
FMF600DXE-24BN, T_{vj}=25℃, V_{GS}=±15V/-7V, $R_{G(on)}$=1.6Ω, $R_{G(off)}$ =1.0Ω, V_{DD}=600V, I_D=600A

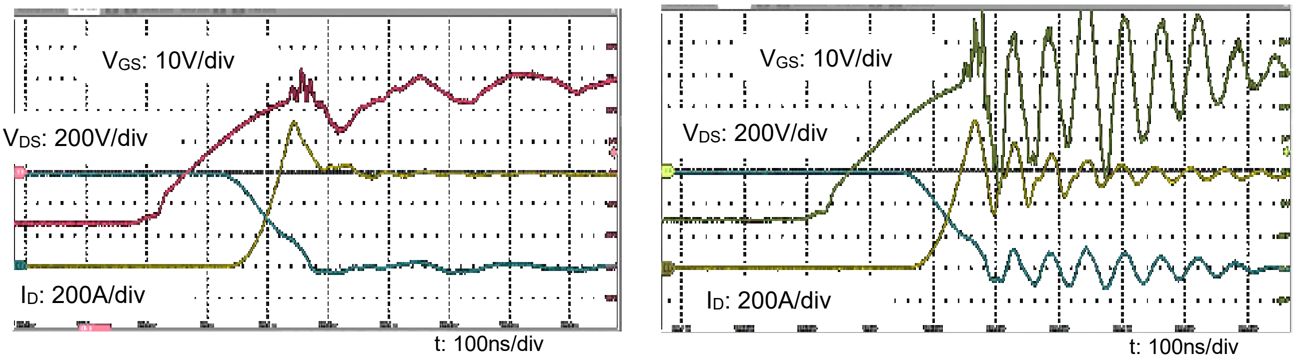
1.5 Recommended operating conditions
The recommended operating range of the NX type of full-SiC power module is as follows. For other details, please refer to each data sheet.

	V_{DD}	$V_{GS(+)}$	$V_{GS(-)}$
FMF600DXE-24BN	～850V	13.5～16.5V	-8.5～-5.5V
FMF600DXE-34BN	～1200V	13.5～16.5V	-8.5～-5.5V

1.6 Short circuit operation
The NX type full-SiC power module does not guarantee short-circuit operation.

1.7 Note of measurement

SiC-MOSFET is more possibility to pick up noise in measurements due to their fast switching speed. For example, if the ground lead of the probe is long, the noise may appear due to the inductance and the parasitic capacitance of the probe. The waveform below is an example of a waveform measured using an optical differential probe and a passive probe for a gate voltage monitor. Other D.U.T. and oscilloscopes are same. It is necessary to pay attention to the waveform that looks like the one below depending on the measuring equipment. It is necessary to divide whether it is the behavior of the actual device or the influence of the measurement equipment.

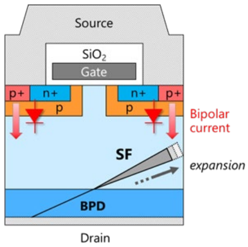


(a) optical differential probe (b) passive probe

Figure 1-10. Switching waveform

1.8 Characteristics shift

It has been widely reported that SiC-MOSFETs have a certain probability of changing their characteristics due to energization of the body diode.
This phenomenon is due to the recombination energy of the hole injected by the continuous energization of the body diode and the discontinuities that are inevitably inherent in the SiC crystal (Stacking fault), which extend the discontinuity and inhibit the conduction path, causing characteristic fluctuations (such as an increase in VDS(on)).
In the NX type full-SiC power module, we have succeeded in reducing the incidence rate to a negligible level during operation by incorporating a chip process to suppress this interaction and expansion.



Image

In general, the gate oxide lifetime depends on the TDDB(Time Dependent Dielectric Breakdown) with the applied gate voltage. In addition, a phenomenon in which VGS(th) and VDS(on) increase by continuous the gate signal on and off (switching operation) has been observed. Mitsubishi full-SiC power modules maintain the expected life of industrial equipment by improving the quality of the gate oxide , and reduce characteristic fluctuations during the operation.
Even if it is assumed to operate for 20 years (*12 hours a day), the fluctuation will be within the product standard.

The negative bias(-VGE) is necessary to prevent malfunction during switching, but pay attention to its voltage value.
Deep negative biases that over the recommended operating range can cause significant fluctuation in the device characteristics (VGS(th)). If it is used within the recommended range, the amount of characteristic fluctuation is negligible and there is no problem.

2. Glossary

2.1 Common

Symbol	Item	Description
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor	Metal-Oxide-Semiconductor Field Effect Transistor
SBD	Schottky Barrier Diode	Schottky Barrier Diode
FWD	Free Wheeling Diode	Free wheel (flywheel) diode
t_{dead}	Dead time	Pause (no signal) time provided in the ON signal between the upper and lower arm transistors
PC	Photocoupler or Optocoupler	Photocoupler or Optocoupler

2.2 Maximum Ratings

Symbol	Item	Definition or description
V_{DSX}	Drain-source voltage	Maximum voltage that can be applied for a short time between the drain and the source with the gate and source short circuited.
V_{GSS}	Gate-source voltage	Maximum voltage that can be applied for a short time between the gate and source with the drain and source short circuited.
I_D	Drain current	Maximum current that can flow continuously from the drain to the source within the rated junction temperature range.
I_{DRM}	Drain current (Maximum)	Maximum current that can be repeatedly flowed from the drain to the source in a short time within the rated junction temperature range.
I_S	Source current	Maximum current that can flow continuously from the source to the drain within the rated junction temperature range.
I_{SRM}	Source current (Maximum)	Maximum current that can be repeatedly flowed from the source to the drain in a short time within the rated junction temperature range.
P_{tot}	Total Power Dissipation	The maximum allowable power loss of the MOSFET at the specified case temperature.
V_{isol}	Insulation withstand voltage	The maximum voltage that can be applied between the terminal and the base plate in a state where the main terminal and the control terminal are collectively short-circuited. It is usually expressed as an effective value.
T_{vjmax}	Maximum junction temperature	The maximum temperature that the chip can tolerate in instantaneous operation such as overload.
T_{vjop}	Continuous operating junction temperature	Allowable temperature range of chip in continuous operation.
T_{cmax}	Maximum case temperature	Allowable maximum temperature of case.
T_{stg}	Storage temperature	The ambient temperature range when storing without power applied.

2.3 Temperature ratings

Symbol	item	Definition or description
T_a	Ambient temperature	When self-cooling or air cooling, the air temperature of a point which is not influenced by the heating element.
T_c	Case temperature	Temperature at a defined point on the enclosure (base plate) of the device.
T_s	Heat sink temperature	Temperature at a defined point on the heat sink.

2.4 Thermal ratings and characteristics

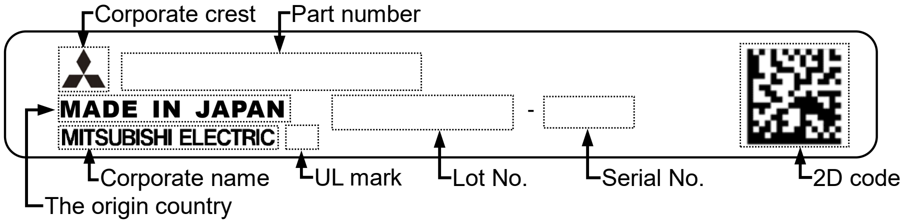
Symbol	Item	Definition or description
R_{th}	Thermal resistance	A value that indicates how many degrees K per unit electric power the junction temperature will rise over the externally specified point when heat flows due to the power dissipation of the junction in steady state.
$R_{th(j-c)}$	Thermal resistance	Thermal resistance from junction (chip) to the case (base plate) surface.
$R_{th(c-s)}$	Contact thermal resistance	Thermal resistance from the surface of the case (base plate) to the surface of the heat sink when thermal conductive grease is applied.

2.5 Electric characteristics

Symbol	Item	Definition or description
I_{DSX}	Drain-source cutoff current	The leakage current which flows upon application of a specified voltage between the drain and source while applying the specified negative bias between the gate and source.
I_{GSS}	Gate-source leakage current	The leakage current which flows upon application of a specified voltage between the gate and source while short-circuiting the drain and source.
$V_{GS(th)}$	Gate–source threshold voltage	Under specified conditions, the gate-source voltage required to supply the specified drain current.
$V_{DS(on)}$	Drain-source on voltage	Drain-source voltage when specified drain current is supplied under specified conditions.
$r_{DS(on)}$	Drain-source on resistance	Drain-source resistance when specified drain current is supplied under specified conditions.
C_{iss}	Input capacitance	Capacitance inside the device as seen from between the gate and source terminals, under the specified conditions, in a state where the drain and the source are short-circuited in an AC manner.
C_{oss}	Output capacitance	Capacitance inside the device as seen from the drain-source terminal, under the specified conditions, in a state where the gate and the source are short-circuited in an AC manner.
C_{rss}	Feedback capacitance	Capacitance inside the device as seen from between the drain and gate terminals, under the specified conditions, in a state where the drain and the source are short-circuited in an AC manner.
Q_G	Gate charge	During MOSFET switching, the electric charge which is required for charge injection into the gate.
$t_{d(on)}$	Turn-on delay time	During turn-on, the time from 0% of the gate voltage until the drain current rises to 10% of the final value.
t_r	Rise time	During turn-on, the time until the drain current rises from 10% of the final value to 90%.
$t_{d(off)}$	Turn-off delay time	During turn-off, the time from 90% of the gate voltage until the drain current falls to 90% of the initial value.
t_f	Fall time	During turn-off, the time from when the initial drain current drops to 90% until the time when it drops to 10%.
E_{on}	Turn-on energy (Turn-on loss)	The time integral value of the product of the drain current and the drain-source voltage from the moment the drain current rises to 10% of the final value at the turn-on until the drain-source voltage drops to 10% of the initial value.
E_{off}	Turn-off energy (Turn-off loss)	The time integral value of the product of the drain current and the drain-source voltage from the moment when the drain-source voltage rises to 10% of the final value at the turn-off until the drain current drops to 2% of the initial value.
E_{rr}	Reverse-Recovery energy (Recovery loss)	The time integral value of the product of the recovery current and the drain-source voltage from the moment when the recovery current 0% value at the diode recovery until the recovery current 0% .
V_{SD}	Source–drain voltage	Source-drain voltage when specified source current is supplied under specified conditions.
$R_{DD'+SS'}$	Internal wiring resistance	Wiring resistance value from chip to module terminal.
L_s	Internal inductance	Module inductance under the specified path.
r_g	Internal gate resistance	The gate resistance value installed inside the module.

3. Product Label Information

3.1 Label printing example



- This product complies with the RoHS(Note) Directive (2011/65/EU, 2015/863/EU).
  (Note) Restriction of the use of certain hazordous substances in electrical and electronic equipment.

3.2Lot number configuration

```
T 2 5 A A 1 G
| | |     |   └–– RoHS directive compliant identification mark
| | |     └–––––– Production management number
| | └–––––––––––– Production month: 1 to 9;  January to September
| |                                  O;October, N; November, D; December
| └–––––––––––––– Production year: Single-digit of the year end
└–––––––––––––––– Factory symbol (UL factory identification mark)
```

3.3 Two-dimensional barcode configuration

Two-dimensional code specifications

specification

Item	Specification
Code type	Data Matrix (ECC200)
Data type	Alphanumeric characters
Error correction capability	20 to 35%
Symbol size	6.0 mm × 6.0 mm
Code size	24 cell × 24 cell
Cell size	0.25 mm
Data capacity	39-digit

Data Example

Item	Characters count
Model	1-20
space	21-22
Lot number	23-30
space	31
Parallel specification	32-34
Space	35
Serial	36-38
space	39
total	39

Data Example

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
F	M	F	6	0	0	D	X	E	-	2	4	B	N	SP	SP	SP	SP	SP	SP	SP	SP	T	2	5	A	A	1	G	SP	SP	SP	SP	SP	SP	0	0	1	SP

"SP" represents a space (blank = equivalent to ASCII code number 32).

4. Control circuit design

The key points of designing gate driving circuit are gate resistance, gate voltage, and wiring method. Figure 4-1 shows the basic form of the gate circuit.

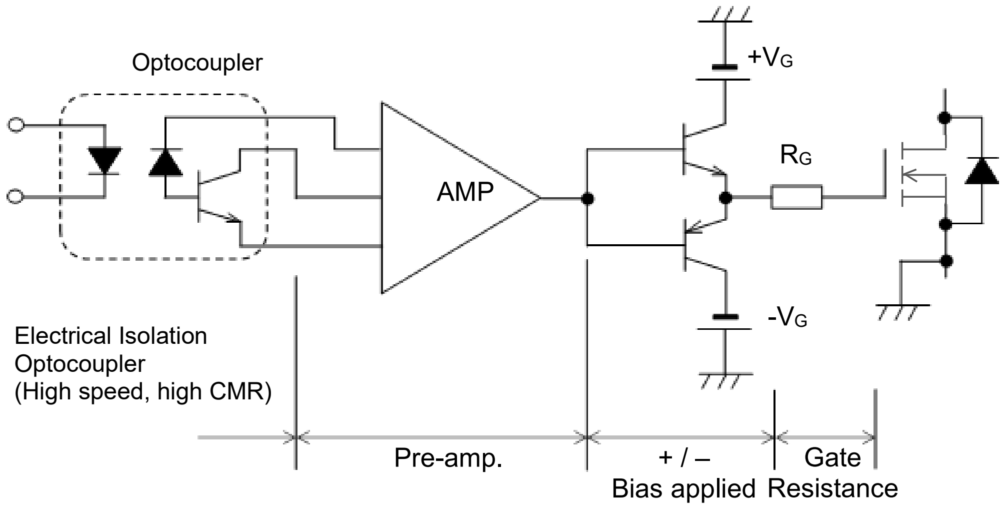


Figure 4-1. The basic form of the gate circuit

- Electrically isolate the power module and the input signal by using an optocoupler. The optocoupler must be high speed with high noise immunity (high CMR).
- Be sure to design the buffer circuit to apply the positive and negative bias so that the gate current can flow sufficiently.
- Reduce the wiring between the gate drive circuit and the power module as much as possible. Avoid noise induced from main circuit etc. by e.g. twisting pair of the gate wiring and the source wiring. Do not bind up the gate wiring with the one for the other phases.
- When the load is short-circuited, the gate-source voltage V_{GS} rises and may break down due to the larger current flowing. Therefore, it is recommended to suppress surges of the gate-source voltage. An example is shown below in Figure 4-2.
- If the voltage is applied to the main circuit before the control voltage supply becomes stable, the power module may be destroyed.
- In case the voltage is applied to the main circuit before the control voltage supply becomes stable, it is recommended to insert a resistor between the gate and the source. (Resistance value example: several kΩ to several tens of kΩ)

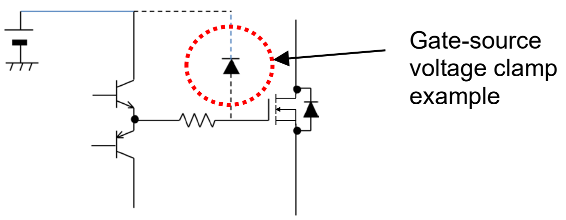


Figure 4-2. Gate-source voltage surge clamp example

4.1 Selection of gate resistance

Gate resistance (R_G) is one of the important parameters related to switching characteristics and noise. Recommended maximum and minimum values of R_G are given by the data sheet. The main items affected by the gate resistance are shown below. Optimum R_G should be selected with careful confirmation for no occurrence of any maximum rating violation (Tvj, Vces, etc.) or any unexpected malfunction (arm-shoot-through, oscillation, etc.) at the actual user system set up. Since the surge voltage will change depending on the wiring inductance of the equipment and the snubber circuit etc., the optimum value varies depending on the user. In order to maximize the device performance, it is recommended to individually set the gate resistance on turn-on side and turn-off side.

Main items affected by gate resistance

・Switching loss
・Surge voltage
・Dead time
・Noise（switching dv/dt） (etc.)

Item	Advantage	Disadvantage
Increased gate resistance（Reduced switching speed）	・Surge voltage reduction ・Noise reduction（switching dv/dt reduction）	・Increased switching loss ・Increased required dead time
Reduced gate resistance（Increased switching speed）	・Switching loss reduction ・Required dead time reduction	・Increased surge voltage ・Increased Noise (Increased switching dv/dt)

4.2 Setting of gate voltage

The gate voltage values greatly affect the switching characteristics. The Mitsubishi Electric SiC power modules herein can be driven under the same gate voltage conditions (± 15V) as a Si IGBT module. The recommended gate voltage values are 13.5V to 16.5V for positive bias and -5.5V to -8.5V for negative bias.

4.2.1 Gate positive bias

The value of the gate positive bias mainly affects the turn-on characteristics and diode characteristics. When the gate positive bias is increased ($V_{GS\,(+)}$ = 13.5V⇒16.5V), the switching speed at turn-on becomes faster and the turn-on loss decreases. On the other hand, the diode surge voltage increases and the diode switching dv/dt increases.

Table 4-1. Effect of increasing gate positive bias value

Advantage	Disadvantage
Reduced turn-on loss Reduced $V_{DS(on)}$	Increased diode surge voltage Increased diode switching dv/dt

Also, in case gate positive bias is lower than the recommended range, the V_{DS} value is expected to increase, as shown in Figure 4-3. Therefore, the power module would be failed due to over temperature in a short time due to rapid temperature rise.

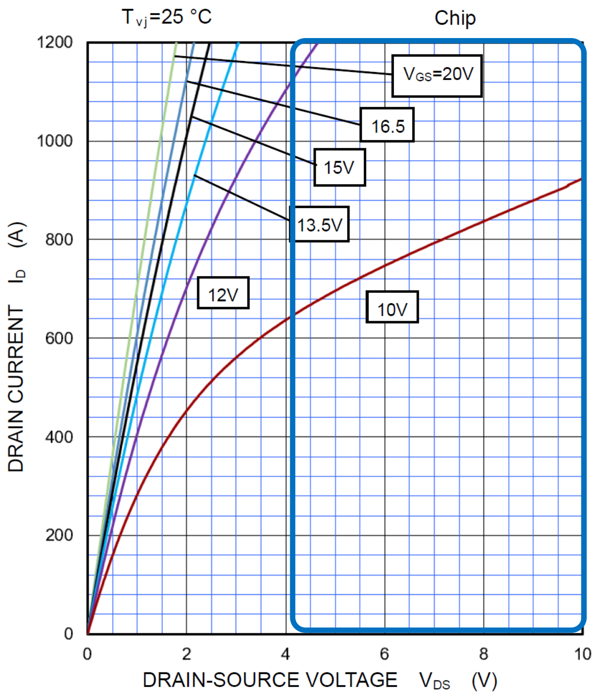


Figure 4-3. Output characteristics (FMF600DXE-24BN)

4.2.2 Gate negative bias

The larger the gate negative bias value ($V_{GS\,(-)}$ = -5.5V⇒-8.5V), the smaller the turn-on loss and turn-off loss, but the larger the surge voltage and switching dv/dt. dv/dt(max) is the value when the rate of change in drain-source voltage during switching is maximum.

Advantage	Disadvantage
Reduced turn-on, turn-off loss	Increased diode surge voltage Increased diode and switching dv/dt (turn-off)

4.3 Gate drive power supply

A gate drive power supply that can supply sufficient gate current and drive power is necessary. Figure 4-4 shows the relationship between the gate voltage and the gate current. Once the gate voltage and gate resistance R_G are determined, the gate current of the drive circuit and the required drive power are calculated as follows.

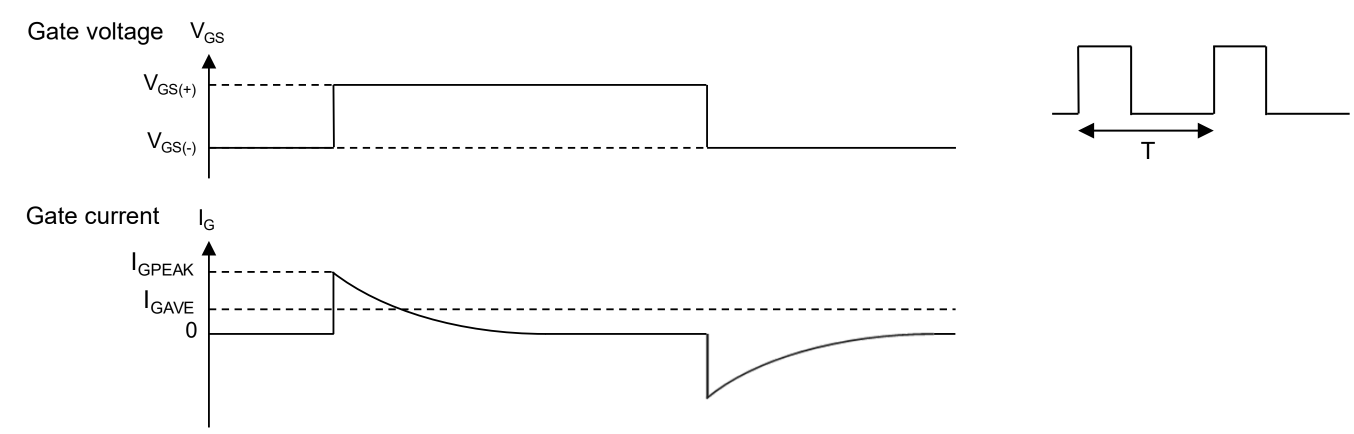


Figure 4-4. Relationship between gate voltage and gate current

(1) Average current (Excluding consumption by drive circuit)

$$I_{Gave} = Q_G\left(V_{GS(-)} \to V_{GS(+)}\right) \times f_c$$

Q_G : Gate charge amount
fc : Switching carrier frequency

(2) Peak output current

$$I_{Gpeak} = \frac{(+V_{GS})-(-V_{GS})}{R_G(External)+r_g(module\ intenal)}$$

Note) In actual practice, the peak current value may be smaller than the calculated value due to the delay of the drive circuit, the inductance of the drive wiring, etc.

(3) Average drive power

$$\frac{1}{T}\int V \bullet idt$$
$$= (+V_{GS})\frac{1}{T}\int idt + (-V_{GS})\frac{1}{T}\int idt$$
$$= (+V_{GS}) \bullet f_c \bullet Q_G + (-V_{GS}) \bullet f_c \bullet Q_G$$
$$= ((+V_{GS}) + (-V_{GS})) \bullet Q_G \bullet f_c$$

4.4 Dead time setting

In the inverter circuit etc., it is necessary to set the upper and lower arm dead time in the sequence of the drive signals in order to prevent upper and lower arm short circuit.

The required dead time depends on the switching time when the upper and lower arms turn on and turn off. Therefore, the required dead time will change depending on the gate resistance value. If the dead time is too short, upper and lower arms are short-circuited in the same phase and short-circuit current flows, so there is a possibility of thermal destruction. After testing with the actual unit, please set the dead time appropriately.

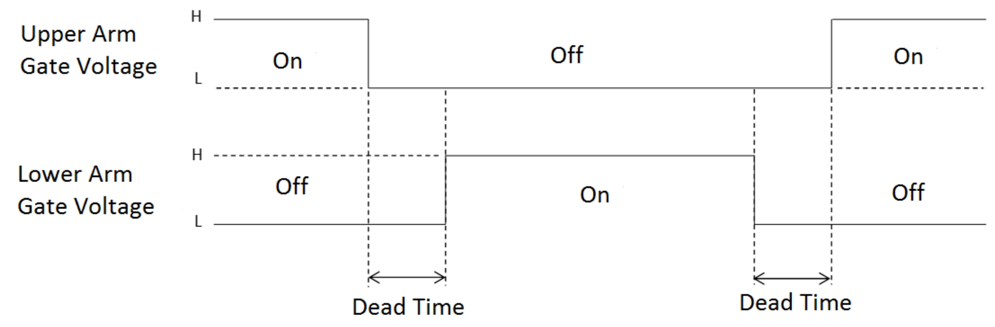


Figure 4-5. Upper and lower arm dead time

4.5 Gate driver

Some manufacturers provide the gate driver that can be applied to full SiC power modules. For inquiries about gate drivers, please contact each company directly.

■ISAHAYA ELECTRONICS CORPORATION

■Tamura Corporation

5. Power module implementation

5.1 System Layout

During switching, high voltage is induced in power circuit stray inductance by the high di/dt of the main current when the stray inductance is large. This voltage can appear on the power module and cause MOSFET or diode destruction. In order to avoid this problem, guidelines that should be followed in designing the circuit layout are:

① Reduce the L1 inductance by bringing the connection of the smoothing capacitor close to that of the module and arranging the return connection in a laminated plate structure to cancel the magnetic field.
② Connect the snubber capacitor close to the module terminal in order to bypass the high frequency current and absorb the surge voltage.
③ The smoothing capacitor itself should be of low impedance type.
④ Decrease the di/dt by slowing the switching speed of the element (increase the gate resistance, etc.).

It is a general measure to suppress the wiring inductance (L1) of the main circuit as much as possible by ① or ③, and still suppress surge voltage using ② or ④ when the surge voltage is large. Regarding ②, if the wiring inductance (L1) is large, the voltage oscillation may increase due to the resonance between C_s and L1. At that time, oscillation can be suppressed by changing the value of C_s.

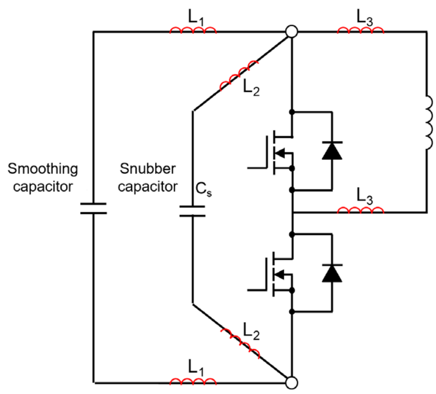


Figure 7-1. Power Module application circuit

L1: Inductance of the wiring connecting the smoothing capacitor and the power module. Since it is a round-trip line, it is necessary to use laminated conductors made of parallel flat metal plates sandwiching an insulator so that mutual magnetic fields are canceled.
L2: Inductance of the snubber capacitor lead wire. If this inductance is large, it will not be an effective bypass.
L3: Inductance of the wiring connecting the load.

5.2 Method of attaching the module to the heat sink

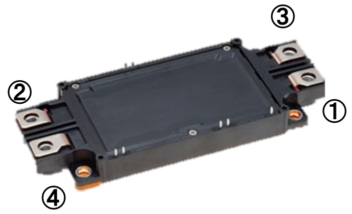
In order to suppress the temperature rise of the chips, please design for appropriate heat dissipation by attaching the power module to a heat sink. Also, it is necessary to minimize the contact thermal resistance by maximizing the contact area as much as possible in order to maximize heat dissipation.

Precautions for tightening

When attaching the module to a heat sink or similar, if extreme tightening is performed, stress will be applied to the insulating ceramic substrate or silicon carbide chip inside the module, causing destruction or deterioration of the element. An example of tightening sequence is shown in Figure 5-2.

When installing the heat sink, be careful not to allow foreign matter to get in between the power module and the heat sink. Also, please use a torque driver or torque wrench to tighten to the specified torque when tightening. Please use spring washer and flat washer. We recommend installing screws with the spring washer + flat washer built-in as shown in Figure 5-3. Depending on the viscosity of the grease used and the application method, the grease may not spread after temporary tightening and excessive stress may be applied during final tightening. Therefore, please ensure sufficient time/speed when tightening.

Please check if there are any problems under the actual tightening conditions (grease, tools, tightening order, tightening time interval, etc...).



Temporary tightening ①→②→③→④, final tightening①→②→③→④

* Temporary tightening torque should be set to 0.3N･m to 1.2N･m as a guideline

Figure 5-2. Tightening sequence

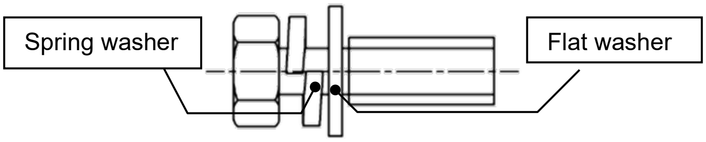


Figure 5-3. Example of Washer embedded screw (spring and flat washers)

- Please use mounting screws and washers that match the module mounting hole size. If screws with a size smaller than the recommended screw size (with flat washer) are used, there is a possibility that a misalignment of the center line of the screw occurs, a shearing force is applied to the flat washer, and the clamping force is not evenly applied to the module mounting hole. This will cause loosening of the mounting screws. An attaching method that makes axial force uniform and that the head end face of the screw can be held within the center line deviation so as to cover the whole mounting hole is ideal.
- When using iron/steel screws for module installation and screw terminal connection, the tightening torque is limited by the strength of the resin case etc. of the module body. Please note that tightening with the standard tightening torque of the iron/steel screw specified in JIS etc. may cause damage to the case.

Recommended heat sink specifications

- The flatness of the heat sink should be -50μm to +50 μm for a length of 100 mm on the module mounting surface (see Figure 5-4). Also, the surface roughness should be within 10 μm for a length of 100 mm. Sufficient flatness must be provided on the surface of the heat sink. Excessive minus (concave) warp will increase the contact thermal resistance Rth(c-s) and influence the heat dissipation of the module. Excessive plus (convex) warpage may cause stress to be applied to the inside of the module during installation, which may cause damage to the module.

Note: Please judge the decision from user’s side by deeply investigating possibility of any failure and decrease of thermal resistance performance in case recommended condition is not kept by actual usage.

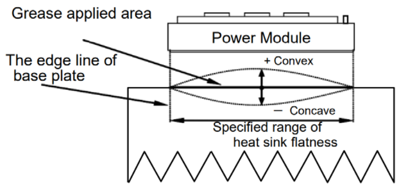


Figure 5-4. Flatness of the heat sink

Thermally conductive grease

Using thermally conductive grease is recommended to fill the gap between the power module and the heatsink.

・Please apply so that it becomes uniform with thickness of 100μm. If the grease is applied unevenly, the stress on the insulating substrate may increase and crack.
・Applying grease to the contact surface with the heat sink also helps prevent corrosion of the contact area. However, please use grease that does not deteriorate within the operating temperature range and does not change over time.
・During long-term use, changes in the thermal resistance value may occur due to changes in grease characteristics or grease removal. Please check the characteristics for long-term use under the actual usage conditions of your application. (including the increase in thermal resistance due to pumping out, etc.) If the temperature rises due to long-term use, it should be used below the maximum rating.

5.3 Thermally conductive (heat dissipating) grease application example

Method of applying the thermally conductive grease to the power module.

① Materials Required: Power module, thermally conductive grease, screen, electronic mass meter, gloves
What is called a thermal compound basically performs the same function as the thermally conductive grease. When using a highly viscous compound, thoroughly stir before spreading so that it spreads over the entire baseplate.

② The relationship between the amount and the thickness of the thermally conductive grease to be applied is as follows:

$$\text{Thickness of thermally conductive grease} = \frac{\text{amount of grease [g]}}{\text{baseplate area of module } [\text{cm}^2] \times \text{density of grease } [{}^{\text{g}}/_{\text{cm}^3}]}$$

Our recommended thermal conductivity grease thickness is 100μm.
Note, this thickness is the initial value at the time of coating, it changes depending on the flatness of the base plate and heat sink after installation.

Calculate the amount of thermal conductive grease required for the power module. Calculation example:
Mounting area 97 mm × 58 mm, for case of G-747 made by Shin-Etsu Chemical Co., Ltd. for heat conductive grease

$$100\mu\text{m} = \frac{\text{amount of grease [g]}}{12.2 \times 6.6\ [\text{cm}^2] \times 2.65\ [{}^{\text{g}}/_{\text{cm}^3}]}$$

∴ Thermally conductive grease amount ≒ 2.13 [g].

③ Measure the mass of the power module without grease applied.

④ Add the amount of thermally conductive grease calculated in ① to the base plate of the power module using an electronic mass meter. There is no specific/required method for applying the grease.

⑤ Apply the added thermal conductive grease to the entire surface of the base plate so as to be uniform. There is no particular limitation on the application method as long as the target thickness is nearly uniform over the entire surface of the baseplate of the power module.

Please be careful not to contaminate with foreign matter and bubbles when applying the grease. When coating with a roller etc., please be careful that bubbles do not get mixed in the grease. When using metal spatula, please be careful not to scratch the baseplate surface. It is possible to reduce the aging effect of the thermally conductive grease on the baseplate by not wiping off the excess grease after installing to the heatsink.

Grease for aluminum conductor connections is mainly aimed at improving the contact properties of the aluminum surface and lowering electrical contact resistance by preventing corrosion. Although there seems to be a long-term use record, it is not intended to improve the heat conduction of the contact part, so it cannot be expected to make much reduction in contact thermal resistance. If this grease is adopted, sufficient heat dissipation design/study is required.

The optimum thermal conductivity grease varies depending on the application and usage, so please directly contact the grease manufacturer at the time of selection / specification.

5.4 Installation to the main terminal

When tightening the main terminal, please tighten within the recommended tightening torque range described in the data sheet. Also, please note the screw length. If screws longer than necessary are used, it may cause resin breakage at the terminal. Please refer to the following dimensions and use the screw of the optimum length.

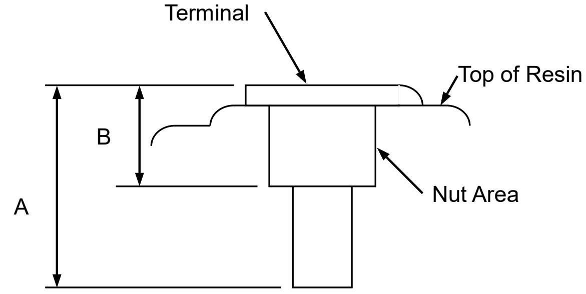


Figure 5-5. Schematic cross-sectional view of the main terminal

Terminal screw hole depth (Unit: mm, resin portion tolerance: ±0.3 mm)

Screw and size		Model	Terminal	A	B
Main terminal	M6	P, N  OUT	P, N OUT	13.5	6.5

5.5 Mounting to control terminal

Terminal specifications

Item	Specification	
Terminal material	Copper（Cu）	
Plating type	Tin（Sn）	
	Base Nickel（Ni）	
Plating thickness	Sn	4～10 μm
	Ni	1～6 μm

Recommended soldering conditions

Soldering by solder immersion (flow solder)

Solder temperature	Immersion time
260 °C±5 °C	10 sec ±1 sec

Soldering with a soldering iron (hand soldering)

Soldering iron temperature	Heating time
360 °C±10 °C	5 sec ± 1 sec

Stand-off recommended use conditions

Recommended conditions for tightening the standoff screws to attach the printed circuit board are described below.

Recommended screw

Thread type	Screw size	Tightening torque	Tightening Method
B1 tapping screw	φ2.6x10	0.75N・m±10%	1. Manual method by hand (equivalent to electric driver 30 rpm) 2. Electric screwdriver 600 rpm or less
B1 tapping screw	φ2.6x12		
PT® Screw	K25x8	0.55N・m±10%	
PT® Screw	K25x10	0.75N・m±10%	
DELTA PT® Screw	K25x8	0.55N・m±10%	
DELTA PT® Screw	K25x10	0.75N・m±10%	

※ PT® · DELTA PT® is a registered trademark of EJOT.

* 1 The above conditions are tightening conditions when printed circuit board thickness t=1.6mm.
* 2 When considering other screws or when changing tightening conditions, please separately evaluate and check the acceptability.
* 3 When using a high-speed tightening tool such as electric screwdriver, ensure it has performance that meets the recommended conditions and is regularly calibrated for both rotation speed and torque.
* 4 The standoff may only be used 1 time and is not recommended to be reused.
* 5 The above conditions may differ depending on usage environment etc. Please be sure to determine the conditions after actual evaluation.

5.6 Concept of thermal resistance

The module datasheet defines the thermal resistance $R_{th(j-c)}$ between the chip junction and case (baseplate) and the contact thermal resistance $R_{th(c-s)}$ between case (baseplate) and heat sink. The reference point of thermal resistance (case temperature) is just under the chip center. Chip placement of each product is described in the data sheet. An example of that is described below.

Tr** indicates the center position of the MOSFET chip. For 2 elements, Tr1 indicates the upper arm and Tr2 indicates the lower arm. Measure the base plate and heat sink temperature by attaching a thermocouple to the position (directly under the chip) shown in the figure.

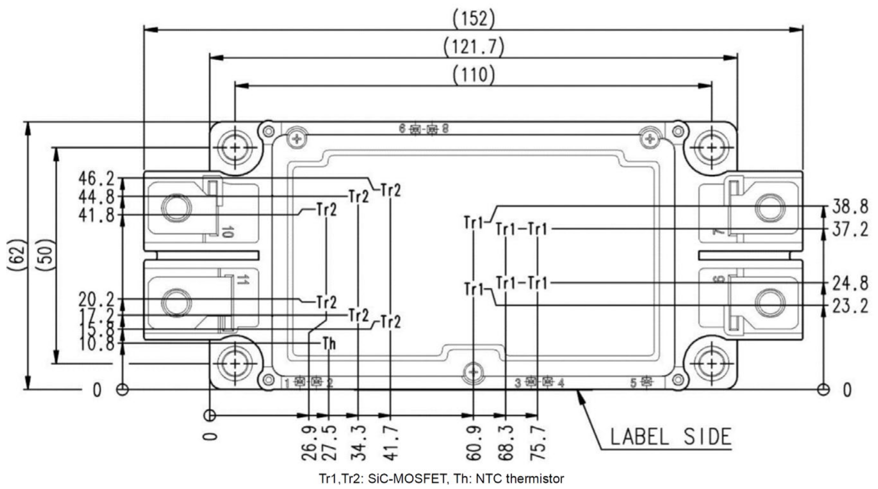


Figure 5-6. Chip location（FMF600DXE-24BN）

Notes

・ The thermal resistance of the heat sink will change depending on the material, area, and thickness used. Generally, with heat sinks of the same material, the smaller the area and the thinner the heatsink, the higher the thermal resistance.

・ The contact thermal resistance $R_{th(c-s)}$ shown in the data sheet is the typical value under noted application conditions of thermal conductive grease. The thermal conductivity conditions of the grease for the Rth(c-s) values are 0.9W/(m・K) respectively. Actual contact thermal resistance varies depending on the type of grease, the applied amount and the heat generation conditions, so confirm (measure) with the grease and heat sink used and in actual operation conditions.

・ Water-cooled heat sink:
The general industrial power module is assumed to be used in a cooling system using a natural convection heatsink or air-cooling heat sink. If you use a water-cooled heat sink, thermal resistance $R_{th(j-c)}$ and contact thermal resistance $R_{th(c-s)}$ may change significantly due to the nature of heat spreading. Further, if condensation occurs, discharge may occur between the main electrodes. Destruction caused by dew condensation is possible due to overvoltage breakdown resulting from the surge voltage generated by the discharge. Since there is no dew condensation countermeasure as part of the module, it is necessary to take dew condensation measures in the unit using the module when it is used with water cooling. The sealing material (DP resin) filled in the module has moisture permeability.

・ Packaging for general industrial power modules is not an airtight structure, so liquid can be absorbed by module. Both the package materials and semiconductor chips are not designed assuming long-term contact with any liquids. Therefore, characteristics and reliability cannot be guaranteed when the module is immersed in silicone oil or similar.

5.7 Example of thermocouple attachment

Example of thermocouple attachment for case temperature measurement just under the chip is shown below.

●Case temperature measurement
Case temperature just under chip is used for estimation of junction temperature.

Figure 5-7 shows the example of grooving from the edge of base plate to just below the chip. After checking the position just under the chip, use a milling machine to groove the base plate of the module. The depth of the groove is 1mm, the width is 1.5 mm ~ 2 mm as a guideline. The length of the groove should be about 2.0 mm longer than the thermocouple mounting hole in consideration of workability during thermocouple caulking work. After grooving, deburr the grooving surface so as not to damage the thermocouple film and heat sink.

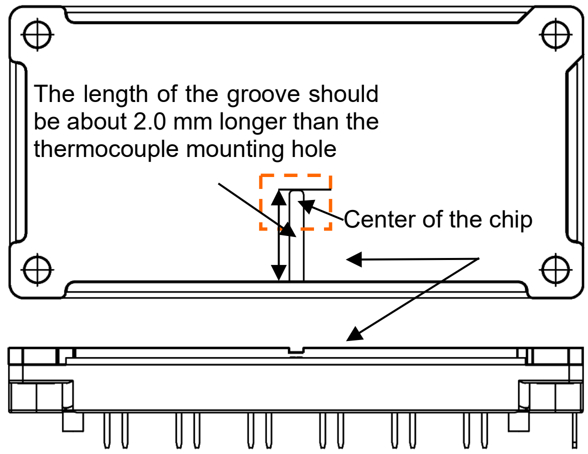


Figure 5-7. Grooving example (rear surface, side surface)

Use a drilling machine to drill a hole with hole diameter of 0.8φ and depth of 1 mm just below the tip. Figure 5-8 shows the state of the base plate after drilling.

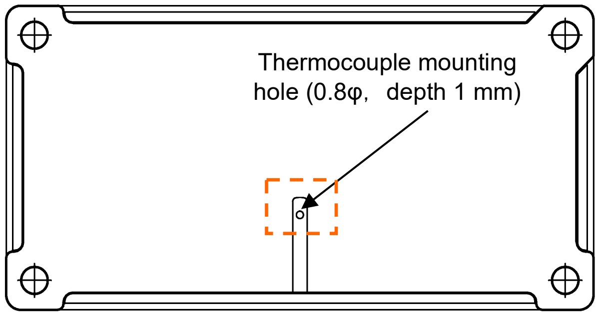


Figure 5-8. Hole drilling example (rear surface of module)

Insert the thermocouple into the mounting hole and press the thermocouple so that the tip alloy part is in proper contact with the base plate. In that state, form both ends of the mounting hole with a center punch as shown in Figure 5-9. If the tip alloy part is 1 mm or more, cut it to about 1 mm. After forming is finished, place the thermocouple in the groove to prevent the thermocouple from sticking out beyond the baseplate.

The installation of the thermocouple is completed by the above procedure. However, use a high thermal conductivity filler so that the thermocouple in the groove does not protrude and is not cut or pinched at the time of installation to the heat sink.

After applying grease, mount the module on the heat sink based on the module mounting method. After installing the module, connect the thermocouple to a temperature measuring instrument (multimeter, logger, etc.) and check that the display on the measuring instrument does not fluctuate. If the thermocouple is installed properly, the display on the measuring instrument will be stable.

In contrast, if the temperature display of the measuring instrument fluctuates, it is possible that the contact between the tip alloy part and the base plate is poor or the thermocouple is broken, so check the mounting status again.

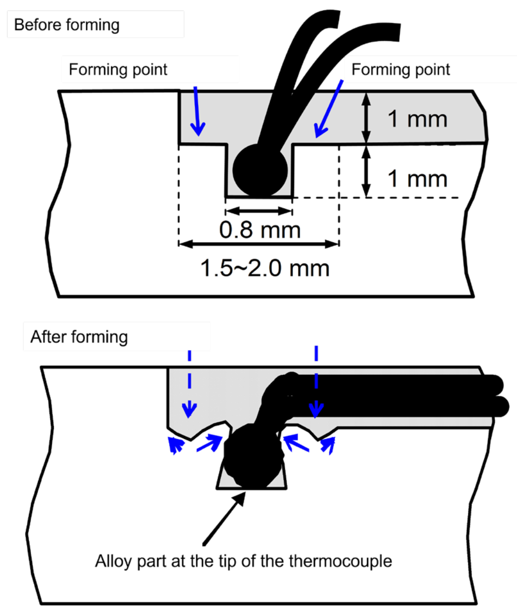


Figure 5-9. Example of thermocouple attachment

●Heatsink temperature measurement

<Step 1>
Drill into the heat sink as shown in Figure 5-10.
(The depth of the groove is 1mm, the width is 1mm as a guideline when a thermocouple with a wire diameter of 0.3mm (recommended value) is used.
Please be careful that the base of the thermocouple tip (blue line) comes to the point you want to measure (just under the chip).

<Step 2>
Insert a thermocouple into the groove drilled in Step 1, place it on the heat sink, and seal it with a high thermal conductivity filler from the top so that the thermocouple does not move. It is not a problem even if the thermocouple is caulked to the heat sink.

Figure 5-11 shows an example of groove processed on a heat sink.
Be careful not to impact the flatness of the heat sink by burrs and filling materials after the groove processing.

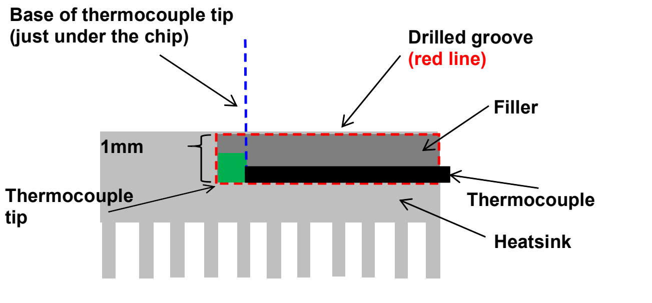


Figure 5-10. Example of heatsink thermocouple mounting

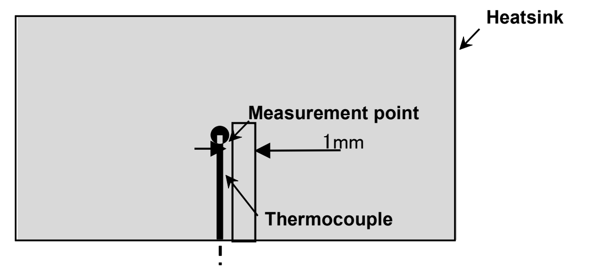


Figure 5-11. Grooving example (heatsink)

6. How to use industrial full SiC Power modules

6.1 Power module selection

6.1.1 Voltage rating

The voltage rating of the power module is determined by the input supply voltage of the applicable device or the bus voltage applied between P and N of the module. Generally, Table 6-1 shows the input power supply voltage, bus voltage, and rating of module.

Table 6-1. Application example of input power supply voltage and device rating

Voltage	Voltage rating of the power module	
	1200V	1700V
Input supply voltage (AC)	～480Vrms	～690Vrms
P-N bus voltage (DC)	～850V	～1200V

6.1.2Current rating

It is the current value that can flow as DC current. For switching operation (pulse), up to twice the rated current can be tolerated. Also, in actual use, it is necessary to consider junction temperature, case temperature, lifetime (lifetime of power cycle, thermal cycle etc) etc.

6.2 Surge voltage suppression method

Surge voltage is generated by the wiring inductance of main circuit (L) inside or outside the module and the switching speed (di / dt) of the module. In addition, surge voltage is generated when switching elements and diodes are turned off.

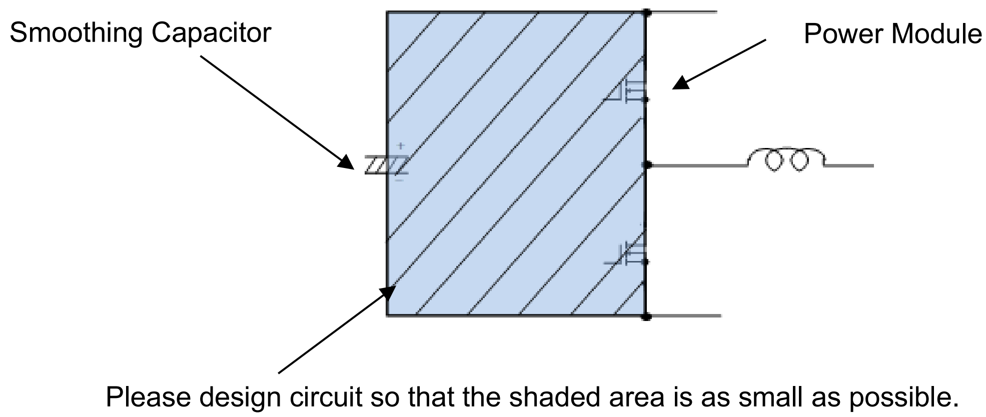
Surge voltage : $\Delta V = di/dt \times L$

Since the SiC power module uses MOSFETs and the switching speed is faster than that of Si products, higher surge voltage is likely to be generated. Therefore, we recommend the following as the method for suppressing surge voltage.

- Suppressing the wiring inductance of the main circuit as much as possible.
- Inserting snubber circuit.
- Reducing the wiring inductance of snubber circuit.
- Inserting overvoltage protection circuit.
- Slowing the switching speed of the element (increase the gate resistance, insert capacitor between gate and source etc.).

6.2.1 Reduction of main circuit wiring

In order to reduce the main circuit wiring inductance (L1) that exists in the connection path between the smoothing capacitor and the power module, please design circuit so that the area of the closed circuit formed in the shaded area below is as small as possible. One example of reducing inductance of the main circuit is to use a parallel plate with an insulating plate sandwiched between two DC bus conductors.

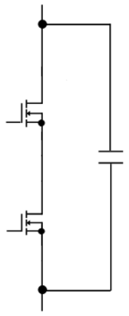
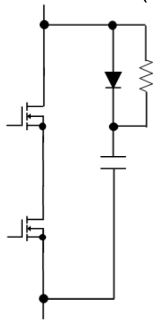
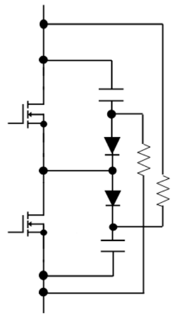


6.2.2 Snubber circuit

Please connect the snubber circuit to the nearest module P and N terminals and make the wiring inductance between the snubber circuit and the terminals as small as possible. If the distance between the snubber circuit and the terminals (P, N) is long, the effect will not be obtained.

There are different types of snubber circuits as shown in Table 6-2. Select an appropriate circuit after actual evaluation based on the characteristics of each circuit method.

Table 6-2. Example of snubber circuit

	C snubber	RCD snubber (1)	RCD snubber (2)
Circuit			
Advantage	This is simplest circuit.	This is relatively simply circuit.	It has surge suppression effects and has small snubber loss.
Disadvantage	The voltage oscillates due to the resonance of the inductance of the main circuit and the snubber capacitor.	Since the snubber circuit wiring is long, the surge suppression effect is low.	This circuit is expensive

6.3 Parallel operation

It is possible to obtain higher output current beyond the rated current of the power module as a system by connecting power modules in parallel. The following sub-sections outline the basic requirements and considerations for parallel operation.

$V_{DS(on)}$ characteristics of the full SiC power modules have a positive temperature coefficient. Positive temperature coefficient is the property where the resistance value increases as the temperature rise. When the junction temperature of MOSFET rises, the $V_{DS(on)}$ increases and the drain current reduces accordingly. Even when the current value to one element is large during parallel connection, the current imbalance between parallel connections is suppressed by the rise in chip temperature. Therefore, full SiC power modules can easily operate in parallel.

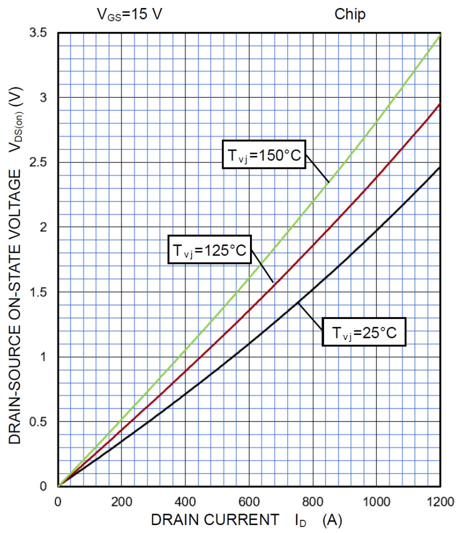


Figure 6-1. $V_{DS(on)}$ vs. I_D characteristics (FMF600DXE-24BN)

6.3.1 Current derating

In the case of connecting power modules in parallel, the current tends to flow to the element with a small $V_{DS\,(on)}$ and the current balance is lost if there is a variation in the $V_{DS\,(on)}$ of each element. The current imbalance rate at this time is called the current unbalance rate.

One example of current imbalance rate calculation is as shown below:

<Condition>

Total output current of two parallel devices: 600 A
Current value of element A: 330A
Current value of element B: 270A
Average current value of element A and B: 300A

<Example>

(330A -300A) ÷300A×100=＋10%
(270A -300A) ÷300A×100=－10%

It is important to combine products so that $\Delta V_{DS\,(on)}$ is small, because the current imbalance rate decreases as the difference in $V_{DS\,(on)}$ ($\Delta V_{DS\,(on)}$) decreases. Therefore, we recommend combining modules from the same product lot. Matching $V_{DS(on)}$ is effective for maintaining good static steady state current balance, but it has no effect on switching current balance.

As the number of modules connected in parallel increases, there is a possibility for any one single module to experience a high collector current. When modules are paralleled, calculate the derating current with formula shown below:

$$\left\{1-\frac{(n-1)\times\frac{1-x}{1+x}+1}{n}\right\}\times 100\%$$

Where n: number of paralleled modules
x: ratio of static current imbalance

Figure 8-3 shows the relationship between the number of paralleled modules and the derating rate when the current imbalance rate is 15%.

When the maximum current value of one module is 600A, 3 paralleled, and the current imbalance rate is 15%, the total current value after derating is as follows:

600A × 3 parallel × (1-0.174) = 1486.8A

Please check the current imbalance in the actual device before determining the derating rate because simple calculation cannot be done due to current imbalance.

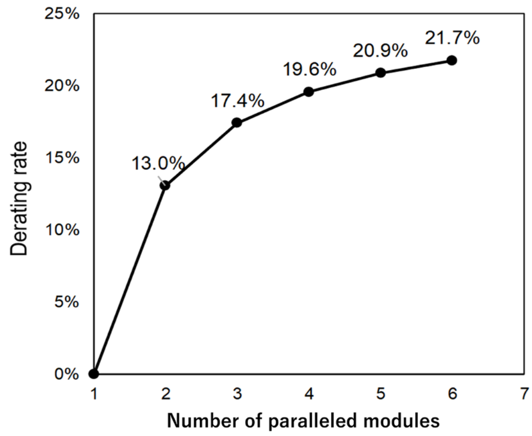


Figure 6-2. Relationship between the number of paralleled modules and the derating rate (Current imbalance rate is 15%)

6.3.2 Main circuit wiring

Main circuit wiring affects both static and dynamic current balance. The precautions for main circuit wiring when connecting power modules in parallel are shown below.

● Circuit connections should be low inductance and laid out symmetrically for balanced inductance.
Difference in the circuit inductance between each device may result in current imbalance.
Asymmetrically high power loss may occur on one particular device and cause thermal destruction.

● Use snubber circuit for each module individually and reduce circuit inductance in order to minimize surge voltage.

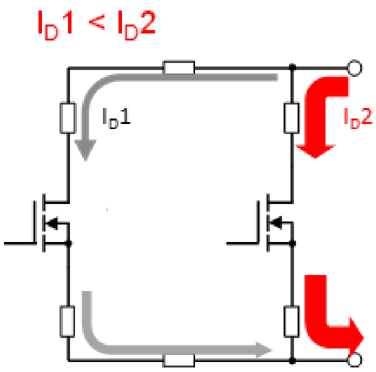
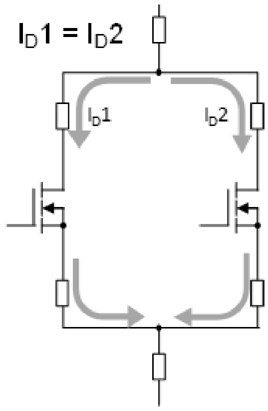
<Example of Imbalanced current> Collector current through each device has a large deviation due to an imbalance in the circuit inductance between devices.	<Example of balanced current> Collector current flows symmetrically due to balanced circuit inductance between devices.
	

Figure 6-3. Current imbalance caused by an asymmetric main circuit inductance

6.3.3 Gate drive circuit

The precautions for gate drive circuit when connecting power modules in parallel are shown below.

- Uniform impedance of each gate drive circuit. In case the difference in the impedance consisting of gate resistance and stray inductance is high, current imbalance may occur.
- Use short and tightly-twisted wires of equal length.
- Gate resistance should not be too high.
- Avoid running the wiring of drive circuit in parallel to main circuit.
- Use gate resistor for each device individually to prevent gate oscillation. (Figure 8-5)
- Insert a low value resistance (e.g. 0.1Ω) or ferrite core in the emitter wiring of the gate drivers in case an inductive current flows in the loop of the main emitter wiring and the gate driver wiring. This loop current may cause a difference in the switching speeds between paralleled devices by influencing the instantaneous gate voltage. (Figure 8-6)

<Example of Imbalanced current>
Only a single gate resistor is employed to connect the gates of the paralleled devices.

<Example of Current balance>
Use gate resistors for each device individually to prevent gate oscillations

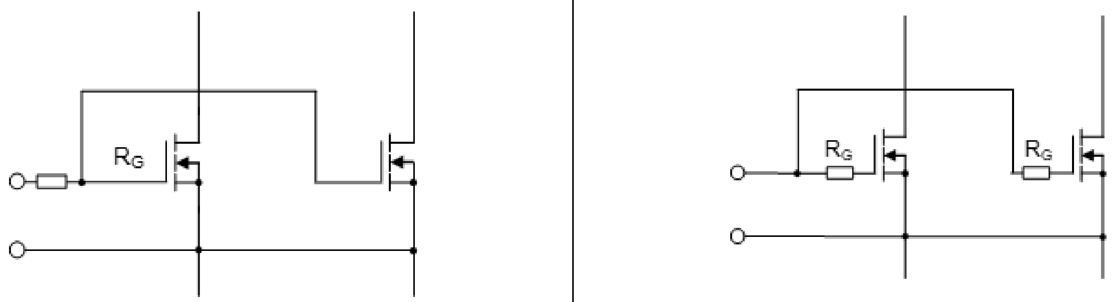


Figure 6-4. Measures to limit gate oscillation

<Example of Imbalanced current>
Inductive current flows through the drive circuit via source connection due to a difference in the value of the inductances Ls1 and Ls2.

<Example of Current balance>
Insert resistors (Rs =0.1ohm) or ferrite core in emitter wiring of the gate drive circuit to limit the inductive current flow.

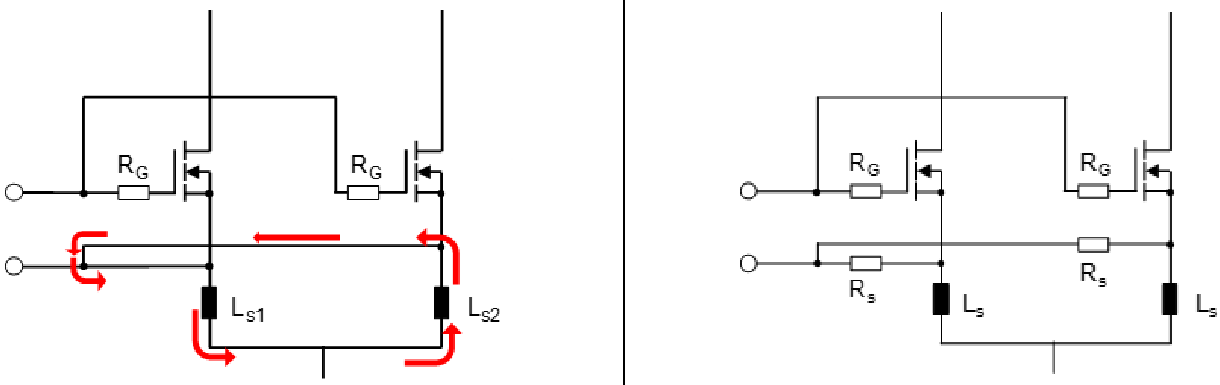


Figure 6-5. Measures to limit inductive current in emitter wiring

7. Power loss and heat dissipation design

Loss calculation of the power module

In order to use the power module safely, it is necessary to calculate the power loss and the junction temperature under the conditions to be used, and to use the module within the absolute ratings.

Power loss and junction temperature

It is very important to understand the junction temperature when using the power module. How to obtain the junction temperature is explained by taking the waveform of Figure 7-1 as an example. The calculation of the MOSFET part is shown below as an example. Regarding the temperature rise, please be careful not only to the maximum rating, but also to the power cycle lifetime due to temperature swing.

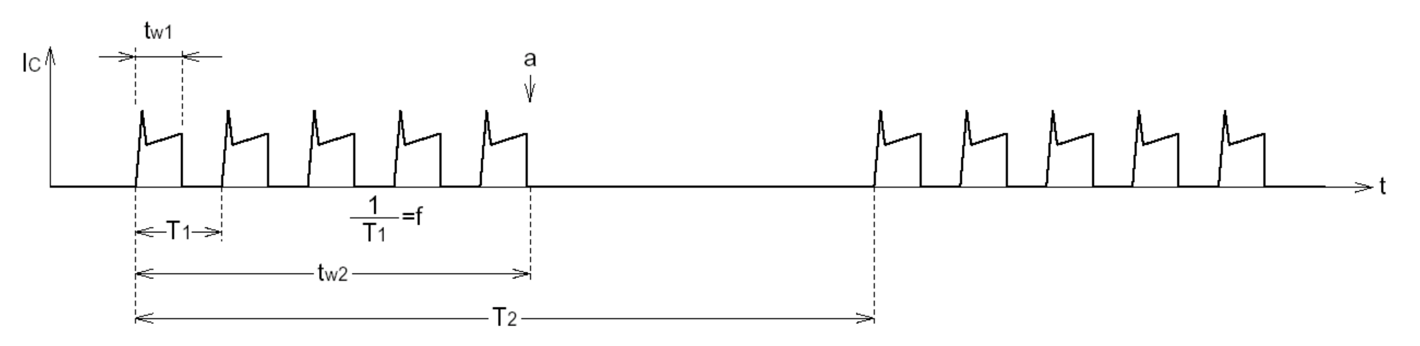


Figure 7-1. Determination of the junction temperature

7.1 Power loss

To determine the junction temperature, the user will need to know the losses of the power module. The loss per pulse should be first determined. The loss of one pulse is divided into steady-state and switching losses. Figure 7-2 shows a schematic diagram of the current-voltage waveform of one pulse and the loss generated. The integrated value of current and voltage is the generated loss. In Figure 7-2, $E_{(sat)}$ is the steady-state loss, and E_{on} and E_{off} are the switching loss.

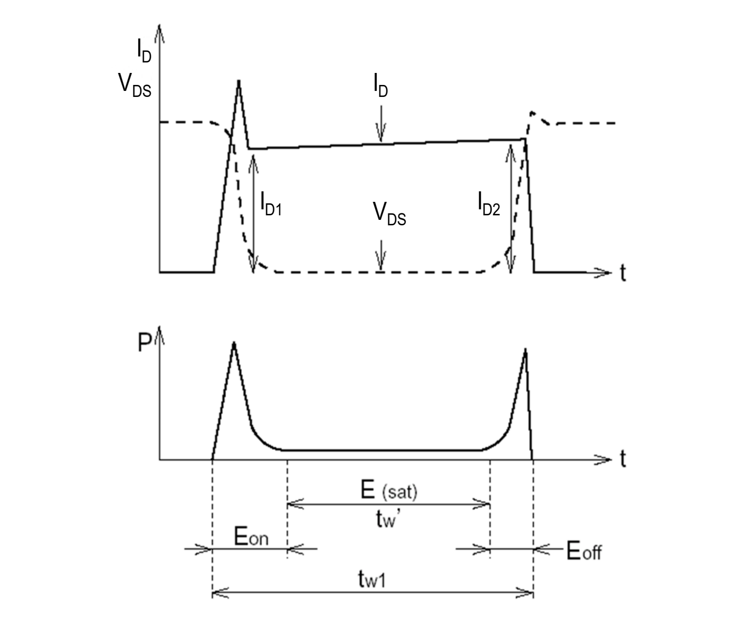


Figure 7-2. Steady-state Loss and Switching Loss

7.1.1 Steady-state loss

(a) Forward conduction (drain-source direction energization)

When energized in the forward direction, current flows through the MOSFET chip. Using a graph of $V_{DS(on)}$ vs. I_D characteristics at Tvj = 150℃, calculate the energy. The formula for calculating steady-state loss is as follows:

$$E_{sat} = \frac{I_{D1} \times V_{DS} + I_{D2} \times V_{DS}}{2} \times t_{w\prime}$$

Note) The above expression is simplified. Originally described as:

$$E_{sat} = \int_0^{t_{w\prime}} I_D(t) \cdot V_{DS(on)}(t)\mathrm{dt}$$

(b) Reverse conduction (source-drain direction energization)

When energizing from the source to the drain, the energization mode changes according to the gate voltage at the time of energization as shown in figure 7-3.

If negative bias is applied to the gate during reverse conduction, current will flow only through the body diode. On the other hand, when positive bias is applied to the gate, current flows through the MOSFET reverse conduction (channel conduction). This section describes how to calculate the steady-state loss in each energization mode.

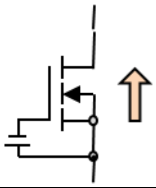
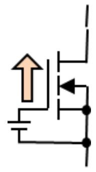
 Body diode conduction	Channel conduction 
(a)Applied negative bias to the gate.	(b)Applied positive bias to the gate

Figure 7-3. Reverse conduction energization mode according to gate voltage

Applied negative bias to the gate (Current flows in MOSFETs body diode part)

The steady loss of body diode can be calculated by the same method as in (a) Forward conduction described above. Using a graph of V_{SD} vs. I_S characteristics, calculate the energy.

Applied positive bias to the gate (Current flows in MOSFETs channel part)

It is necessary to calculate the loss separately for Body diode and MOSFET.

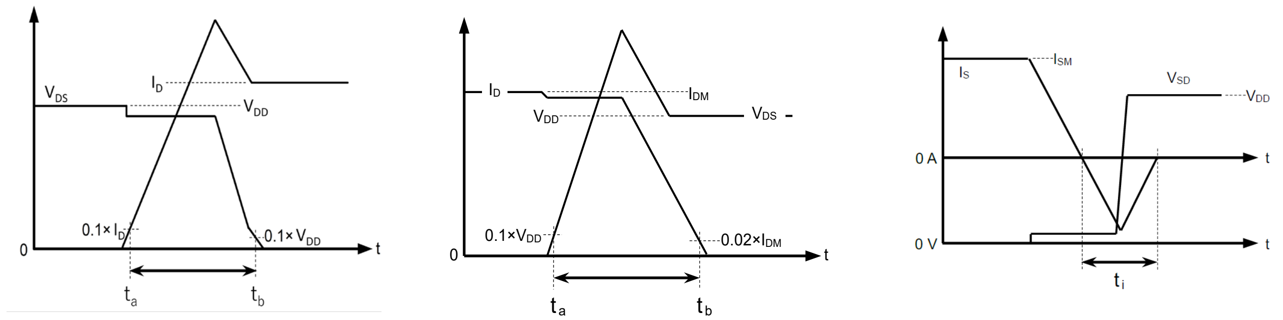
①Obtain the V_{SD} corresponding to the energization current I_S from the I_S vs. V_{SD} characteristics when the positive bias is applied to the gate.
②Obtain the energization amount I_S of the Body diode and MOSFET corresponding to the obtained V_{SD}.
③Using the obtained V_{SD} and I_S, calculate the conduction loss of each Body diode and MOSFET in the same way as in (a) Forward conduction described above.

7.1.2 Switching loss

The switching loss is obtained from the actual waveform by the piecewise quadrature. Refer to the integration range of switching loss as follows.

$$E_{on}\ or\ E_{off}\ or\ E_{rr} = \int_{t_a}^{t_b} I_D(t) \cdot V_{DS}(t)\mathrm{dt} = \frac{1}{n}\sum_{n-1}^{n} P_n \times (t_b - t_a)$$

n : number of divisions
(Equally divide the section of t_a - t_b, averaging the power loss for each point)



(a)Turn on (b)Turn off (c)Recovery

Figure 7-4. Integration range of switching loss

7.1.3 Average power loss.

When the loss of a MOSFET per pulse is E1, $E_1 = E_{sat} + E_{on} + E_{off}$

The average power loss in one pulse is

$$P_1 = \frac{E_1}{t_{w1}} \quad \text{(W)}$$

If the waveform in Figure 7-4 is approximated as a rectangular wave with respect to power, it is represented as shown in Figure 7-5.

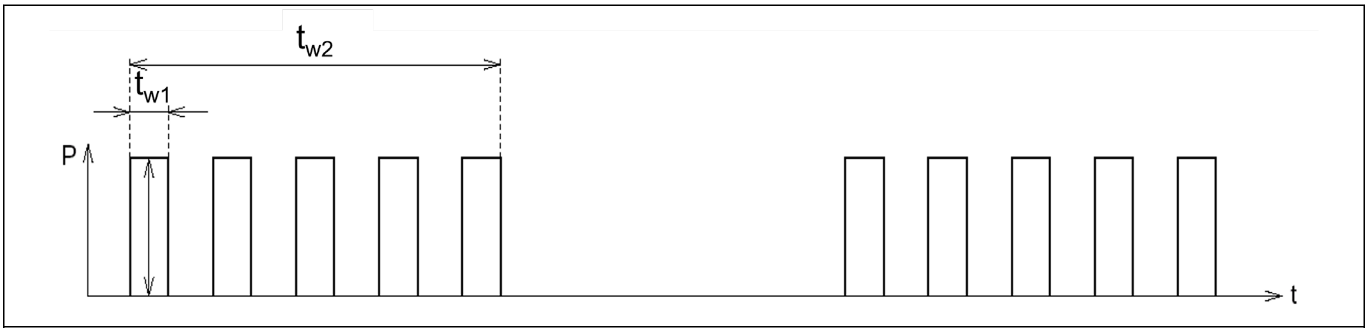


Figure 7-5. Concept of Average Power Loss 1

Calculate the average power loss in the period t_{w2}. (See Figure 7-6)

$$P_{av} = \frac{E_1}{t_{w2}} \times N \quad \text{(W)}$$

N: number of pulses within the t_{w2} period

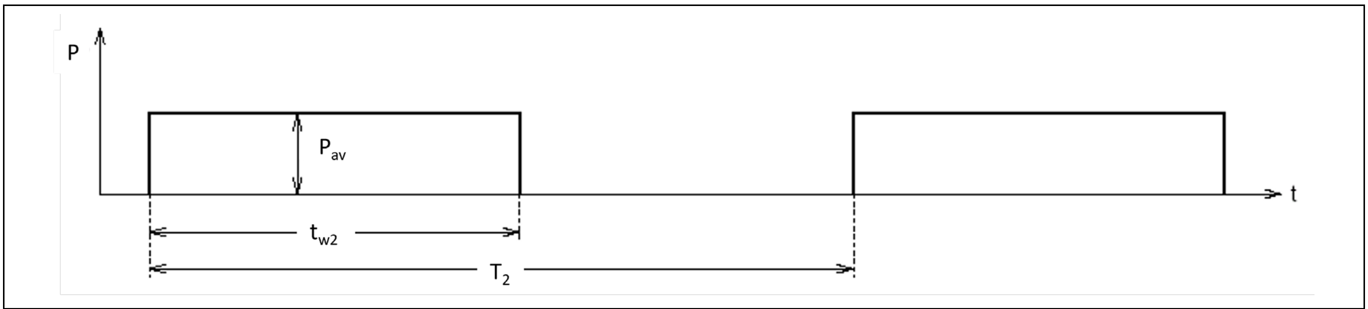


Figure 7-6. Concept of Average Power Loss 2

Calculate the overall average power loss. (See Figure 7-7)

$$P_{AV} = P_{av} \times \frac{t_{w2}}{T_2} \quad \text{(W)}$$

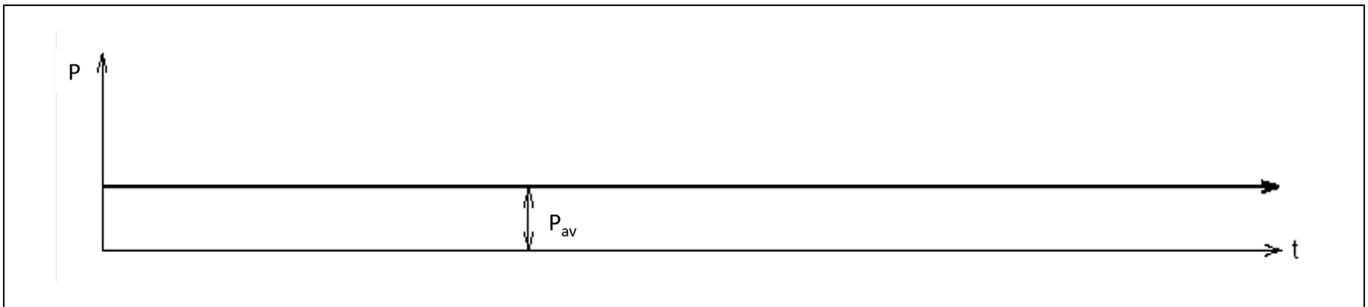


Figure 7-7. Concept of Average Power Loss 3

7.1.4 Calculation of temperature rise

Calculate the junction temperature using P_1, P_{av}, P_{AV} obtained above.

(1) t_{w1} << 1ms

In the approximation in Figure 7-8, the junction temperature is highest when the case temperature (or heat sink temperature) reaches steady state and the time when t_{w2} expires. (See Figure. 7-9)

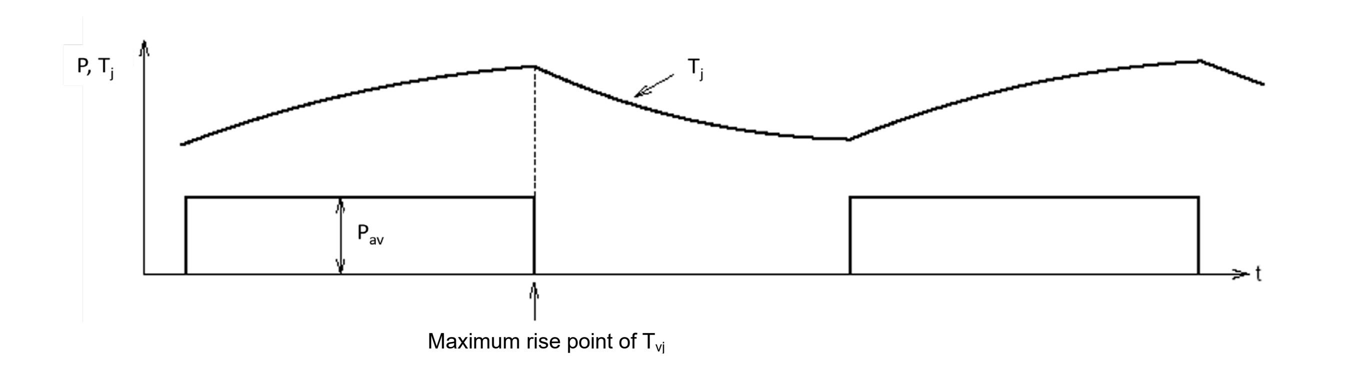


Figure 7-8. Concept of the junction temperature 1

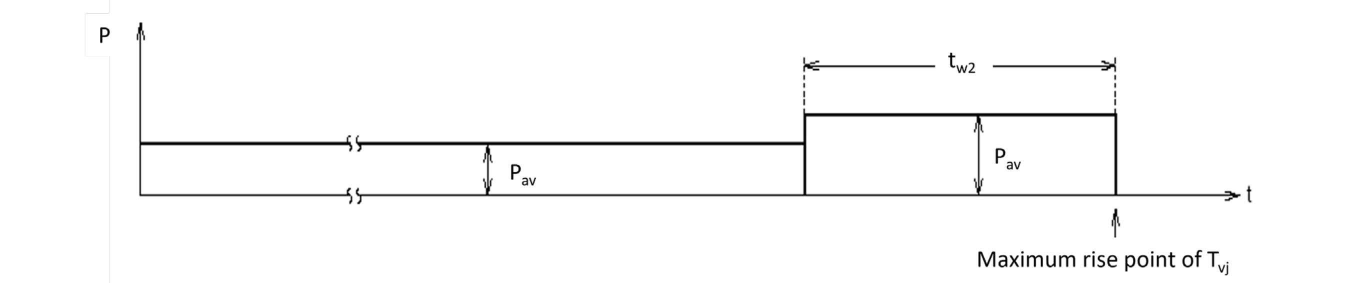


Figure 7-9. Concept of junction temperature 2

Assuming that the temperature difference between the junction and case is $\Delta T_{(j-c)}$

$$\Delta T_{(j-c)} = R_{th(j-c)} \times j_{AV} - Z_{th(j-c)}@t_{w2} \times 2_{AV} + Z_{th(j-c)}@t_{w2} \times P_{av} = R_{th(j-c)} \times j_{AV} + (P_{av} - P_{AV}) \times Z_{th(j-c)}@t_{w2}$$

$R_{th(j-c)}$ ……Thermal resistance between junction and case

$Z_{th(j-c)}@t_{w2}$ ……Transient thermal impedance at the time of t_{w2} between junction and case

Using the above calculated ΔT(j-c), the junction temperature can be calculated as

$T_{vj} = T_c + \Delta T_{(j-c)}$ (Here Tc is measurement value at the position of just under chip by e.g. thermocouple)

Also, in order to keep the T_{vj} lower than the maximum rating T_{vjmax}= 175ºC, the allowable case temperature rise can be calculated as:

$T_{C(max)} = 175 - \Delta T_{(j-c)}$.

Please also note that the case temperature T_C should not exceed its maximum rating T_{Cmax}.

(2) Overload from steady-state operation

In this case, ripple due to P_{OL} must also be taken into consideration. As in the case of (1), perform a square wave approximation as shown in Figure 7-10.

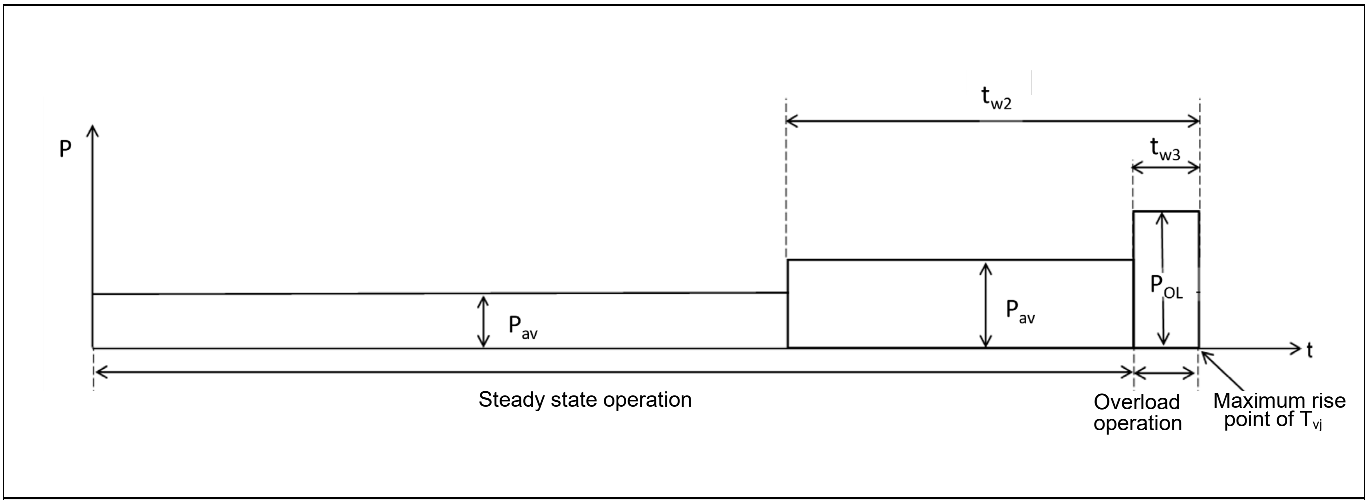


Figure 7-10. Concept of the junction temperature 3

$$\Delta T_{(j-c)} = R_{th(j-c)} \times j_{AV} - Z_{th(j-c)}@t_{w2} \times 2_{AV} + Z_{th(j-c)}@t_{w2} \times P_{av} - Z_{th(j-c)}@t_{w3} \times P_{av} + Z_{th(j-c)}@t_{w3} \times 3_{OL}$$

$$= R_{th(j-c)} \times j_{AV} + (P_{av} - P_{AV}) \times Z_{th(j-c)}@t_{w2} + (P_{OL} - P_{av}) \times Z_{th(j-c)}@t_{w3}$$

$R_{th(j-c)}$ Thermal resistance between junction and case

$Z_{th(j-c)}@t_{w2}$ Transient thermal impedance at the time of t_{w2} between junction and case

$Z_{th(j-c)}@t_{w3}$ Transient thermal impedance at the time of t_{w3} between junction and case

Using the above calculated $\Delta T_{(j-c)}$, the junction temperature can be calculated as

$T_{vj} = T_c + \Delta T_{(j-c)}$ (Here Tc is measurement value at the position of just under chip by e.g. thermocouple)

Please also note that the case temperature T_C should not exceed its maximum rating T_{Cmax}.

(3) Transient thermal impedance

Transient thermal impedance is calculated by the following equation.

The details of $R_{th(j-c)}$, R_i and τ_i are written in each product data sheet.

$$Z_{th(j-c)} = R_{th(j-c)} \times \sum_{i=1}^{4} \left\{ R_i \times \left(1 - e^{-\frac{t}{\tau_i}} \right) \right\}$$

7.2 Heat sink selection

Figure 7-11 shows the thermal equivalent circuit when multiple modules are mounted on one heat sink.
In this equivalent circuit, the temperature of the heat sink is $T_s = T_a + (P_{Q(AV)} + P_{D(AV)}) \times N \times R_{th(s-a)}$

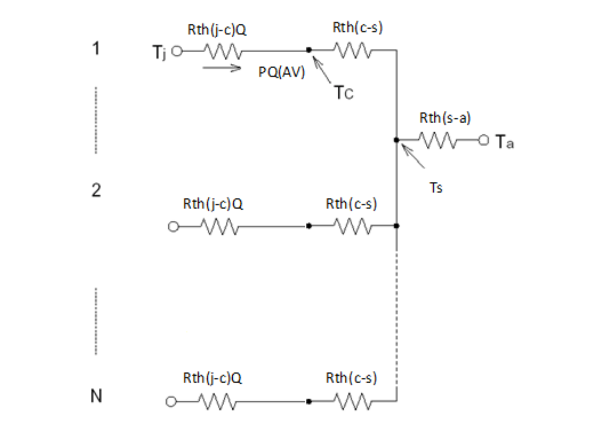


Figure 7-11. Thermal equivalent circuit

T_a: Ambient temperature
$P_{Q(AV)}$: average power loss of transistor part (W)
N: number of modules
$R_{th(s-a)}$: thermal resistance from heatsink to ambient (K/W)

In this equivalent circuit, case temperature T_C is calculated as:

$T_C = T_s + (P_{Q(AV)} + P_{D(AV)}) \times R_{th(c-s)}$
$\quad = T_a + (P_{Q(AV)} + P_{D(AV)}) \times N \times R_{th(s-a)} + (P_{Q(AV)} + P_{D(AV)}) \times R_{th(c-s)}$
$R_{th(c-s)}$: Contact thermal resistance between case and heat sink

Heat sink should be selected so that the calculated Tc does not exceed the value $T_{C(max)}$ which is obtained in 7.1.
Therefore, the required thermal resistance of heat sink is calculated as:

$T_C = T_a + (P_{Q(AV)} + P_{D(AV)}) \times N \times R_{th(s-a)} + (P_{Q(AV)} + P_{D(AV)}) \times R_{th(c-s)} < T_{C(max)}$

$$\therefore R_{th(s-a)} < \frac{T_{C(max)} - T_a - (P_{Q(AV)} + P_{D(AV)}) \times R_{th(c-s)}}{(P_{Q(AV)} + P_{D(AV)}) \times N}$$

7.3. General precautions when applying to inverters

The above calculation method is a simplified calculation method. Please pay attention to the following when conducting detailed calculations.

① One period of output current should be divided into multiple pulses and it is necessary to calculate the power loss and the temperature based on actual "PWM duty", "Output current" and "V_{CEsat}, V_{EC}, E_{on}, E_{off}, E_{rr} at the output current" ,and to accumulate the results.
② PWM duty depends on the signal generation method (modulation method).
③ The relationship between the output current waveform (or output current) and the PWM duty depends on various factors such as signal generation method (modulation method), load, etc. Therefore, the output current should be based on actual measured waveforms.
④ For V_{CEsat} and V_{EC}, use the value of T_{vj} = 150℃.
⑤ For E_{on}, E_{off}, and E_{rr}, the value at T_{vj} = 150℃ under half bridge operation is used.

7.4 General precautions for thermal design

① It is necessary to consider the operating conditions that make the worst case losses.
② Temperature change due to output current frequency/period should be taken into account.
(Approximately +30% at 60 Hz. When the output current fundamental frequency is low (several Hz) and lasts several seconds, it will be similar as the temperature when DC continuous switching operation at its peak current.
③ In addition to T_{vjmax}, the influence of power cycles and thermal cycles must also be taken into consideration.

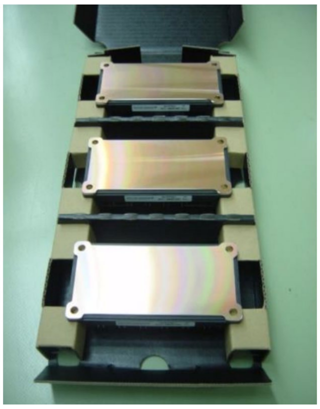
8. Handling Precautions

Elements of a power module may be damaged depending on usage conditions (electrical / mechanical stress, handling, etc.). In order to use our power module safely, observe the following precautions and use correctly.

8.1 Handling Precautions

Caution	
Transportation method	• During transportation, please keep the shipping box in the correct orientation. If it is inverted or excessive force is applied, the terminals may be deformed or the resin case may be broken. • Throwing or dropping may cause the device to break. • Care should be taken when transporting during rainfall or snowfall to not expose the device to water. Do not use the device if it is exposed to water as it may malfunction at the time of use.
Storage method	• The temperature and humidity of the storage location is desirably within the normal temperature and humidity range of 5 - 35°C and 45 - 75%. If stored in a more extreme environment than this temperature and humidity, the performance and reliability of the device may decrease.
Long-term storage	• When storing the product for a long term (over 1 year), please take measures for dehumidification. In addition, please confirm that there is no scratch, dirt, rust etc. on the device when using after long term storage.
Usage environment	• Use in environments where high humidity (including condensation), organic solvents directly adhere, where corrosive gas is generated, or in places where explosive gas, dust, salt, etc. are present may cause serious accidents. Please avoid usages in these environments.
Flame retardance	• For the case material, UL standard 94V-0 certified products are used. It is not incombustible, so please use caution.
Countermeasure against static electricity	· Please observe the following items in order to prevent damage due to static electricity. (1) Precautions to prevent static electricity destruction If static electricity charged on the human body and packing materials becomes an excessive voltage (±20V or more) and is applied between the gate and the source, the device may be damaged. The basic principle of static electricity countermeasure is to minimize the generation of static electricity and to avoid application of the voltage to the device. * Do not use containers that are susceptible to static electricity for transportation and storage. * It is recommended to short-circuit the gate and source with carbon cloth/foam etc. until just before using the module. Also, please wear gloves so as not to touch the terminals with bare hands. Avoid gloves and work clothes that are easy to charge, such as nylon. * During assembly, ground the equipment to be used and the person performing work. It is also recommended to ground a conductive mat on the surface of the work table and the floor around the work table. Assembly refers to the point in time when the product is removed from the packing box. * Please note that when the gate-source is open on the printed circuit board on which the element is mounted, it may be destroyed by the static electricity charged on the printed circuit board. * When using a soldering iron, use a low voltage (12 V to 24 V) soldering iron for semiconductors, Ground the tip. (2) Open Gate-source Guidelines * Do not apply voltage between the drain and the source while the gate and source are open. * When removing the element, short the gate and source and remove it.

⚠ Caution

Countermeasure against static electricity	(3) Interior shipping container Conductive plastic is used for the interior box, so the conductive foam used for short circuiting between gate and source is not necessary. As with the conventional conductive foam, this conductive plastic tray is not an electrostatic component that completely shorts the gate and source or clamps the overvoltage. Please take adequate measures against static electricity during the process of taking out the module out of the packing box to mounting in the equipment, by using a conductive mat grounded to earth with a band to the operator. If you take out the module out of the interior box and store it in another container etc, please implement electrostatic measures such as using a conductive container for the storage container. Also, since the module main body is not fixed to the interior tray, please be careful about handling so as not to drop the module while taking out or unpacking the interior tray.  Built-in tray packing example
Antistatic measures	• When performing an acceptance test (saturation voltage test etc.) such as applying a voltage between the gate and the source, Discharge between the gate and the source before returning to the packing tray or storage (conductive) container after the test is completed. Please discharge the electric charge with a high resistance (about 10 kΩ).
Connection Method	· When mounting the module in the product, do not apply excessive stress to the screw terminal (structure). The terminal structure itself and the joint of the terminal structure case may be damaged. · When connecting to the module pins by using printed circuit board etc, please be careful not to deform with excessive stress. · When fixing the printed circuit board to the module case with tapping screws, please pay attention to the size of the screws and mounting method. If you mistake the screw size and installation method, the case of the module may be damaged.

8.2 Flame Retardance

Since the PPS used for the case and lid of the SiC power module has flame retardance conforming to UL 94 V-0 and has self-extinguishing properties, there is no danger of spreading fire if the combustion source is cut off.

Silicone gel is flammable and does not comply with UL 94 V-0. Products with characteristics with a flash point of 340°C, an ignition point of 450°C, and dielectric breakdown strength after curing of 10 kV/mm or more are used. Also, there is no self-extinguishing property, so in case of fire, it is necessary to extinguish by using powder fire extinguisher, carbon dioxide extinguishing agent, foam extinguishing agent etc. Other components such a silicon chip, copper baseplate, etc. do not have applicable UL flame retardance standard.

9. Safety standard (UL Standard)

Mitsubishi Power Modules are UL certified (Recognized) for UL Standard 1557 and Category Code QQQX2.
(Except for some special items, File No. E 323585)

Power modules are not certified for other safety standards (TUV, VDE, CSA etc).
(Reinforcement of CE marking is not made considering correspondence to insulation.)
Regarding European CE and China CCC, as of October 2016, the target regulation as a power module has not been confirmed.

Important Notice

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