MITSUBISHI ELECTRIC

< SOPIPM >

SOPIPM Series APPLICATION NOTE
SP2SK

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CHAPTER 1 INTRODUCTION

1.1 Features of SOPIPM

SOPIPM is an ultra-small compact intelligent power module(IPM) with transfer mold package suitable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which make it easy for fan and low power motor control applications.

Mitsubishi Electric developed Super mini DIPIPM series which is de facto standard power module for inverterized home appliances, SLIMDIP series which can realize smaller package, and so on. SOPIPM series has been newly developed to integrate our conventional technologies and to adding surface mount type into DIPIPM family lineup.

Main features of SOPIPM are as below.

- *Surface mount package realizes easier board mounting.*
- *Optimal pin layout realizes easier PCB wiring design and enables smaller PCB size.*
- *Insulation distance between pins ensured, realizing easier board mounting without coating process.*
- *SOPIPM has newly integrated interlock function in addition to conventional protection functions of the Super mini DIPIPM which is popular to Inverterized appliances.*
- *Installing RC-IGBT simultaneously realizes compact package and low loss performance can go together.*
- *Bootstrap diode is integrated for the P-side drive power supply like conventional DIPIPM series, reducing the number of peripheral.*

By virtue of these features, we believe SOPIPM is especially suitable for low cost inverter motor drive applications and can contribute like fan driving because of achieving system cost reduction.

Fig.1-1-1 and Fig.1-1-2 show the outline and internal cross-section structure respectively.

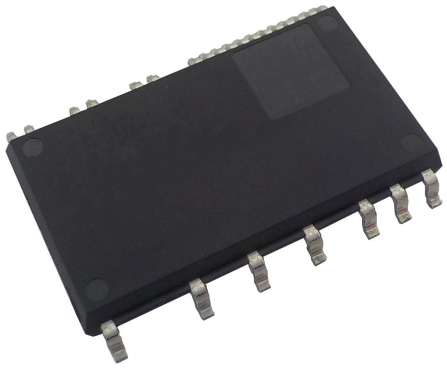


Fig.1-1-1 Package photograph

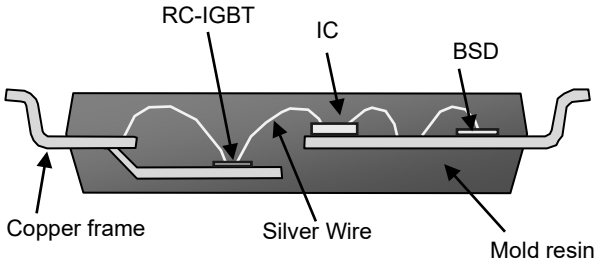


Fig.1-1-2 Internal cross-section structure

1.2 Functions

SOPIPM has following functions and inner block diagram as described in Fig.1-2-1.

- For P-side IGBTs:
  - Drive circuit;
  - High voltage level shift circuit;
  - Control supply under voltage (UV) lockout circuit (without fault signal output).
  - Built-in bootstrap diode (BSD) with current limiting resistor
- For N-side IGBTs:
  - Drive circuit;
  - Short circuit (SC) protection circuit (by inserting external shunt resistor into main current path)
  - Control supply under voltage (UV) lockout circuit (with fault signal output)
  - Over temperature (OT) protection by monitoring LVIC temperature.
  - Outputting LVIC temperature by analog signal
- Fault Signal Output
  - Corresponding to N-side IGBT SC, N-side UV and OT protection.
- Arm short protection
  - Interlock function (IL)
- IGBT Drive Supply
  - Single DC15V power supply (in the case of using bootstrap method)
- Control Input Interface
  - Schmitt-triggered 3V, 5V input compatible, high active logic.
- UL recognized
  - UL 1557 File E323585

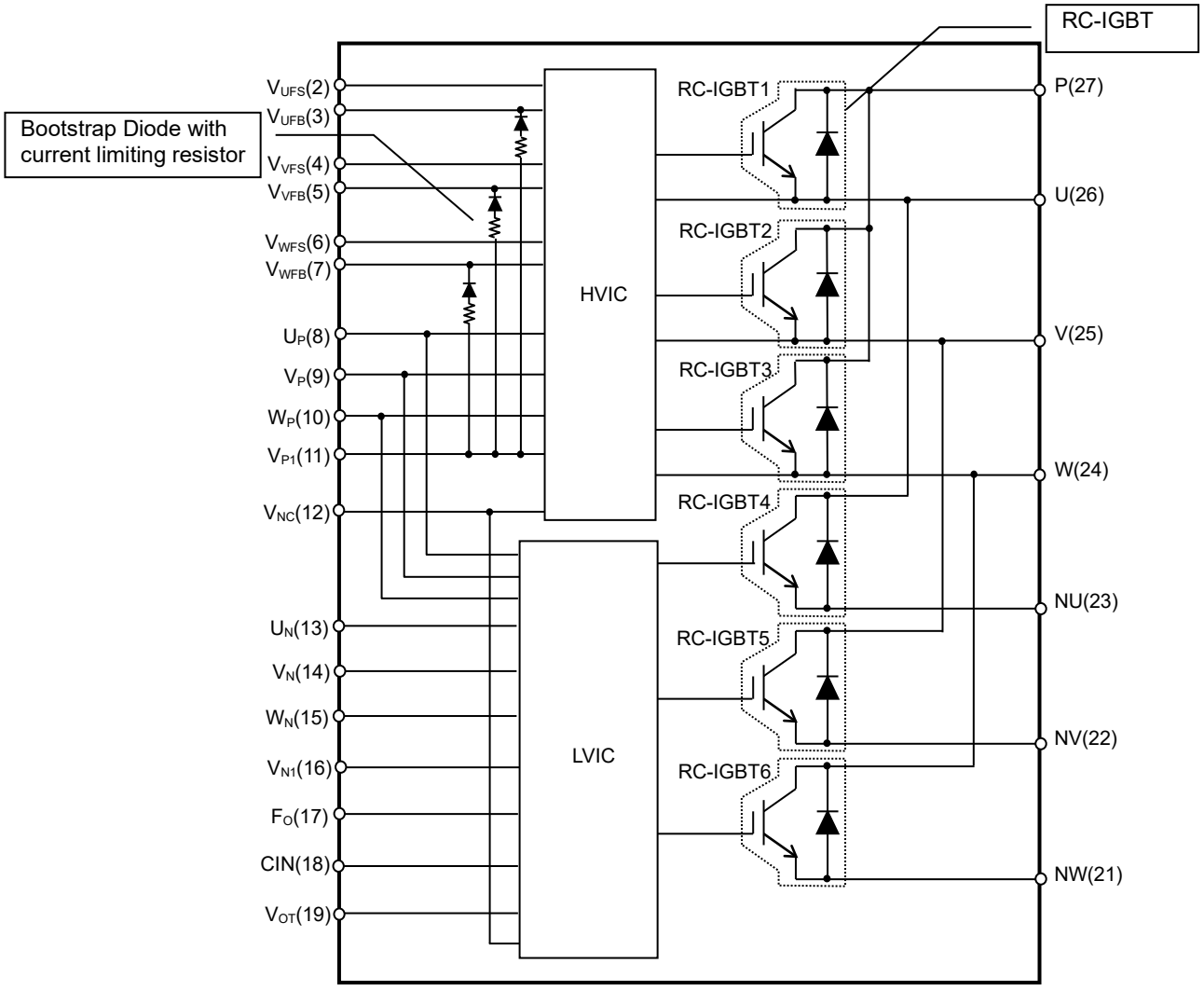


Fig.1-2-1 Inner block diagram

1.3 Target Applications

Motor drives for low power motors, such fan motors, water pumps, and refrigerators

1.4 Product Line-up

Table 1-4-1 SOPIPM Line-up

Part Number	Ratings	Isolation Voltage
SP2SK	2A/600V	V_{iso} = 1500Vrms Sine 60Hz, 1min All shorted pins-heat sink

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 SOPIPM Specifications

SOPIPM specifications are described below by using SP2SK (2A/600V) as an example. Please refer to respective datasheets for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of SP2SK (2A/600V) are shown in Table 2-1-1.

Table 2-1-1 Maximum Ratings (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	450	V	
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V	(1)
V_{CES}	Collector-emitter voltage	-	600	V	(2)
$\pm I_C$	Each IGBT collector current	T_C= 25°C (Note1)	1.5	A	(3)
$\pm I_{OP}$	Output current (peak)	Sine-wave, T_C= 25°C, fo≥1Hz	2	A	(4)
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, less than 1ms	3	A	
T_j	Junction temperature	-	-30~+150	°C	(5)

Note1: Pulse width and period are limited due to junction temperature.

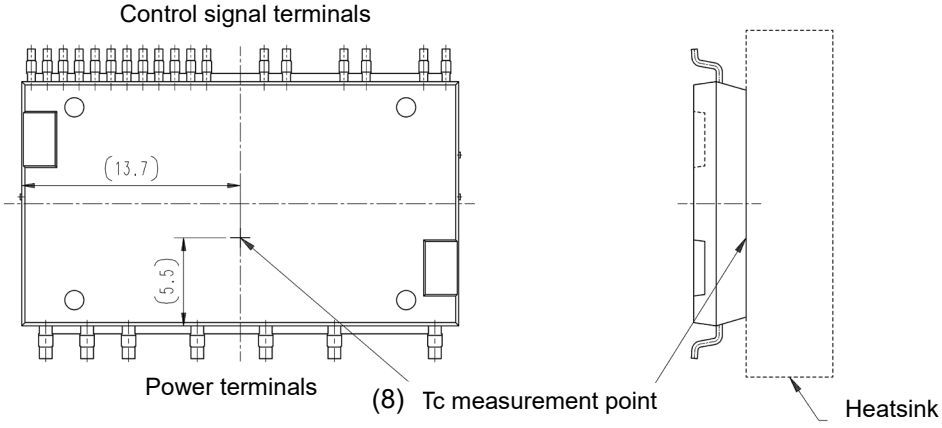
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}- V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	F_O terminal sink current	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 125°C, non-repetitive, less than 2μs	400	V	(6)
T_C	Module case operation temperature	Measurement point of Tc is provided in the following figure	-30~+115	°C	
T_{stg}	Storage temperature	-	-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and marking side or outer heatsink plate	1500	V_{rms}	(7)

Fig.2-1-1 Tc measurement position (unit: mm)



Explanation of each item:

(1) Vcc	The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.
(2) Vcc(surge)	The maximum P-N surge voltage in switching state. If P-N voltage exceeds this voltage, addition of a snubber circuit or reduction of parasitic wiring inductance is necessary to absorb the surge under this voltage.
(3) VCES	The maximum applied collector-emitter voltage of built-in IGBT and FWD.
(4) $\pm I_C$	The allowable current flowing into collector electrode (@Tc=25°C). Pulse width and period are limited due to junction temperature Tj.
(5) Tj	The maximum junction temperature rating is 150°C. But for safe operation, it is recommended to limit the average junction temperature up to 125°C. Repetitive temperature variation ΔTj affects the life time of power cycle, so please refer life time curves for safety design.
(6) Vcc(prot)	The maximum supply voltage for turning off IGBT safely in the case of an SC or OC fault. The power chip might be damaged if supply voltage exceeds this specification.
(7) Isolation voltage	Isolation voltage is the voltage between all pins, which are shorted mutually, and marking side of SOPIPM package surface (attached heatsink side). The maximum rating of isolation voltage of SOPIPM is 1500Vrms.
(8) Tc position	When operating SOPIPM with a heatsink, its junction temperature Tj should be considered with its power loss, its case temperature Tc and its Junction to case thermal resistance Rth(j-c). To monitor accurate case temperature Tc, it is necessary to mount a thermocouple on the heat sink surface at the defined position.

2.1.2 Thermal Resistance

Table 2-1-2 and table 2-1-3 show the thermal resistance of SP2SK (2A/600V).

As SOPIPM applies RC-IGBT, which integrates IGBT and FWD on one chip die as a power chip, it is necessary to consider the sum of IGBT part and FWD part losses for its temperature estimation. Please refer Chapter 3.2 for its Power Loss and Thermal Dissipation Calculation.

(1) In case of using outer heatsink for heat radiation

When operating SOPIPM with a heatsink, its thermal rise should be considered with its power loss, its case temperature Tc and its Junction to case thermal resistance $R_{th(j-c)}$.

Table 2-1-2 shows the thermal resistance of SP2SK (2A/600V).

Table 2-1-2 Thermal resistance of SP2SK (2A/600V)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note)	Inverter IGBT part (per 1/6 module)	-	-	15	K/W

Note: With heatsink

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-2. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max)

For example, the IGBT transient thermal impedance of SP2SK in 0.5s is 15×0.8=12K/W.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order).
(E.g. In the cases at motor starting, at motor lock・・・)

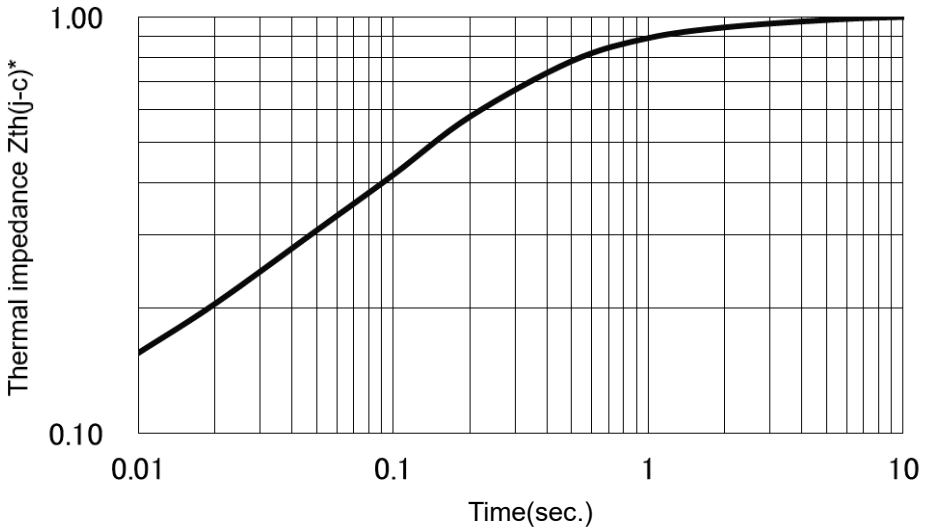


Fig.2-1-2 Typical transient thermal impedance

(2) In case of not using outer heatsink

When operating SOPIPM without heatsink, its thermal rise should be considered with its power loss, its ambient temperature Ta and its Junction to ambient thermal resistance $R_{th(j-a)}$.

Table 2-1-3 shows the thermal resistance of SP2SK (2A/600V). This thermal resistance may be different due to the measurement point of ambient temperature and cooling system conditions.

Table 2-1-3 Thermal resistance of SP2SK (2A/600V)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-a)Q}$	Junction to ambient thermal resistance (Note)	Inverter IGBT part (per module)	-	-	31	K/W

Note : The measurement condition is under JEDEC51-2A.
The junction to ambient thermal resistance depends on the environment condition of board patterns, board specifications, placement, etc.

2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-4 shows the typical static characteristics and switching characteristics of SP2SK (2A/600V).

Table 2-1-4 Static characteristics and switching characteristics of SP2SK (2A/600V) (T_j = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB} = 15V, V_{IN}= 5V	I_C= 2A , T_j= 25°C	-	2.30	3.10	V
			I_C= 2A , T_j= 125°C	-	2.60	3.55	
V_{EC}	FWD forward voltage	V_{IN}= 0V, -I_C= 2A		-	2.30	3.00	V
t_{on}	Switching times	V_{CC}= 300V, V_D= V_{DB}= 15V I_C= 2A, T_j= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		0.40	0.85	1.30	µs
$t_{C(on)}$				-	0.20	0.50	µs
t_{off}				-	0.90	1.60	µs
$t_{C(off)}$				-	0.10	0.35	µs
t_{rr}				-	0.25	-	µs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}	T_j= 25°C	-	-	1	mA
			T_j= 125°C	-	-	10	

Switching time definition and performance test method are shown in Fig.2-1-3 and 2-1-4.
Switching characteristics are measured by half bridge circuit with inductance load.

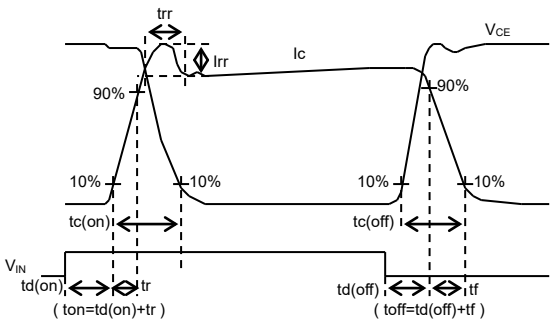


Fig.2-1-3 Switching time definition

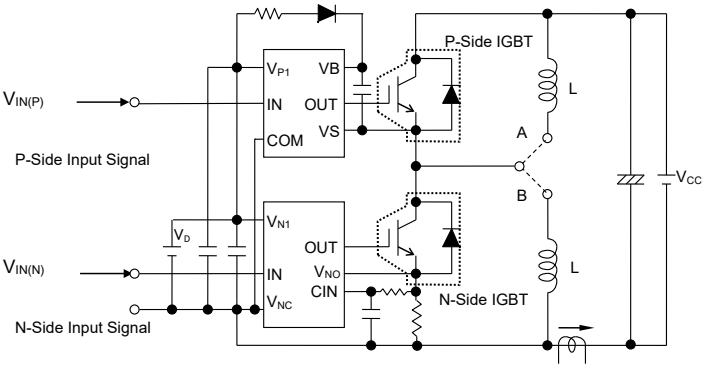


Fig.2-1-4 Evaluation circuit (inductive load)
*Short A for N-side switching, or short B for P-side switching.

Table 2-1-5 shows the typical control part characteristics of SP2SK (2A/600V).

Table 2-1-5 Control (Protection) characteristics of SP2SK (2A/600V) (T_j = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	4.20	mA
			V_D=15V, V_{IN}=5V			4.20	
I_{DB}		Each part of V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.10	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.10	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 1)		0.455	0.480	0.505	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	T_j ≤125°C	Trip level	8.0	10.0	12.0	V
UV_{DBr}			Reset level	8.0	10.0	12.0	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature output	Pull down R=5.1kΩLVIC Temperature=95°C (Note 2)		2.76	2.89	3.03	V
OT_t	Overt temperature protection (Note 3)	V_D = 15V	Trip level	125	135	145	°C
OT_{rh}		Detect LVIC temperature	Hysteresis of trip-reset	-	10	-	°C
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	(Note 4)		20	-	-	µs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	1.70	2.35	V
$V_{th(off)}$	OFF threshold voltage			0.70	1.30	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.25	0.40	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor		1.1	1.7	2.3	V
R	Built-in limiting resistance into bootstrap Di			80	100	120	Ω

Note 1 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 2.5A.
2 : When temperature exceeds the protective level that user defined, controller (MCU) should stop the SOPIPM.
3 : When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and Fo outputs. In that case if the cooling system has error (e.g. cooling fan is out of order) or if operating without heatsink, don't reuse that SOPIPM. There is a possibility that junction temperature of power chips exceeded maximum Tj(150°C).
4 : Fault signal Fo outputs when SC, UV or OT protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20µs), but at UV or OT failure, Fo outputs continuously until recovering from UV or OT state. (But minimum Fo pulse width is 20µs.)

Recommended operating conditions of SP2SK (2A/600V) are given in Table 2-1-6.
It is highly recommended to operate the modules within these conditions so as to ensure SOPIPM safe operation.

Table 2-1-6 Recommended operating conditions of SP2SK (2A/600V)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation		-1	-	+1	V/µs
t_{dead}	Arm shoot-through blocking time	For each input signal	1.0	-	-	µs
f_{PWM}	PWM input frequency	T_C ≤ 100°C, T_j ≤ 125°C	-	-	20	kHz
PWIN(on)	Minimum input pulse width	(Note)	0.7	-	-	µs
PWIN(off)			0.7	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)	-5.0	-	+5.0	V
T_j	Junction temperature		-20	-	+125	°C

Note: SOPIPM might not make response if the input signal pulse width is less than PWIN(on), PWIN(off).

About Control supply variation
If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause SOPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

dV/dt ≤ +/-1V/µs, Vripple≤2Vp-p

2.1.4 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-1-7.
Please refer to Section 2.3 and 2.4 for the detailed outline and mounting instruction of SOPIPM.

Table 2-1-7 Mechanical characteristics and ratings of SP2SK (2A/600V)

Parameter	Condition	Reference	Limits			Unit
			Min.	Typ.	Max.	
Weight			-	3.7	-	g
Terminal pulling strength	Weight ; 2.2N	JEITA ED-4701 401 method Ⅰ	30	-	-	s

2.2 Protective Functions and Operating Sequence

SOPIPM has Short circuit (SC), Under Voltage of control supply (UV), Over Temperature (OT), temperature output (V_{OT}) and arm short prevention (interlock) functions for protection. The operating principle and sequence are described below.

2.2.1 Short Circuit Protection

(1) General

SOPIPM uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection Vsc(ref) is typ. 0.480V.

In case of SC protection works, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output. To prevent SOPIPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: 1.5μ ~ 2μs) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.

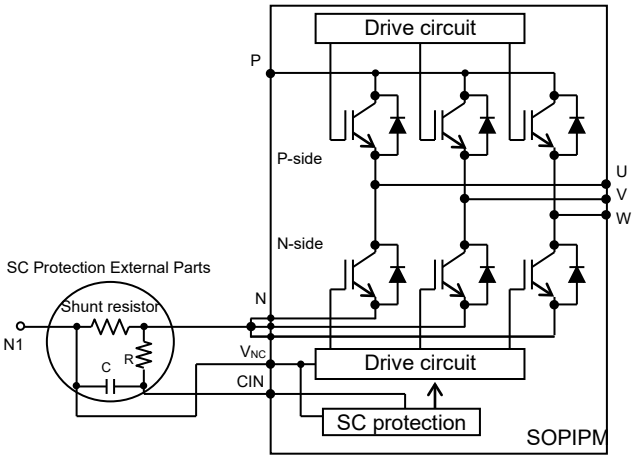


Fig.2-2-1 SC protecting circuit

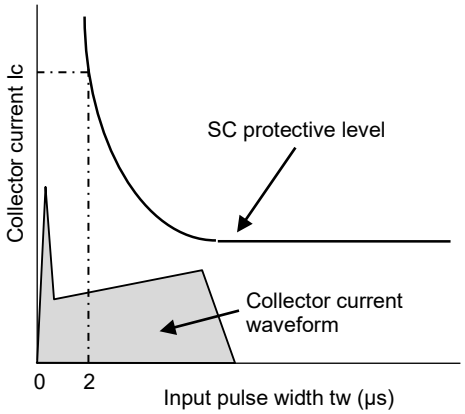


Fig.2-2-2 Filter time constant setting

(2) SC protection Sequence

SC protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: IGBT ON and carrying current.

a2. Short circuit current detection (SC trigger).
(It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)

a3. All N-side IGBTs gate are hard interrupted.

a4. All N-side IGBTs turn OFF.

a5. Fo outputs for t_{Fo}=minimum 20μs.

a6. Input = “L”. IGBT OFF

a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)

a8. Normal operation: IGBT ON and outputs current.

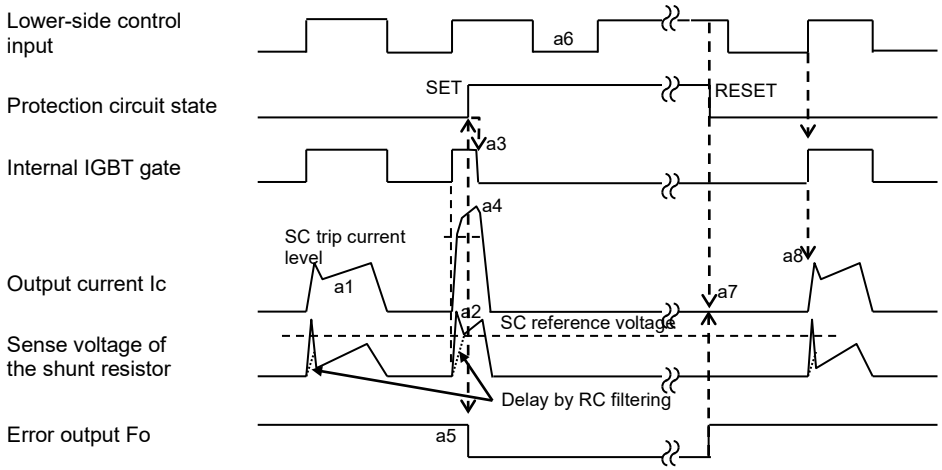


Fig.2-2-3 SC protection timing chart

(3) Determination of Shunt Resistance

1) Shunt resistance

The value of current sensing resistance is calculated by the following expression:

$$R_{Shunt} = V_{SC(ref)} / SC$$

where $V_{SC(ref)}$ is the referenced SC trip voltage.

The maximum SC trip level SC(max) should be set less than the IGBT minimum saturation current which is specified in each product's datasheet. The parameters ($V_{SC(ref)}$, R_{Shunt}) tolerance should be considered when designing the SC trip level.

An example of calculation is shown below for SP2SK.
The SC(max) should be set to 2.5A. Its tolerance in the spec of $V_{SC(ref)}$ is shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$

Condition	Min.	Typ.	Max.	Unit
at T_j=25°C, V_D=15V	0.455	0.480	0.505	V

Then, the range of SC trip level can be calculated by the following expressions:

$R_{Shunt(min)}=V_{SC(ref)\ max}$ /SC(max)
$R_{Shunt(typ)}= R_{Shunt(min)}$ / 0.95* then SC(typ) = $V_{SC(ref)\ typ}$ / $R_{Shunt(typ)}$
$R_{Shunt(max)}= R_{Shunt(typ)}$ x 1.05* then SC(min)= $V_{SC(ref)\ min}$ / $R_{Shunt(max)}$
*)This is the case that shunt resistance tolerance is within +/-5%.

So the SC trip level range is described as Table 2-2-2.

Table 2-2-2 Operative SC Range (R_{Shunt}=202mΩ (min), 213mΩ (typ), 223mΩ (max)

Condition	Min.	Typ.	Max.	Unit
at T_j=25°C, V_D=15V	2.04	2.26	2.50	A

(e.g. 202mΩ ($R_{shunt(min)}$)= 0.505V (=$V_{SC(max)}$) / 2.5A(=SC(max))

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the SOPIPM. (Recommended time constant: 1.5μ ~ 2μs)
When the voltage drop on the external shunt resistor exceeds the SC trip level, the time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$

$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

Vsc : the CIN terminal input voltage, Ic : the peak current, τ : the RC time constant

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to IGBT gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	Min.	Typ.	Max.	Unit
IC transfer delay time	-	-	0.5	μs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:

$$t_{TOTAL}=t1+t2$$

2.2.2 UV : Control Supply under voltage protection

(1) General

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4.

Both P-side and N-side have UV protecting function; however, fault signal (Fo) output only corresponds to N-side UV protection. The Fo output continuously during UV state. P-side UV protection shut the gates off without Fo output.

In addition, there is a noise filter (typ. 7μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 7μs after UV happened.

Table 2-2-4 SOPIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0 - 4V (P, N)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is also not assured. Normally IGBT does not work. But external noise may cause SOPIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4V-UV_{Dt} (N), UV_{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work.
UV_{Dt} (N)-13.5V UV_{DBt} (P)-13.0V	IGBT works; however, conducting loss and switching loss will increase, and result extra temperature rise at this state.
13.5-16.5V (N) 13.0-18.5V (P)	Recommended conditions.
16.5-20V (N) 18.5-20V (P)	IGBT works; however, its switching speed becomes faster at this state. Its saturation current also becomes larger and increases SC broken risk.
20V- (P, N)	The control circuit may be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause SOPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

(2) UV protection Sequence

[N-side UV Protection Sequence]

a1. Control supply voltage V_D rising: After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied (L→H). (IGBT of each phase can return to normal state by inputting ON signal to each phase.)

a2. Normal operation: IGBT ON and carrying current.

a3. V_D level dips to under voltage trip level. (UV_{Dt}).

a4. All N-side IGBTs turn OFF in spite of control input condition.

a5. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during V_D keeps below UV_{Dr}.

a6. V_D level reaches UV_{Dr}.

a7. Normal operation: IGBT ON and outputs current.

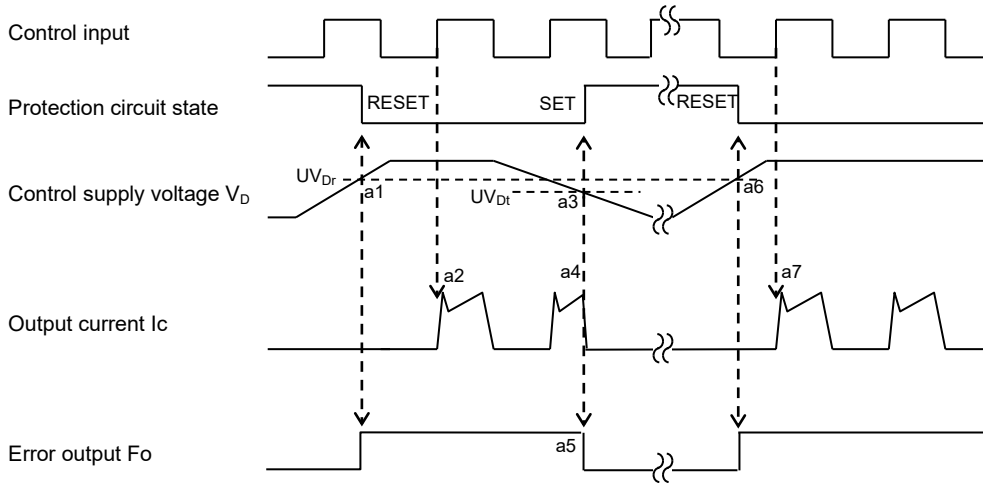


Fig.2-2-4 Timing chart of N-side UV protection

[P-side UV Protection Sequence]

a1. Control supply voltage V_{DB} rises. After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied (L→H).

a2. Normal operation: IGBT ON and carrying current.

a3. V_{DB} level dips to under voltage trip level (UV_{DBt}).

a4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.

a5. V_{DB} level reaches UV_{DBr}.

a6. Normal operation: IGBT ON and outputs current.

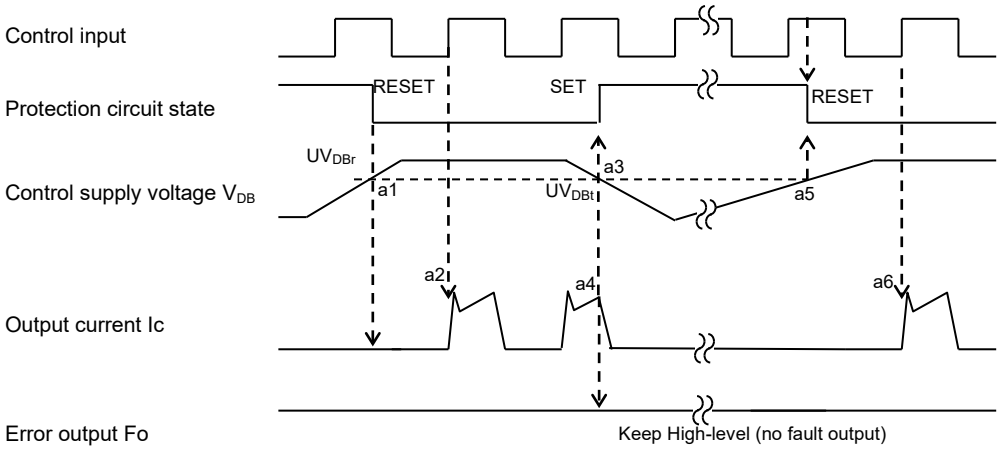


Fig.2-2-5 Timing Chart of P-side UV protection

2.2.3 OT : Over temperature protection

(1) General

SOPIPM series have OT (over temperature) protection function by monitoring LVIC temperature rise.
While LVIC temperature exceeds and keeps over OT trip temperature, error signal Fo output and all N-side IGBTs are shut down without reference to input signal. (P-side IGBTs are not shut down.)
The specification of OT trip temperature is described in Table 2-2-5.

Table 2-2-5 OT trip temperature specification

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Over temperature protection	OT_t	V_D=15V, At temperature of LVIC	Trip level	125	135	145	°C
	OT_{rh}		Trip/reset hysteresis	-	10	-	

(2) OT protection Sequence

[OT Protection Sequence]
a1. Normal operation: IGBT ON and outputs current.
a2. LVIC temperature exceeds over temperature trip level(OT_t).
a3. All N-side IGBTs turn OFF in spite of control input condition.
a4. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during LVIC temperature keeps over OT_t.
a5. LVIC temperature drops to over temperature reset level.
a6. Normal operation: IGBT turns on by next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)

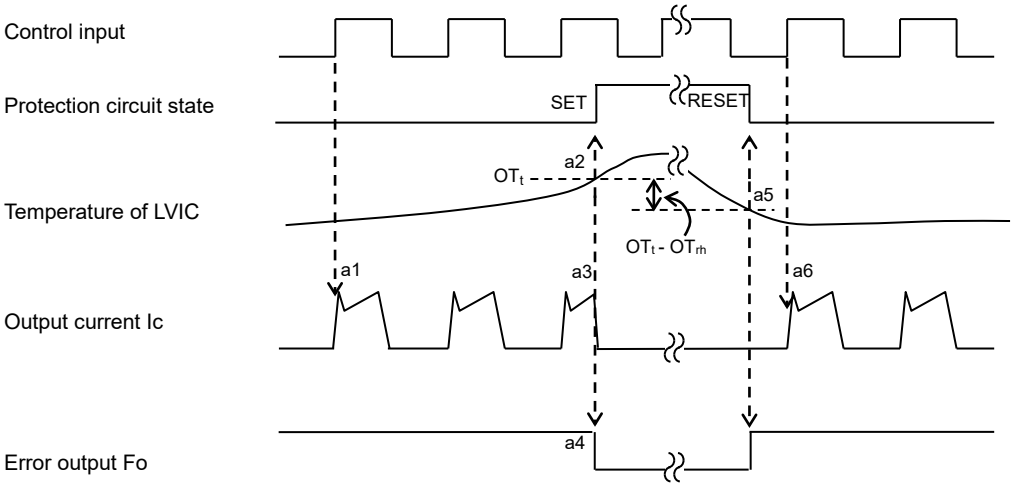


Fig.2-2-6 Timing Chart of OT protection

(3) Precaution about this OT protection function

1) In the case of rapid temperature rise

This OT protection will not work effectively in the case of rapid temperature rise like motor lock or over current. (This protection monitors LVIC temperature, so it cannot respond to rapid temperature rise of power chips.)

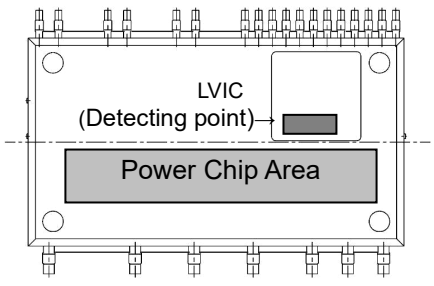


Fig.2-2-7 Temperature detecting point

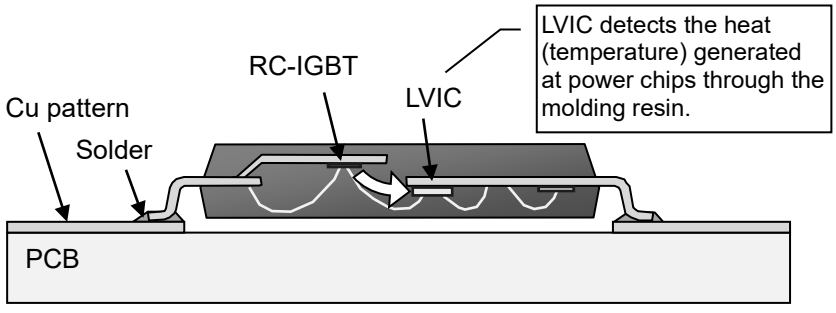


Fig.2-2-8 Thermal conducting from power chips

2) When the cooling system is in an abnormal state

When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and Fo outputs. In that case if the cooling system is in an abnormal state (e.g. the air cooling fan failure) don't reuse that SOPIPM. There is a possibility that junction temperature of power chips exceeded maximum T_j(150°C).

3) ***Without*** heatsink operation

In case of operation without heatsink, LVIC detects the heat (temperature) generated at power chips through the molding resin only. Its LVIC temperature T_{IC} is lower and rises later than the junction temperature T_j. That means the junction temperature Tj might exceed the maximum rating of T_j(150°C) when its OT protection works.

Without heatsink operation, it is recommended to use temperature output function (V_{OT}) and monitor LVIC temperature by your system. When its temperature exceeds and keeps over the threshold temperature for OT protection, your system should shut down to prevent overheating condition. For the temperature output function V_{OT}, please refer Chapter 2.2.4 in details.

2.2.4 V_{OT} : Temperature output function

(1) Usage of this function

This function measures the temperature of control LVIC by built in temperature sensor on LVIC. The heat generated at RC-IGBT transfers to LVIC through molding resin of package. So LVIC temperature cannot effectively respond to rapid temperature rise of the power chips. (e.g. motor lock, short circuit)

It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down or continuance of overload operation. In particular, when using SOPIPM without heatsink, it is recommended to use the temperature output function V_{OT} and set the appropriate temperature protection setting value on your system to prevent overheating condition.

(2) V_{OT} characteristics

V_{OT} output circuit, which is described in Fig.2-2-9, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-2-6. The characteristics of V_{OT} output vs. LVIC temperature is linear characteristics described in Fig.2-2-13. There are some cautions for using this function as below.

Table 2-2-6 Output capability(Tc=-30°C ~100°C)

	Min.
Source	1.7mA
Sink	0.1mA

Source: Current flow from V_{OT} to outside.
Sink : Current flow from outside to V_{OT}.

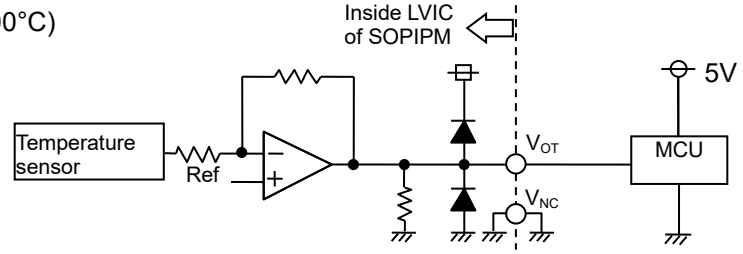


Fig.2-2-9 V_{OT} output circuit

• In the case of detecting lower temperature than room temperature

It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

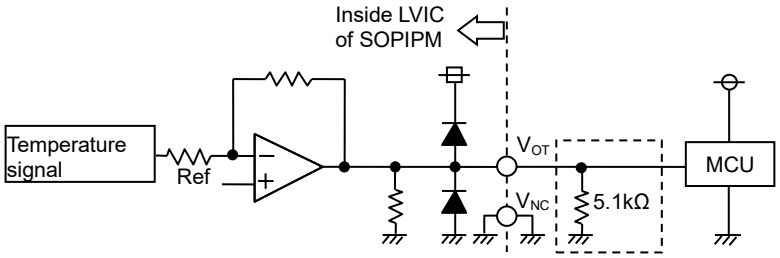


Fig.2-2-10 V_{OT} output circuit in the case of detecting low temperature

• In the case of using with low voltage controller(MCU)

In the case of using V_{OT} with low voltage controller (e.g. 3.3V MCU), V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage.

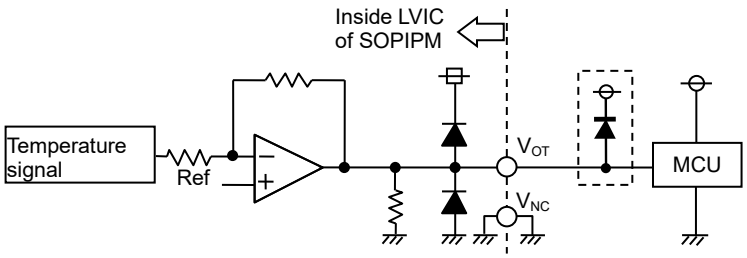


Fig.2-2-11 V_{OT} output circuit in the case of using with low voltage controller

• In the case that the protection level exceeds control supply of the controller

In the case of using low voltage controller like 3.3V MCU, if it is necessary to set the trip V_{OT} level to control supply voltage (e.g. 3.3V) or more, there is the method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-2-12). In that case, sum of the resistances of divider circuit should be as much as 5kΩ.

About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clump diode. But it should be judged by the divided output level finally.

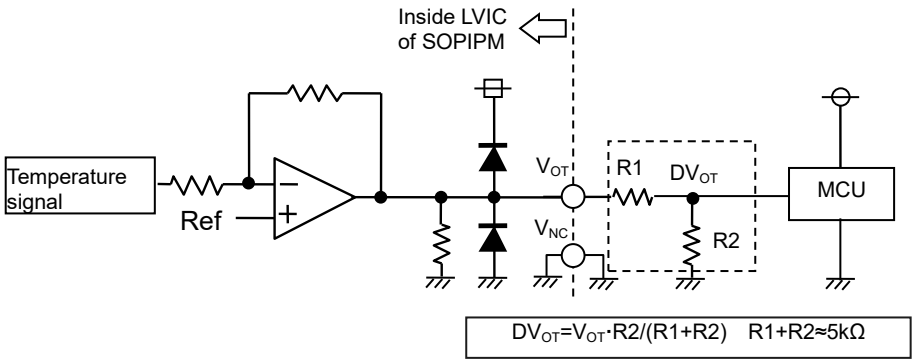


Fig.2-2-12 V_{OT} output circuit in the case with high protection level

(3) Precaution ***with/without*** heatsink

Without a heatsink operation:

As mentioned above, the heat of power chips transfers to LVIC through the package only, so the relationship between LVIC temperature: Tic (=V_{OT} output), ambient temperature: Ta, and junction temperature: Tj depends on the system cooling condition, control strategy, etc.

So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature Tic, it is important to consider the protection temperature assures; Tj≤150°C.

With heatsink operation:

The heat of power chips transfers to LVIC through not only the package but also the heatsink, so the relationship between its LVIC temperature: Tic (=V_{OT} output), its case temperature: Tc and its junction temperature: Tj depends on the system cooling condition, heat sink shape, control strategy, and so on.

So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature Tic, it is important to consider the protection temperature assures; Tc≤115°C and Tj≤150°C.

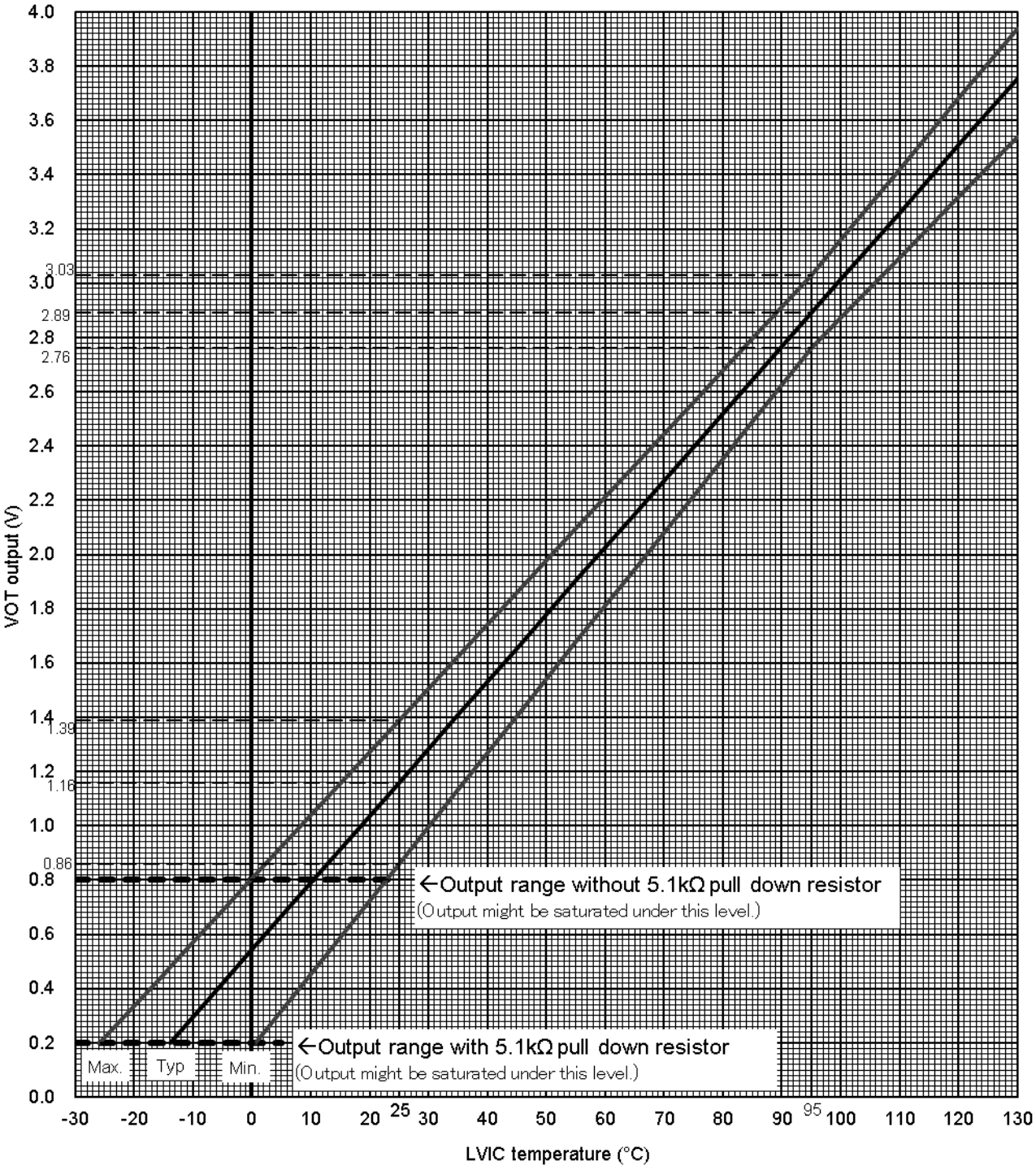


Fig.2-2-13 V_{OT} output vs. LVIC temperature

2.2.5 Interlock function

(1) General

This interlock function detects simultaneous ON of P-side and N-side in the same phase by the control IC (LVIC) and prevents arm short circuit. The LVIC compares P-side control input and N-side control input in the same phase. When the simultaneous ON signals are input, the N-side output is kept OFF state regardless of the its input state. (Fo signal is not output) P-side IGBTs output keeps to follow input signal.

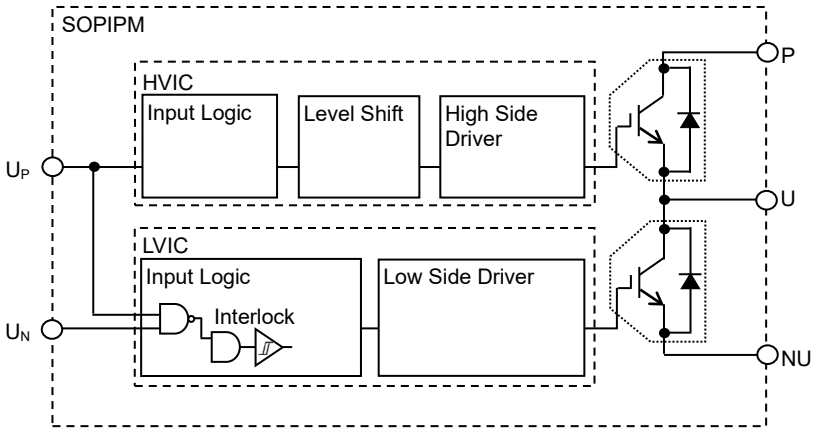


Fig.2-2-14 Interlock function block diagram (typical example: U phase)

(2) Interlock Sequence

[Interlock Sequence]

a1. Normal operation: IGBT ON and outputs current.
a2. When N-side is ON state(H), P-side turn ON(L→H) ····· N-side shut off
a3. When P-side is ON state(H), N-side turn ON(L→H) ····· N-side shut off
a4. P-side turn OFF(H→L) and N-side is ON state(H) ····· N-side turn ON

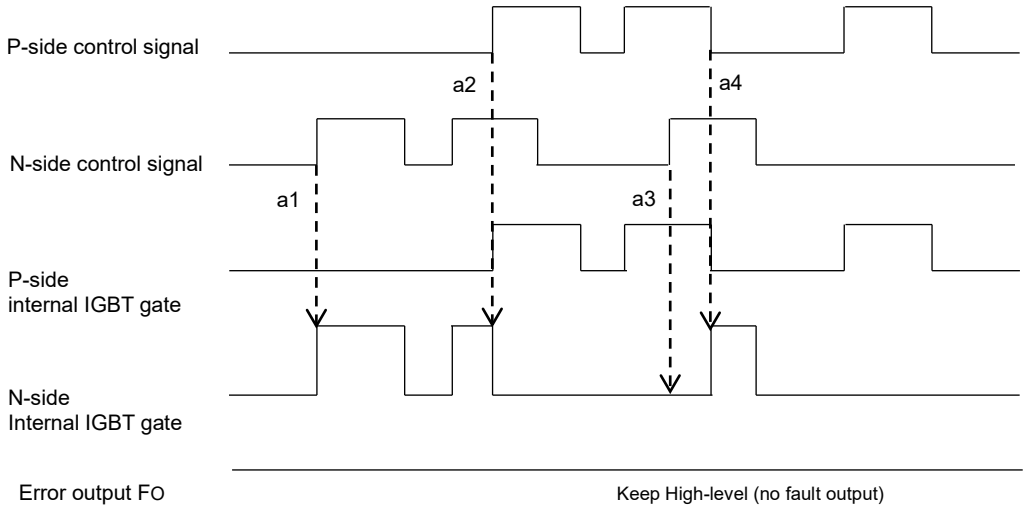


Fig.2-2-15 Timing Chart of Interlock function

2.3 Package Outlines

2.3.1 Package outlines

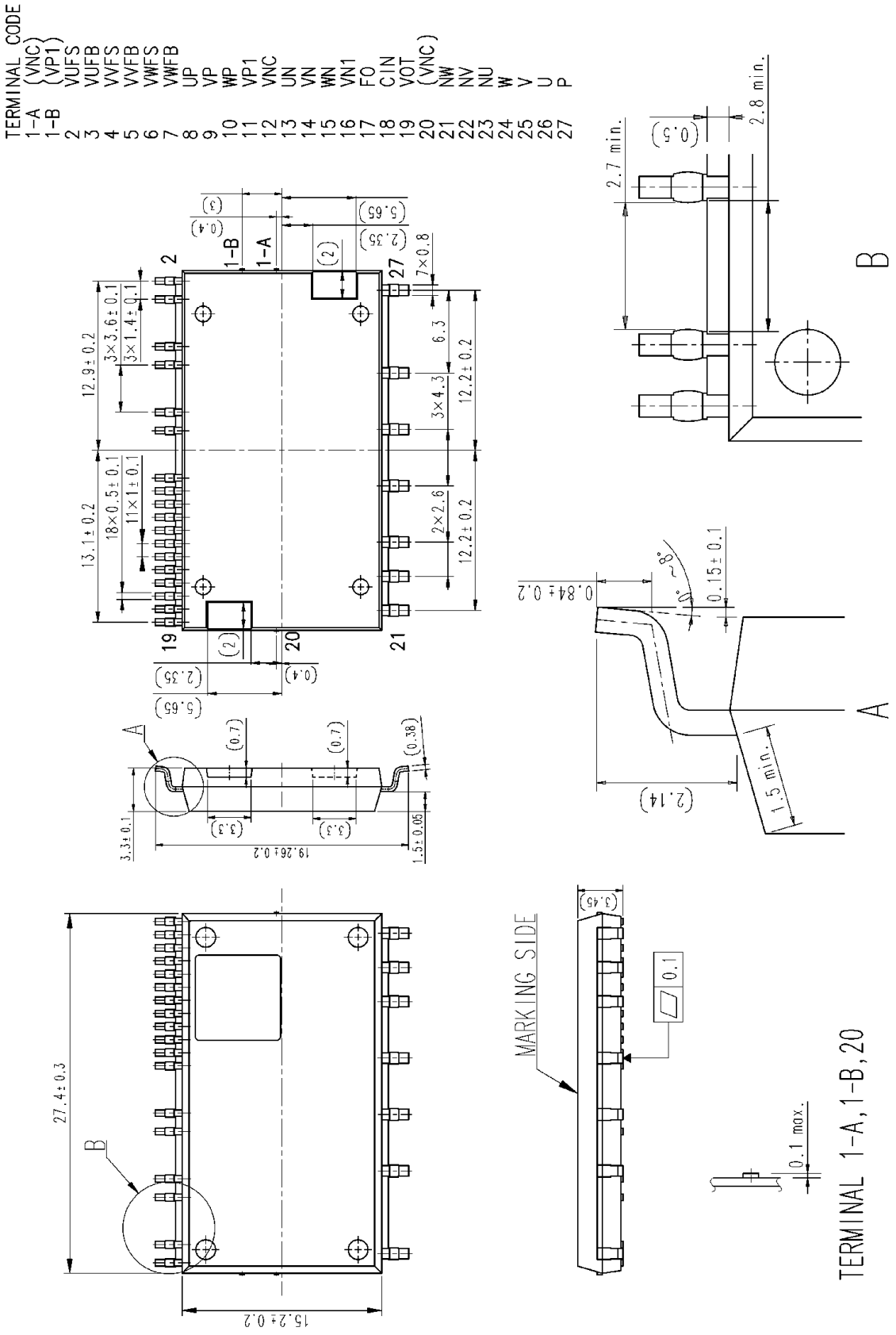


Fig.2-3-1 Package outline drawing for SPxSK (Dimension in mm)

Note) Tolerance is ±0.15mm unless stated. Dimensions do not include resin burr or gate residue.
No.1-A, 1-B and 20 are used internally, and have some potential (e.g. GND). Please leave them NC (no connection).

2.3.2 Marking

The laser marking specification of SOPIPM is described in Fig.2-3-2. Mitsubishi crest, Type name, Lot number, Country of origin, and 2D code are marked in the upper side of module.

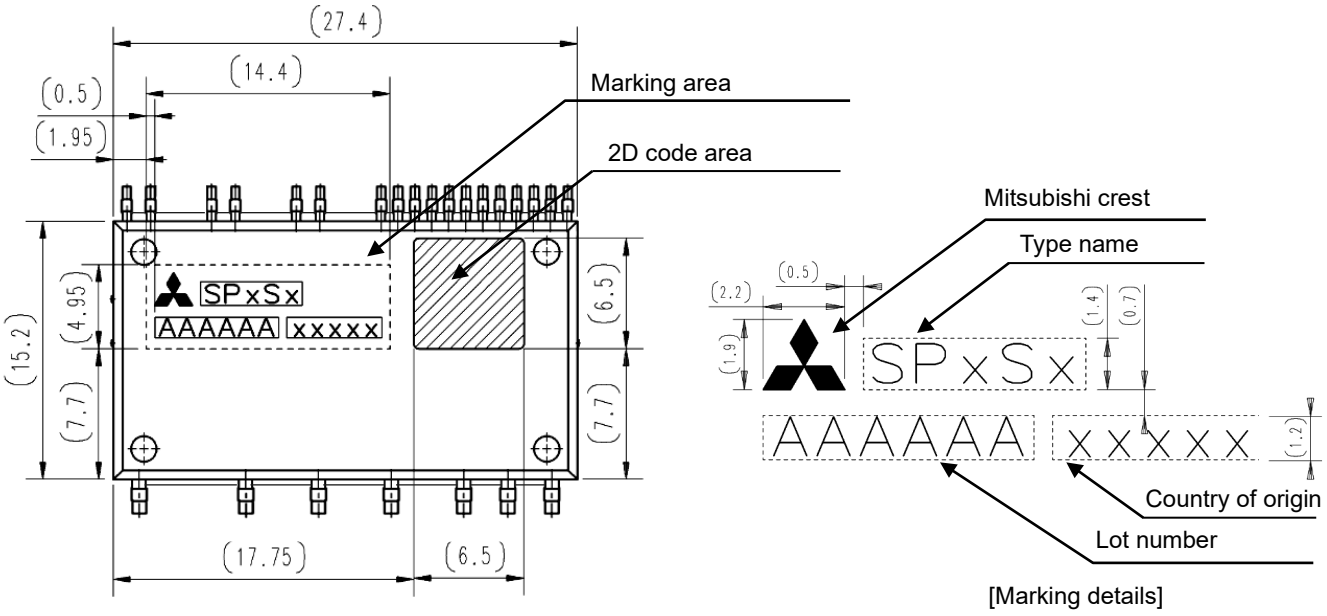


Fig.2-3-2 Laser marking view (unit: mm)

The Lot number indicates production year, month, running number and country of origin.
The detailed is described as below.

(Example) H 9 7 AA1

- Running number
- Product month (however O: October, N: November, D: December)
- Last figure of Product year (e.g. “9” in the case of 2019)
- Factory identification
  - H : Manufactured at the factory in China

2.3.3 Terminal Description

Table 2-3-1 Terminal description

Pin	Name	Description
1-A	(V_{NC})*1	Inner used terminal. Keep no connection It has control GND potential.
1-B	(V_{P1})*1	Inner used terminal. Keep no connection. It has control supply potential.
2	V_{UFS}	U-phase P-side drive supply GND terminal
3	V_{UFB}	U-phase P-side drive supply positive terminal
4	V_{VFS}	V-phase P-side drive supply GND terminal
5	V_{VFB}	V-phase P-side drive supply positive terminal
6	V_{WFS}	W-phase P-side drive supply GND terminal
7	V_{WFB}	W-phase P-side drive supply positive terminal
8	U_P	U-phase P-side control input terminal
9	V_P	V-phase P-side control input terminal
10	W_P	W-phase P-side control input terminal
11	V_{P1}	P-side control supply positive terminal
12	V_{NC}	P-side control supply GND terminal (connected to No.20 terminal internally)
13	U_N	U-phase N-side control input terminal
14	V_N	V-phase N-side control input terminal
15	W_N	W-phase N-side control input terminal
16	V_{N1}	N-side control supply positive terminal
17	F_O	Fault signal output terminal
18	CIN	SC trip voltage detecting terminal
19	V_{OT}	Temperature output
20	(V_{NC})*1	Inner used terminal. Keep no connection It has control GND potential.
21	NW	W-phase N-side IGBT emitter
22	NV	V-phase N-side IGBT emitter
23	NU	U-phase N-side IGBT emitter
24	W	W-phase output terminal (connected to No.6 terminal internally)
25	V	V-phase output terminal (connected to No.4 terminal internally)
26	U	U-phase output terminal (connected to No.2 terminal internally)
27	P	Inverter DC-link positive terminal

*1) No.1-A, 1-B and 20 are used internally, and have some potential (e.g. GND). so it is necessary to leave no connection.

Table 2-3-2 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}- V_{UFS} V_{VFB}- V_{VFS} V_{WFB}- V_{WFS}	• Drive supply terminals for P-side IGBTs. • By mounting bootstrap capacitor, individual isolated power supplies are not needed for the P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply when potential of output terminal is almost GND level. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability due to ripple or surge. In order to prevent its malfunction, a bypass capacitor with favorable frequency and temperature characteristics (~2μF) should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • Connect between V_{P1} and V_{N1} on the PCB pattern externally. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics (~2μF) should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals.Voltage input type. • These terminals are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the SOPIPM from noise interference. • Use RC filter in case of signal oscillation. (Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ))
Short-circuit trip voltage detecting terminal	CIN	• For inverter part SC protection, input the potential of shunt resistor to CIN terminal through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal. • Fo signal line should be pulled up to a 5V logic supply with over 5kΩ resistor for limitting the Fo sink current I_{Fo} up to 1mA. Normally 10kΩ is recommended.
Temperature output terminal	V_{OT}	• LVIC temperature is ouput by analog signal. • This terminal is connected the ouput of OP amplifer internally. • It is recommended to connect 5.1kΩ pulldown resistor when output linearlity is necessary under room temperature.
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be located very closely to the P and N terminal of SOPIPM. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU,NV,NW	• Open emitter terminal of each N-side IGBT • Usually, these terminals are connected to the power GND through individual shunt resistor.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.

Note: Please ensure the voltage (including surge) not exceed the specified limitation. Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to 1μs/div or less, and the sampling time of digital OSC should be set to 100MS/s and more.
If the surge voltage overs the ratings or the overlapped noise beyond its input threshold, consider countermeasures; reviewing its wiring, position and capacity of the capacitors, mounting of zener diode, filter enhancement etc.

2.4 Mounting Method

This section shows the electric spacing and mounting precautions of SOPIPM.

2.4.1 Electric Spacing

The electric spacing specification of SOPIPM is shown in Table 2-4-1 and Fig.2-4-1.

Table 2-4-1 Minimum insulation distance of SOPIPM

	Clearance (mm)	Creepage (mm)
Between live terminals with high potential	2.70	2.80
Between terminals and marking side	1.45	1.50

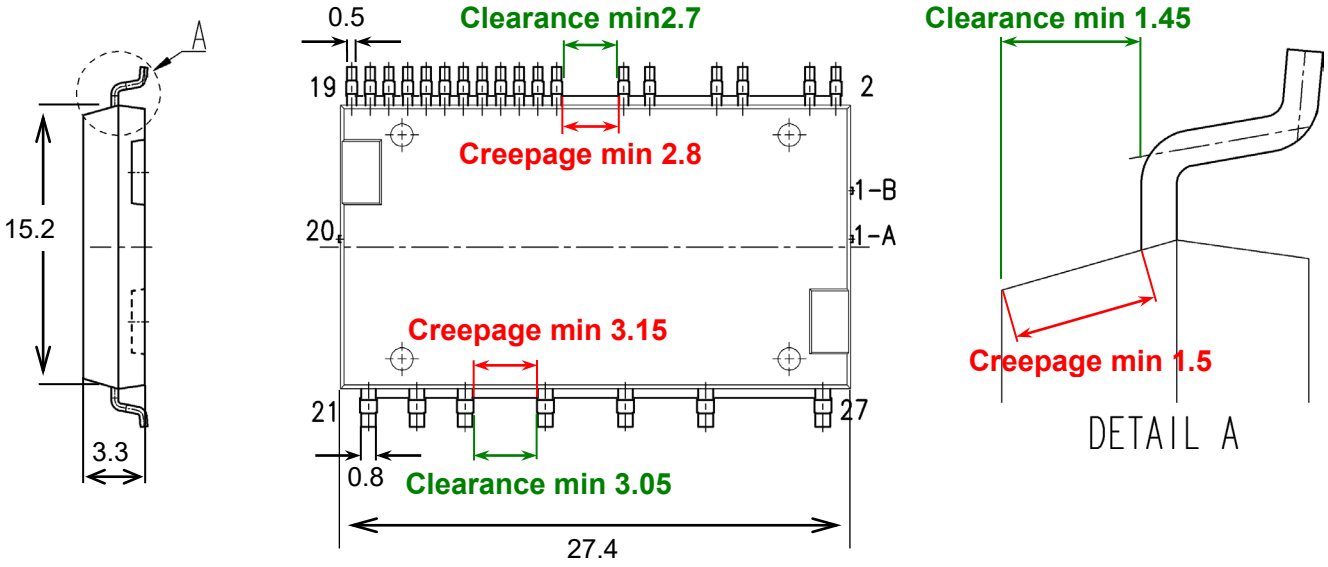


Fig.2-4-1 electric spacing specification of SOPIPM (Unit: mm)

2.4.2 Storage Condition of SOPIPM

SOPIPM series are shipped in moisture proof packing with desiccant agent to avoid moisture absorption. When surface mounted devices are soldered on the board in moisture absorption state, the devices may have package cracks or internal exfoliation at the interface between encapsulation molding resin and internal parts. For packing specification of SOPIPM series, please refer Chapter 5.1 in details.

Please refer the following the storage deadlines in the moisture-proof packing state and after opening the packing state.

(1) The storage deadline in the moisture-proof packing state:

In moisture-proof packing condition, please use within 1 year from moisture proof packing day (label printing date) under storage condition of 5~35°C, 40~75%RH.

When opening the packing, if the 30% humidity control part of the inside indicator turns lavender color or pink color, moisture absorption will occur and please use them after baking (125°C, 24hours). Since the tape carrier is not heat resistant, please bake them after transferring from tape to a heat-resistant container.

(2) The storage deadline after opening the moisture-proof packing:

Please refer Table 2-4-2 for the storage deadline after opening the packing. If it is expected to exceed the following allowable time, it is recommended to store them in a drying oven at room temperature (30%RH or less).

When beyond the following deadline, please use them after baking (125°C, 24hours). Since the tape carrier is not heat resistant, please bake them after transferring from tape to a heat-resistant container.

Table 2-4-2 The storage deadline after opening the packing for SP2SK (2A/600V)
(Equivalent to JEDEC MSL 3 or JEITA MSL 3)

Condition	Storage deadline
30°C or less, 60%RH or less	Within 168hours

2.4.3 Recommended mount pad design

When surface mounted devices are mounted on the printed circuit board, it is important to design the mount pad properly and to select the board material optimally. Mount pad design may affect yield of the soldering process and the board materials may affect reliability after soldering process.

This chapter shows design guideline for SOPIPM mount pad.

Fig.2-4-2 and Table2-4-3 shows reference mount pad design for SOPIPM series. For soldering condition for SOPIPM series, please refer Chapter 2.4.4 in details. This design is one of recommended examples. Please check the mountability in your actual condition and adjust the design finally.

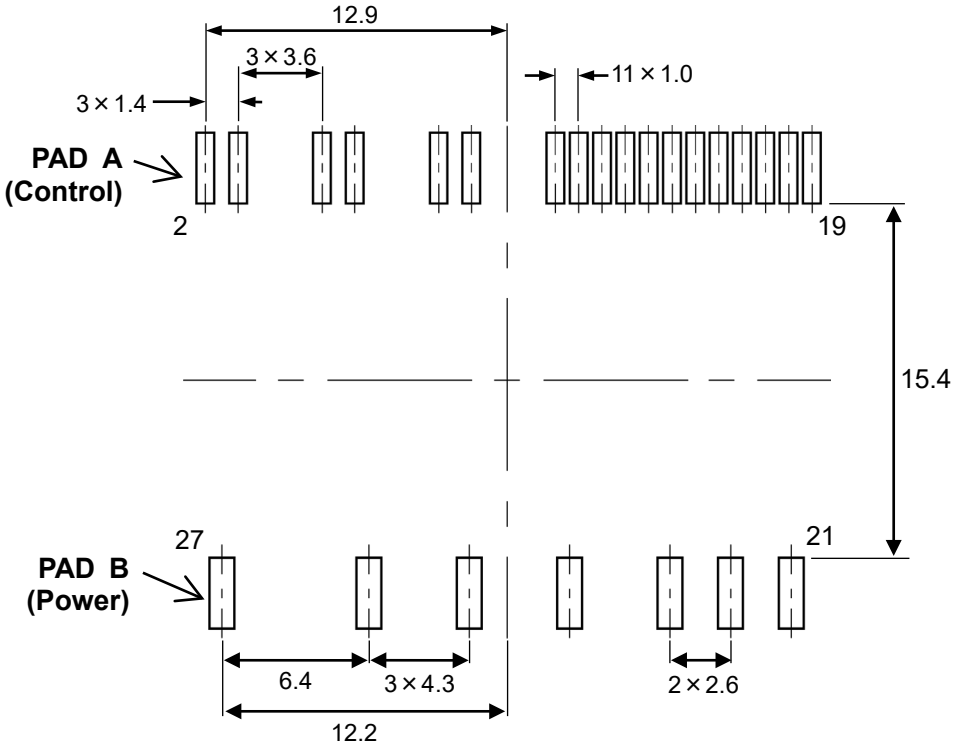


Fig.2-4-2. Recommended mount pad design (Unit:mm)

Table 2-4-3 Recommended mount pad size (Unit:mm)

	Width	Length
PAD A (Control)	0.6	3.0
PAD B (Power)	0.9	3.0

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.

(1) Reflow Soldering

SOPIPM series is tested about the reflow soldering thermostability based on IPC/JEDEC (J-STD-020.1). Fig.2-4-3 shows our recommended temperature profile for reflow soldering. The below profile is the temperature profile on the package surface. Note that the package temperature is applied to the whole device uniformly. Also note that local temperature rise and temperature drop should be avoided. Peak temperature of the terminals is up to 260°C from melting temperature of lead-free solder.

Soldering process is acceptable less than 3 times.

However, the condition might need some adjustment based on condition of solder paste, the speed of the conveyer, the land pattern, etc. It is necessary to confirm whether it is appropriate or not for your actual PCB finally.

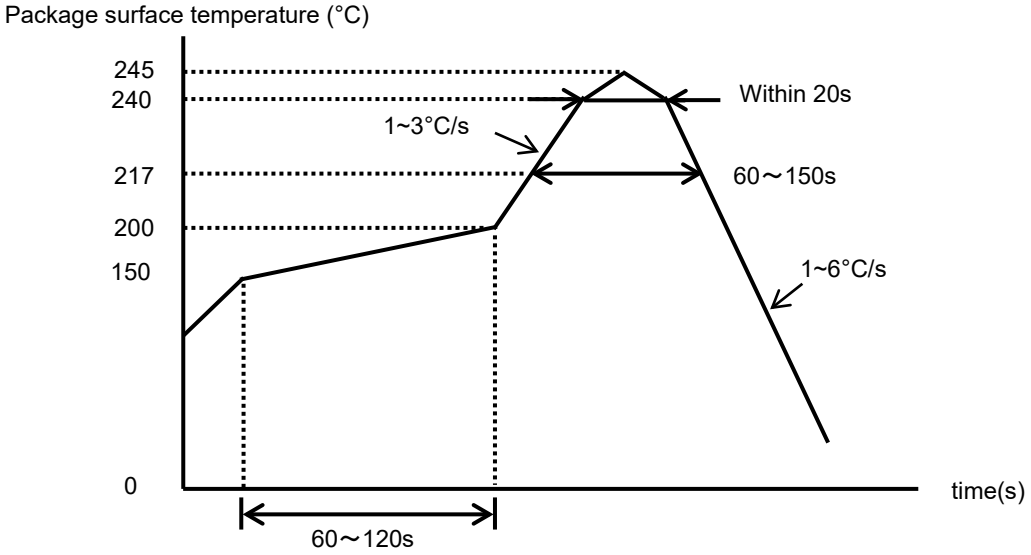


Fig.2-4-3 An example of a lead-free solder reflow temperature profile

(2) Hand soldering

SOPIPM series is also tested about hand soldering by 360 °C soldering iron tip within 5s per terminal.

The retouch is acceptable within 2 times per terminal.

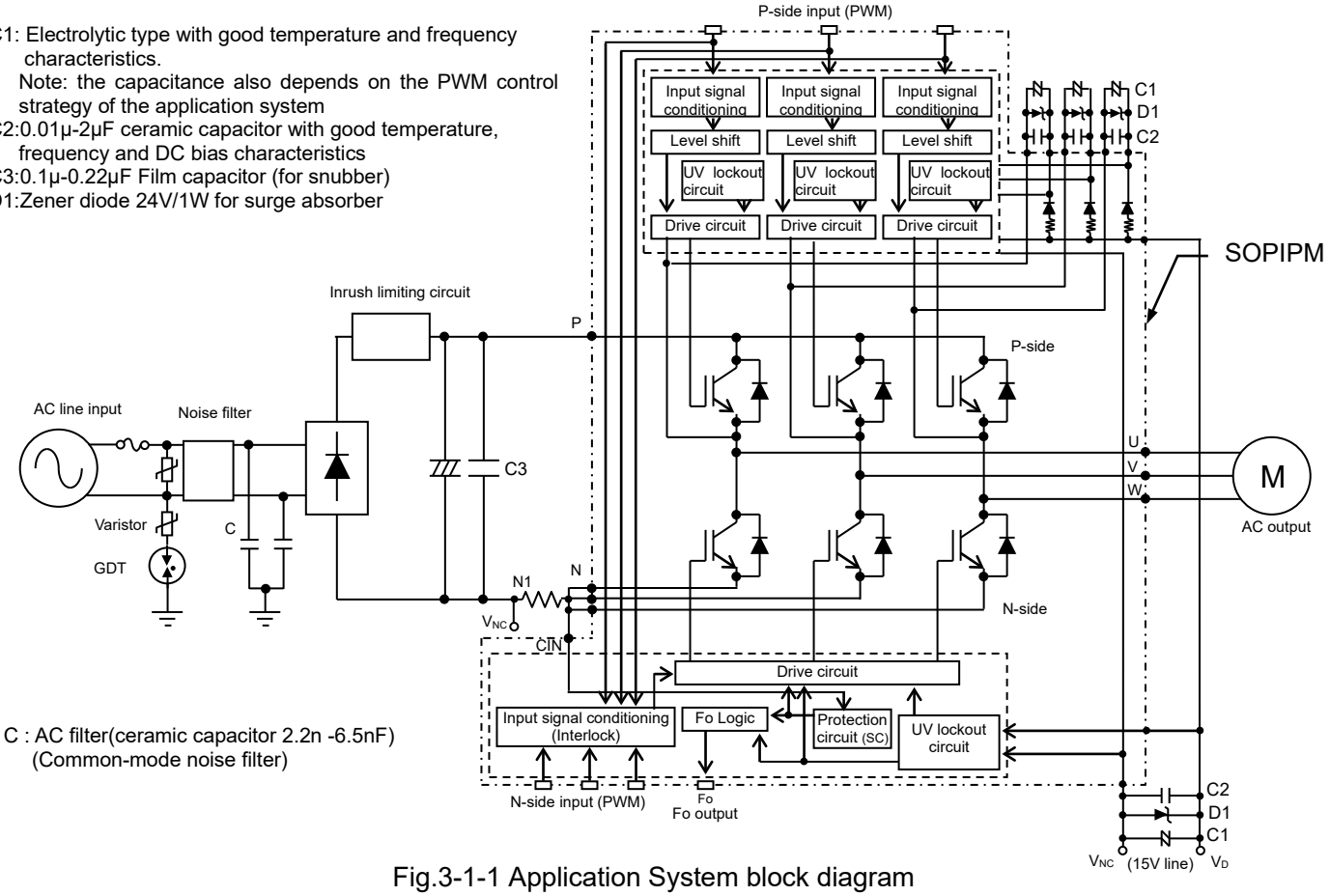
CHAPTER 3 SYSTEM APPLICATION GUIDANCE

3.1 Application Guidance

This chapter states the SOPIPM application method and interface circuit design hints.

3.1.1 System connection

C1: Electrolytic type with good temperature and frequency characteristics.
Note: the capacitance also depends on the PWM control strategy of the application system
C2:0.01μ-2μF ceramic capacitor with good temperature, frequency and DC bias characteristics
C3:0.1μ-0.22μF Film capacitor (for snubber)
D1:Zener diode 24V/1W for surge absorber



C : AC filter(ceramic capacitor 2.2n -6.5nF)
(Common-mode noise filter)

Fig.3-1-1 Application System block diagram

3.1.2 Interface Circuit (Direct Coupling Interface example for using one shunt resistor)

Fig.3-1-2 shows a typical application circuit of interface schematic, in which control signals are transferred directly input from a controller (e.g. MCU, DSP).

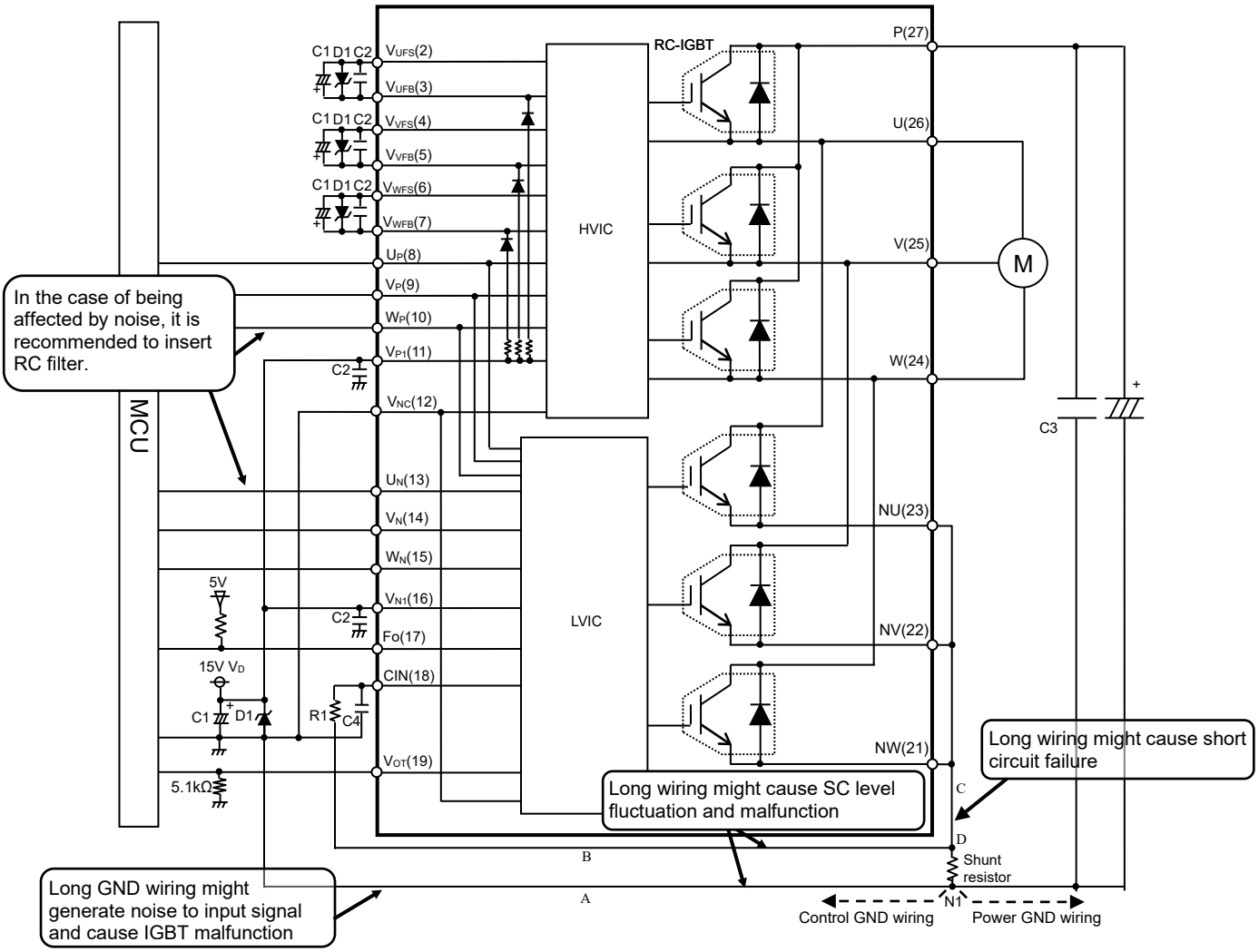


Fig.3-1-2 Interface circuit example in the case of direct input from a controller

Note:

(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).

(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.

(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.

(5) The wiring of A, B, C affect IGBT operation. Wring B and C should be as short as possible to prevent malfunction. Wring A should design with some length according to the wring route in the power part. By designing the wring A with enough high impedance against the power wring, it is possible to prevent wraparound of short-circuit current to the control side.

(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.

(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.01μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(8) Input drive is High-active type. There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(9) Thanks to built-in HVIC, direct coupling to MCU without any optocoupler or transformer isolation is possible.

(10) Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)

(11) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause SOPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.

3.1.3 Interface Circuit (Example of Opto-coupler Isolated Interface)

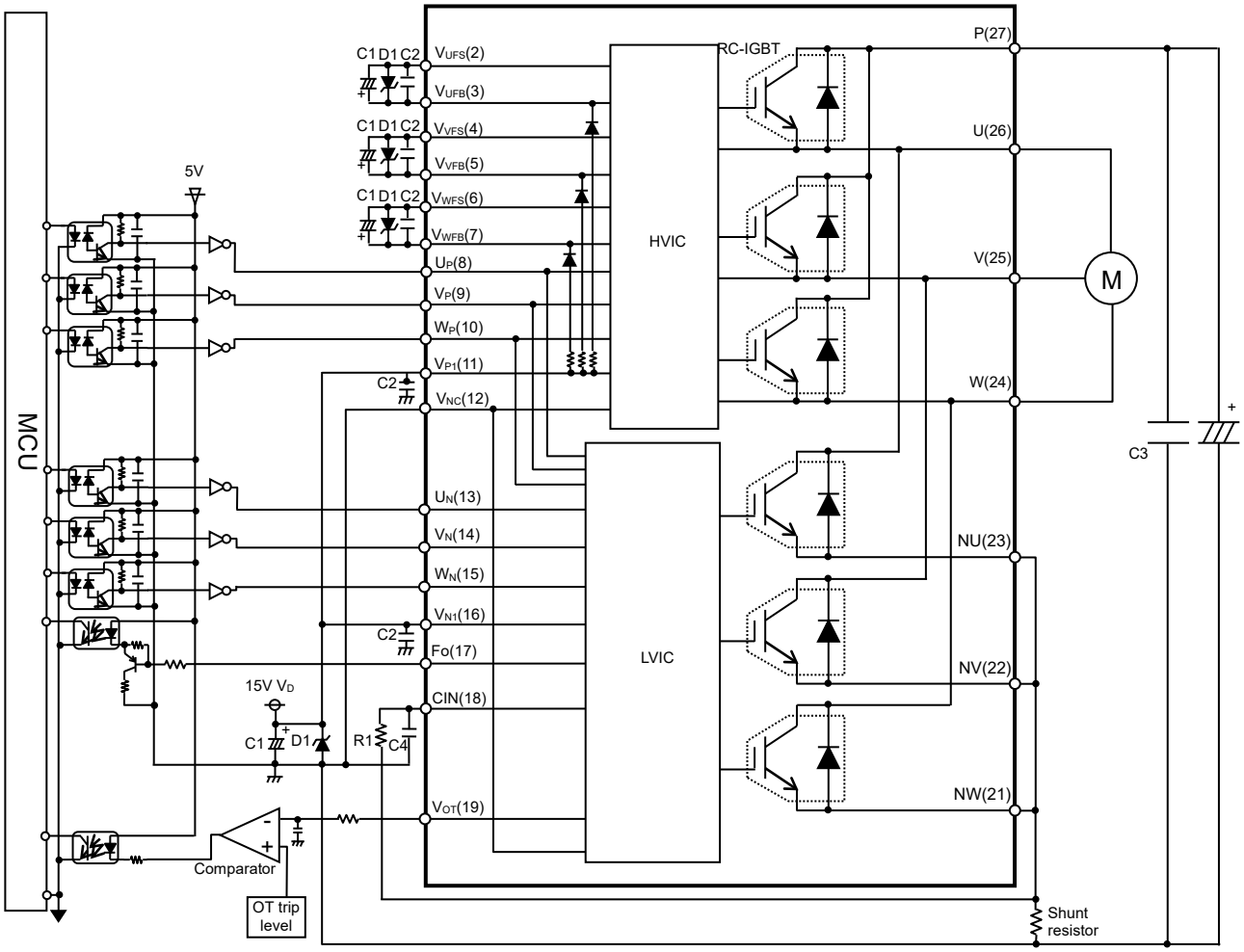


Fig.3-1-3 Interface circuit example with opto-coupler

Note:

(1) High speed (high CMR) opto-coupler is recommended.

(2) Fo terminal sink current for inverter part is max.1mA.

(3) About comparator circuit at V_{OT} output, it is recommended to design the input circuit with hysteresis to prevent output chattering.

(4) In the case that input signal to SOPIPM is affected by noise, it is recommended to insert RC filter. When using RC filter, make sure the input signal level meet the turn-on and turn-off threshold voltage. (There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC.)

3.1.4 External SC Protection Circuit with Using Three Shunt Resistors

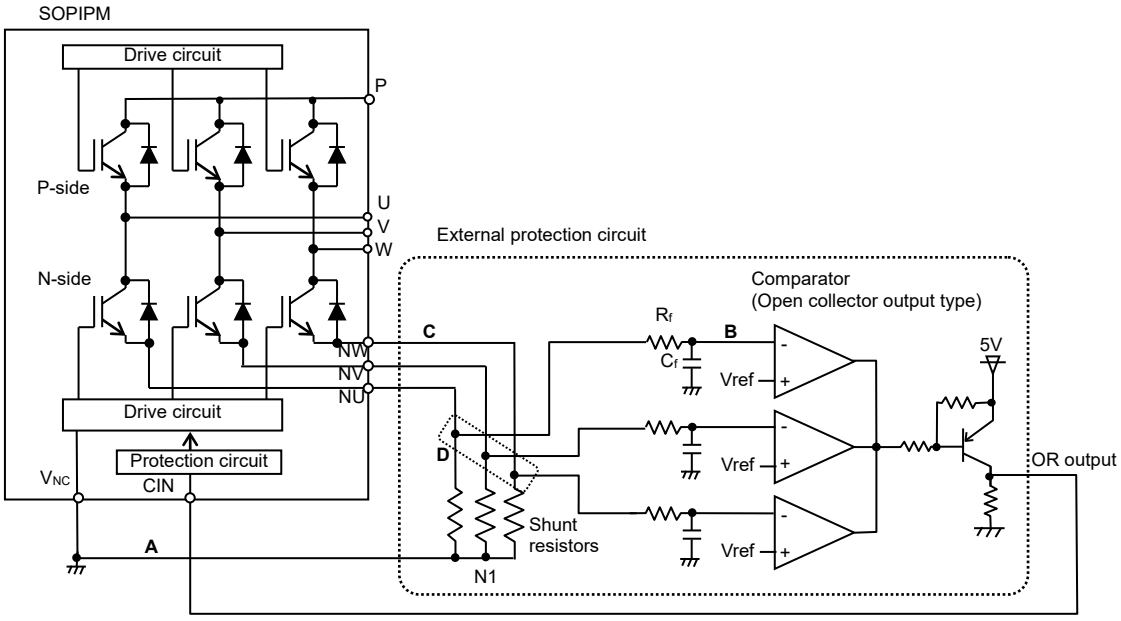


Fig.3-1-4 Interface circuit example

Note:

(1) It is necessary to set the time constant R_fC_f of external comparator input so that IGBT stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.480V).
(3) Select the external shunt resistance so that SC trip-level is less than specified value.
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
(6) OR output high level should be over 0.505V (=maximum Vsc(ref)).
(7) GND of Comparator, Vref circuit and Cf should be connected to control GND wiring, not to noisy power GND.

3.1.5 Circuits of Signal Input Terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

SOPIPM is high-active input logic.
A 3.3kΩ(min) pull-down resistor is built-in each input circuits of the SOPIPM as shown in Fig.3-1-5 , so external pull-down resistor is not needed.
Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 3-1-1, a direct coupling to low voltage microcomputer or DSP becomes possible.

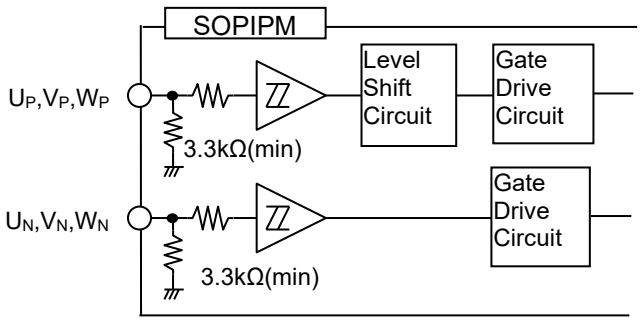


Fig.3-1-5 Internal structure of control input terminals

Table 3-1-1 Input threshold voltage ratings(Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{NC} terminals U_N,V_N,W_N-V_{NC} terminals	-	1.70	2.35	V
Turn-off threshold voltage	Vth(off)		0.70	1.30	-	
Threshold voltage hysterisis	Vth(hys)		0.25	0.40	-	

Note: There are specifications for the minimum input pulse width in SOPIPM. SOPIPM might make no response if the input signal pulse width (both on and off) is less than the specified value. Please refer to the datasheet for the specification.

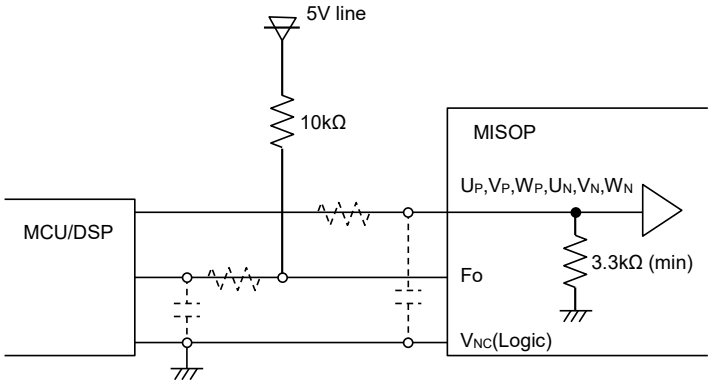


Fig.3-1-6 Control input connection

Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.
The SOPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type, it should be pulled up to a 5V supply as shown in Fig.3-1-6. Fig.3-1-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA. If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-1-2 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V, Fo=10kΩ, 5V pulled-up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V, Fo=1mA	-	-	0.95	V

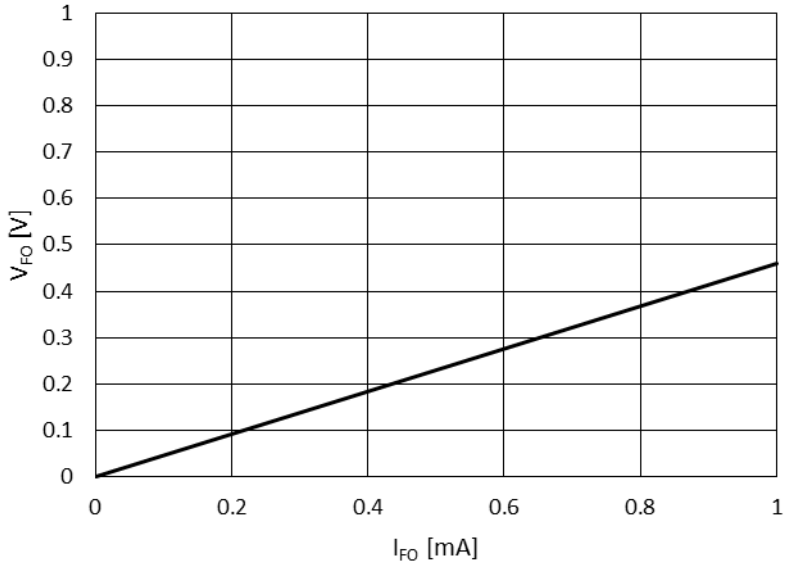


Fig.3-1-7 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.6 Snubber Circuit

In order to prevent SOPIPM from destruction by extra surge, the wiring length between the smoothing capacitor and SOPIPM P terminal - N1 points (shunt resistor terminal) should be as short as possible. Also, a 0.1μ~0.22μF / 630V snubber capacitor should be mounted in the DC-link and near to P, N1.

There are two positions ((1)or(2)) to mount a snubber capacitor as shown in Fig.3-1-8. Snubber capacitor should be installed in the position (2) so as to suppress surge voltage effectively. However, the charging and discharging currents generated by the wiring inductance and the snubber capacitor will flow through the shunt resistor, which might cause erroneous protection if this current is large enough.

In order to suppress the surge voltage maximally at position (1), the wiring at part-A (including shunt resistor parasitic inductance) should be as small as possible. A better wiring example is shown in location (3).

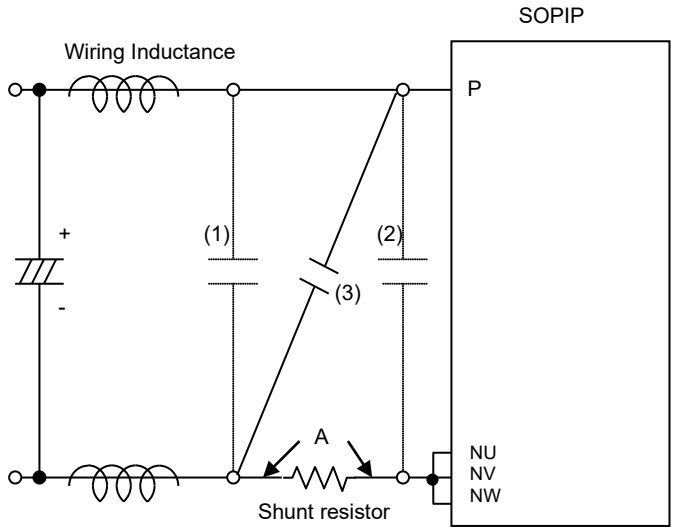


Fig.3-1-8 Recommended snubber circuit location

3.1.7 Recommended Wiring Method around Shunt Resistor

External shunt resistor is employed to detect short-circuit accident. A longer wiring between the shunt resistor and SOPIPM causes so much large surge that might damage built-in IC.

To decrease the pattern inductance, the wiring between the shunt resistor and SOPIPM should be as short as possible and using low inductance type resistor such as SMD resistor instead of long-lead type resistor.

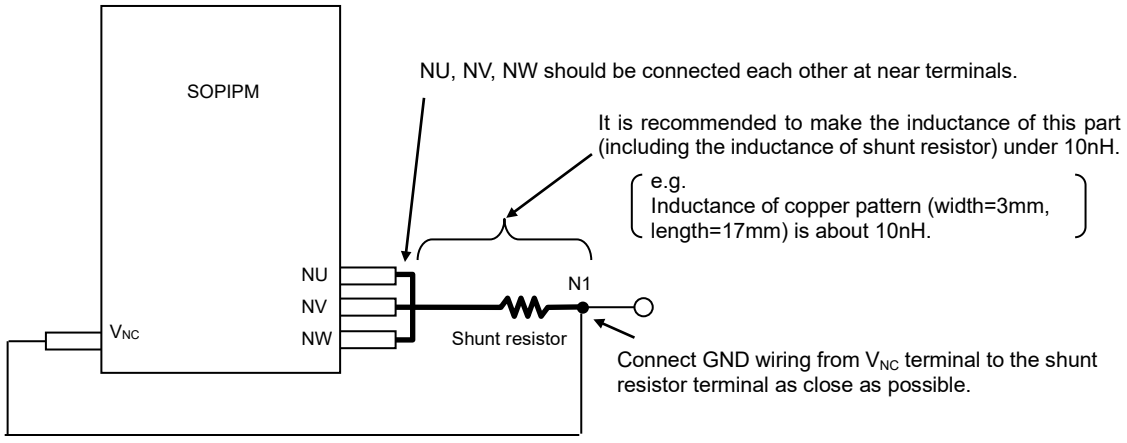


Fig.3-1-9 Wiring instruction (In the case of using with one shunt resistor)

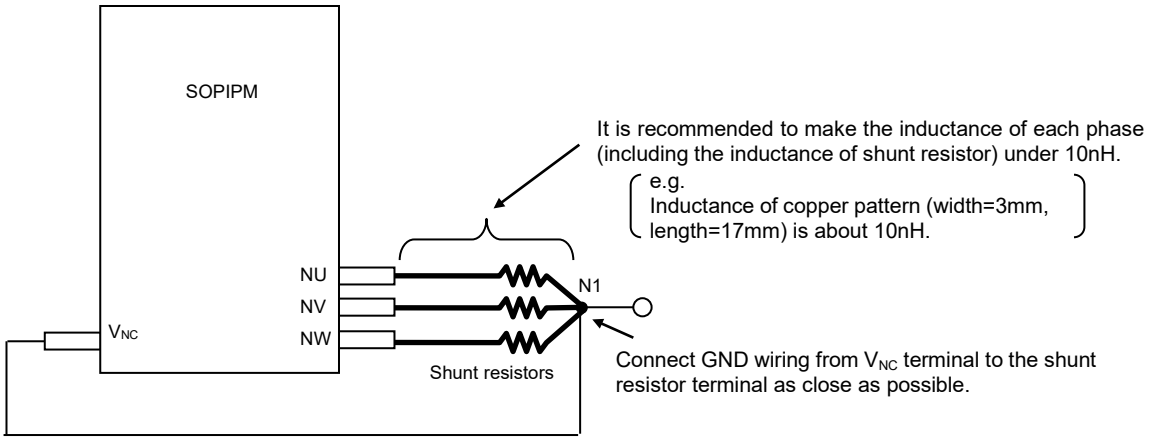


Fig.3-1-10 Wiring instruction (In the case of using with three shunt resistor)

Influence of pattern wiring around the shunt resistor is shown below.

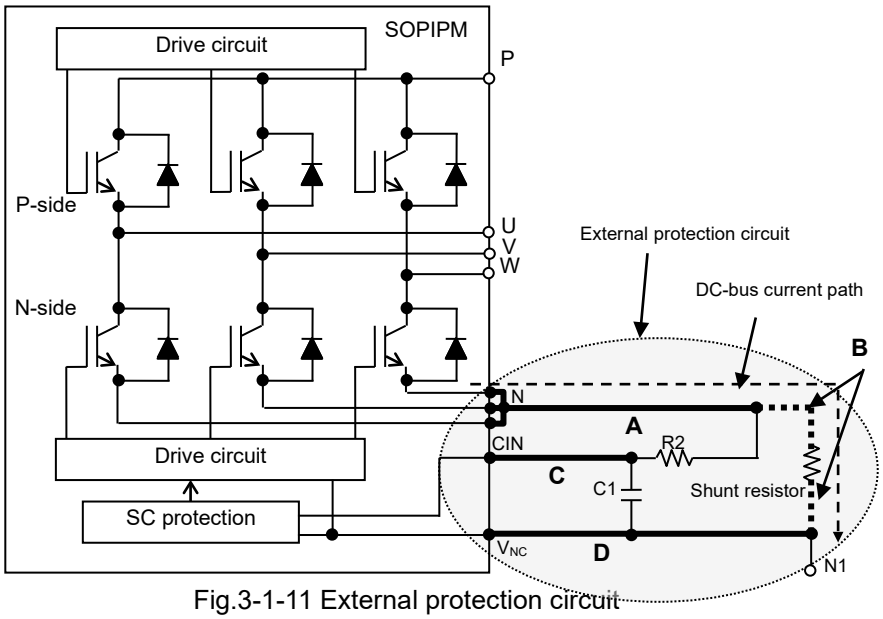


Fig.3-1-11 External protection circuit

(1) Influence of the part-A wiring

The ground of N-side IGBT gate is V_{NC}. If part-A wiring pattern in Fig.3-1-11 is too long, extra voltage generated by the wiring parasitic inductance will result the potential of IGBT emitter variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring affects SC protection level. SC protection works by detecting the voltage of the CIN terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. It is necessary to connect CIN and V_{NC} terminals directly to the two ends of shunt resistor and avoid long wiring.

(3) Influence of the part-C wiring pattern

C1R2 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring is too long. It is necessary to install the C1R2 filter near CIN, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected.

3.1.8 Precaution for Wiring on PCB

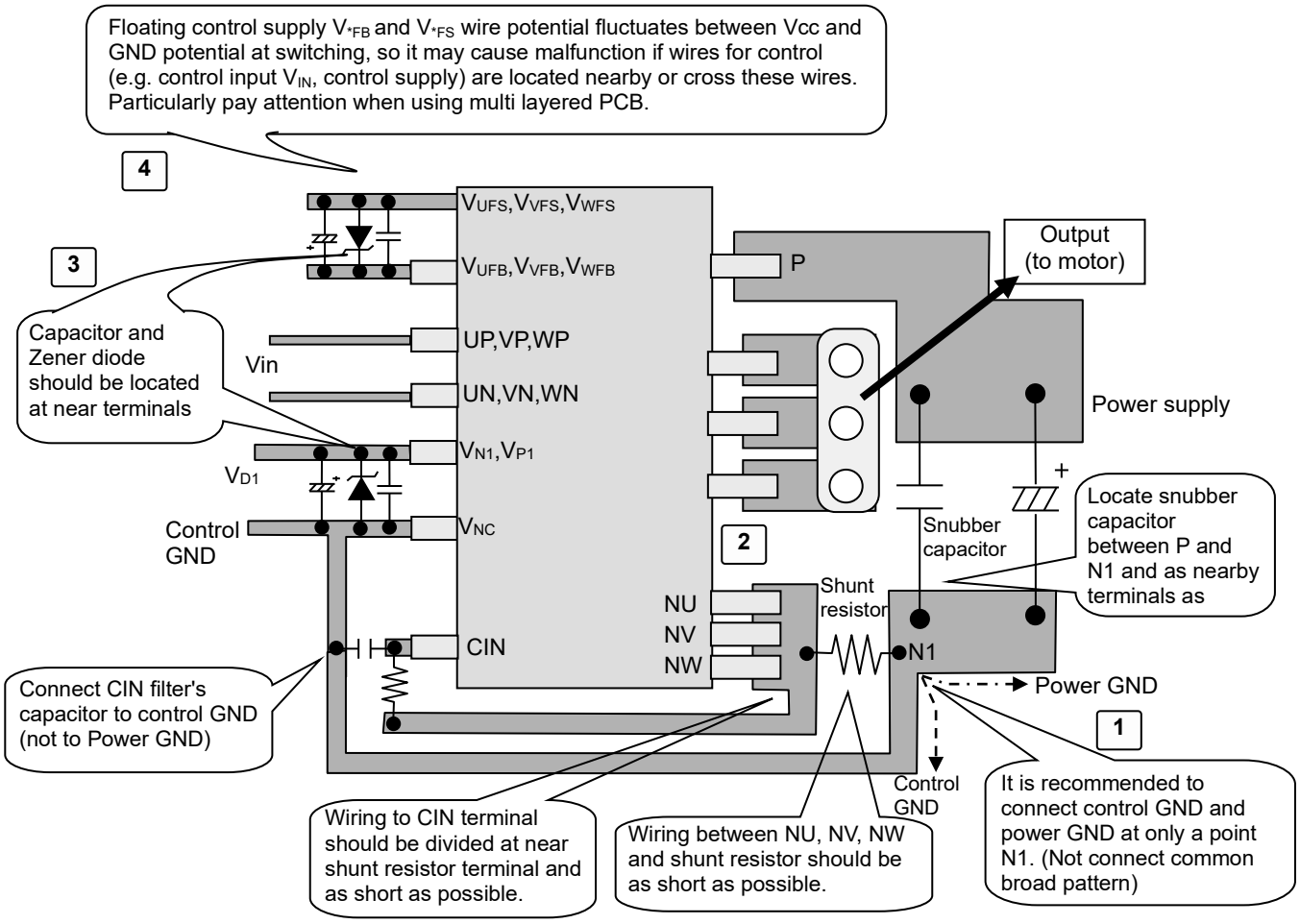


Fig.3-1-12 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Then the arm short might occur.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short might occur.
2	•Large inductance of wiring between N and N1 terminal	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction might occur.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to SOPIPM. Then incorrect signals are input to SOPIPM input, and arm short (short circuit) might occur.

3.1.9 SOA of SOPIPM

The following describes the SOA (Safety Operating Area) of the SOPIPM. (Not specified)

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: Total amount of V_{CC} and surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(PROT)}$: DC-link voltage that SOPIPM can protect itself.

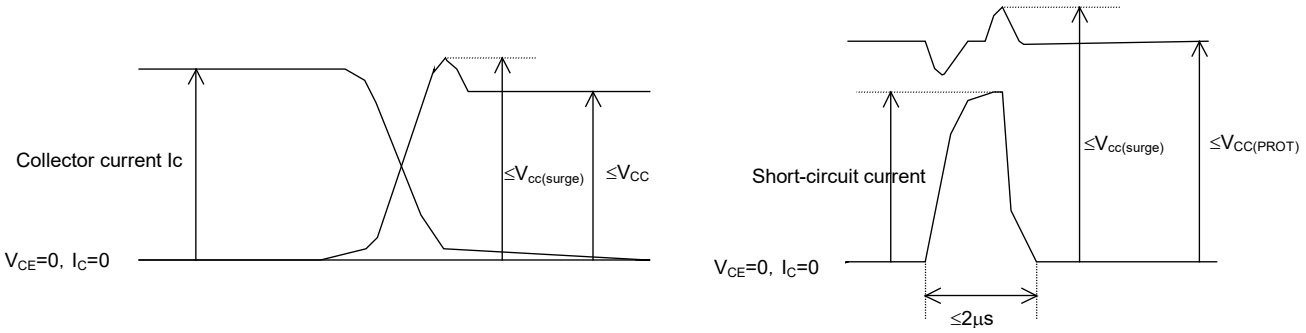


Fig.3-1-13 SOA at switching mode and short-circuit mode

In Case of switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between SOPIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC}, that is 450V.

In Case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the SOPIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC}, that is, 400V.

3.1.10 SCSOA

Fig.3-1-14 shows the typical SCSOA performance curves of SP2SK.

(Conditions: V_{cc}=400V, T_j=125°C at initial state, Vcc(surge)≤500V(surge included), non-repetitive,2m load.)

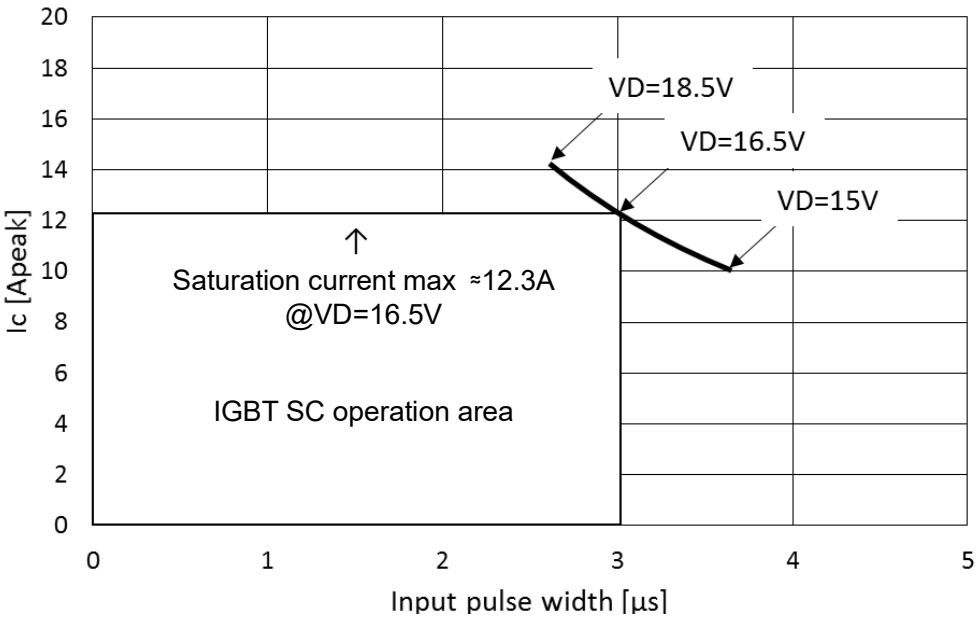


Fig.3-1-14 Typical SCSOA curve of SP2SK

3.1.12 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happens on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-1-15 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj).

(The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

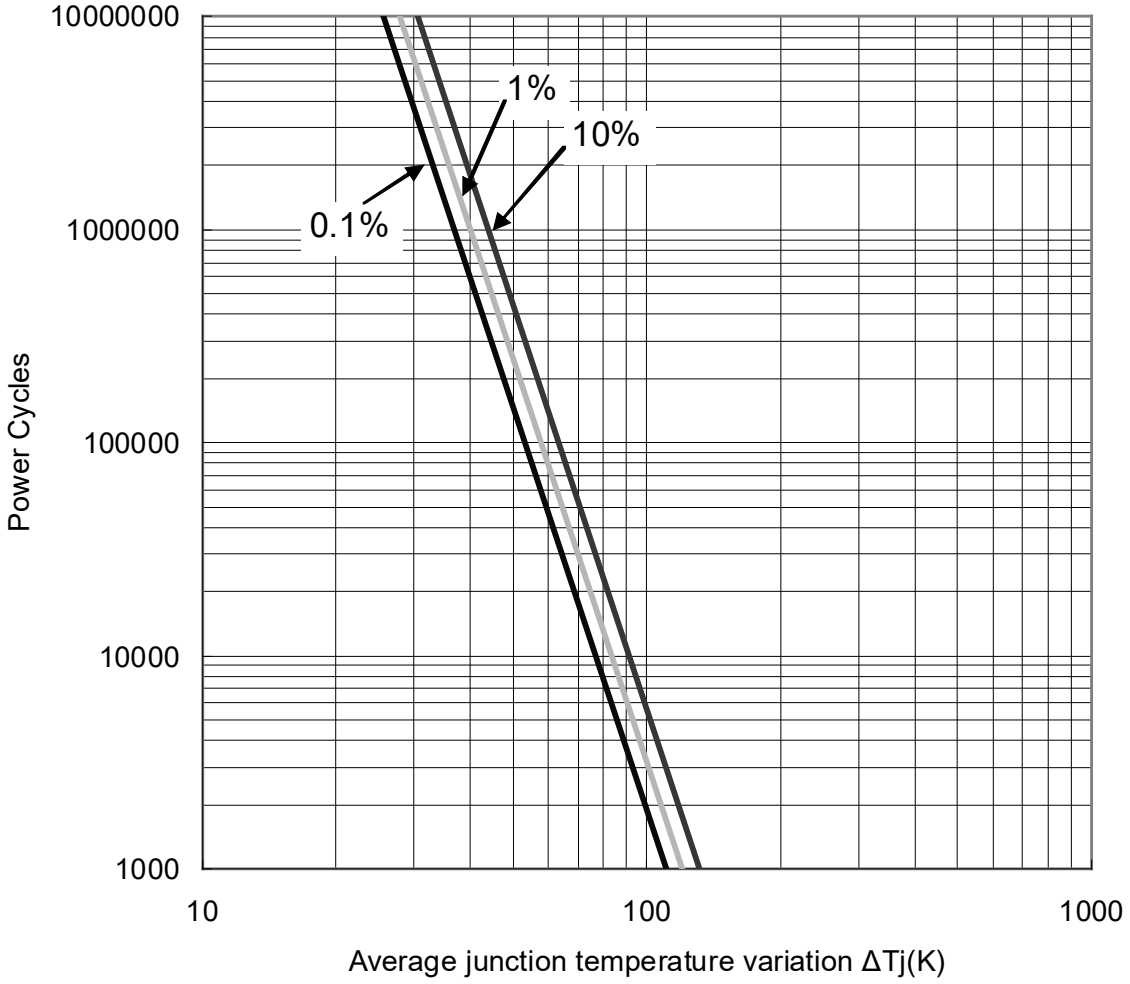


Fig.3-1-15 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

As SOPIPM applies RC-IGBT which integrates IGBT and FWD on one chip die, it is necessary for loss and temperature estimation to consider the sum of IGBT and FWD losses.

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$

$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\, Icp \times \sin x)$$
$$Vec = (-1) \times Vec(@\, Iecp(= Icp) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Icp \times \sin x) \times Vce(sat)(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} ((-1) \times Icp \times \sin x)((-1) \times Vec(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Psw(on)(@\, Icp \times \sin x) + Psw(off)(@\, Icp \times \sin x)) \times fc \bullet dx$$

FWD recovery characteristics can be approximated by the ideal curve shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

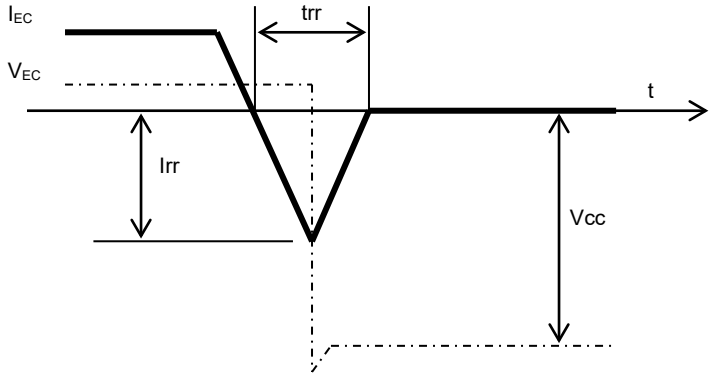


Fig.3-2-1 Ideal FWD recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x)}{4} \times fc \bullet dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at Tj=125°C.

3.2.2 Allowable motor current *WITHOUT heatsink operation*

Without heatsink operation, the junction temperature rise should be calculated by the module total loss and the junction to ambient thermal resistance Rth(j-a). So its allowable inverter operating loss should be determined from its ambient temperature Ta.

As examples, when operating SP2SK at the ambient temperature Ta=60ºC, its typical allowable total loss can be calculated as the following formula.

Allowable total loss=(125ºC-60ºC)/31K/W=2.09W
(T_j=125ºC; Recommended max. junction temperature, $R_{th(j-a)\_Q}$=31K/W; rating value)

Based on the above allowable total loss, the allowable motor current should be obtained.

Table.3-2-1 shows the typical allowable motor current in major control methods when operating SP2SK at the carrier frequency fc=20kHz.

Table.3-2-1 Relationship between the control method and allowable output current for SP2SK (Typical)
(Condition: V_{CC}=300V, Vo=184Vrms, V_D=V_{DB}=15V, P.F=0.8, M=1, Typical characteristics@T_j=125ºC, fo=60Hz, fc=20kHz, $R_{th(j-a)}$=31K/W, Ta=60ºC or 75ºC)

Control method	Ta=60ºC (Allowable total loss=2.09W)	Ta=75ºC (Allowable total loss=1.61W)
3-phase modulation	0.21Arms	0.14Arms
SVPWM	0.21Arms	0.13Arms
2-phase modulation	0.32Arms	0.23Arms
2-phase modulation (Ⅱ)	0.30Arms	0.21Arms

The actual junction to ambient thermal resistance $R_{th(j-a)}$ varies depending on its ambient environment; such as its PCB pattern, its cooling conditions, and so on.

Please refer Chapter 3.2.4 for typical motor current vs. module total loss of SP2SK.

3.2.3 Allowable motor current *WITH heatsink operation*

Fig.3-2-2 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{CC}=300V, Vo=184Vrms, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., Switching loss=Typ., Tj=125°C, Tc=100°C, $R_{th(j-c)}$=Max., P.F=0.8, M=1, 3-phase PWM modulation, 60Hz sine waveform output

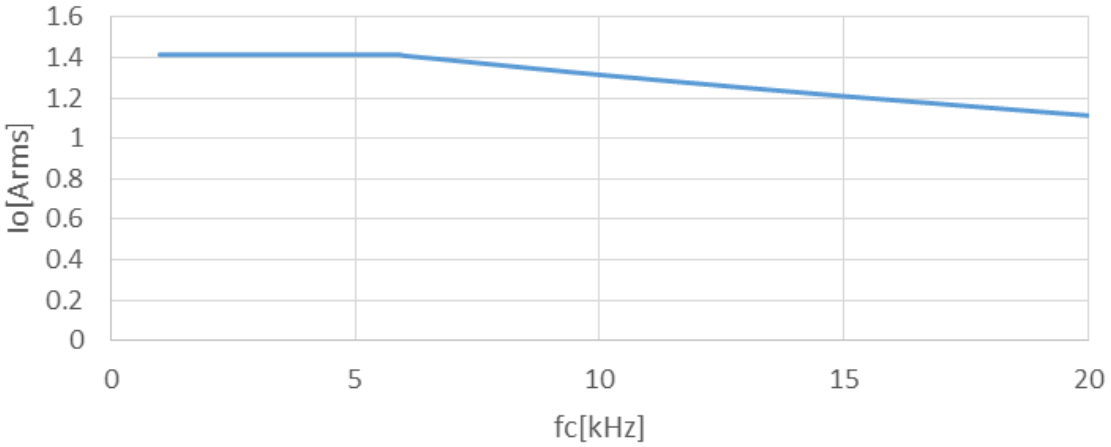


Fig.3-2-2 Effective current-carrier frequency characteristics (Typical)

Fig.3-2-2 shows an example of estimating allowable inverter output rms current under different carrier frequency and recommended average maximum junction temperature Tj=125ºC at Tc=100°C. The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

3.2.4 Carrier frequency characteristics for Total loss vs. Motor current

Fig.3-2-3~6 show the typical carrier frequency dependency of module total loss versus motor rms current under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{CC}=300V, Vo=184Vrms, V_D=V_{DB}=15V, P.F=0.8, M=1, fo=60Hz, fc=5~20kHz,
Typical characteristics@Tj=125ºC

(a) 3-phase modulation control

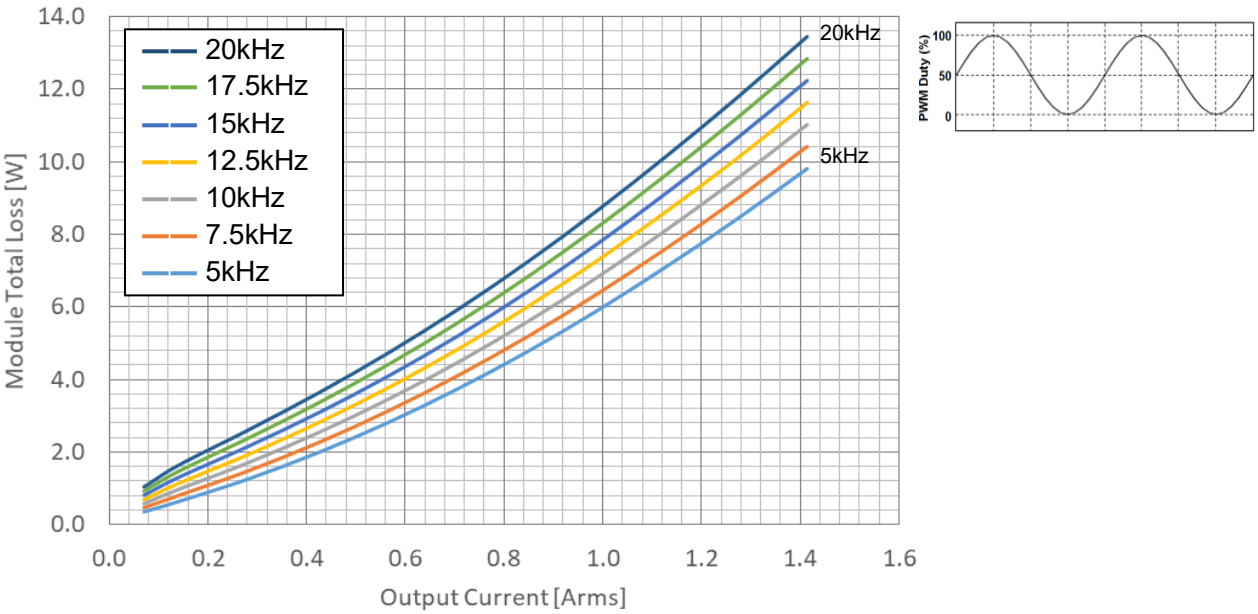


Fig.3-2-3 Carrier frequency characteristics for Total loss vs. Motor current (3-phase modulation control)

(a) SVPWM

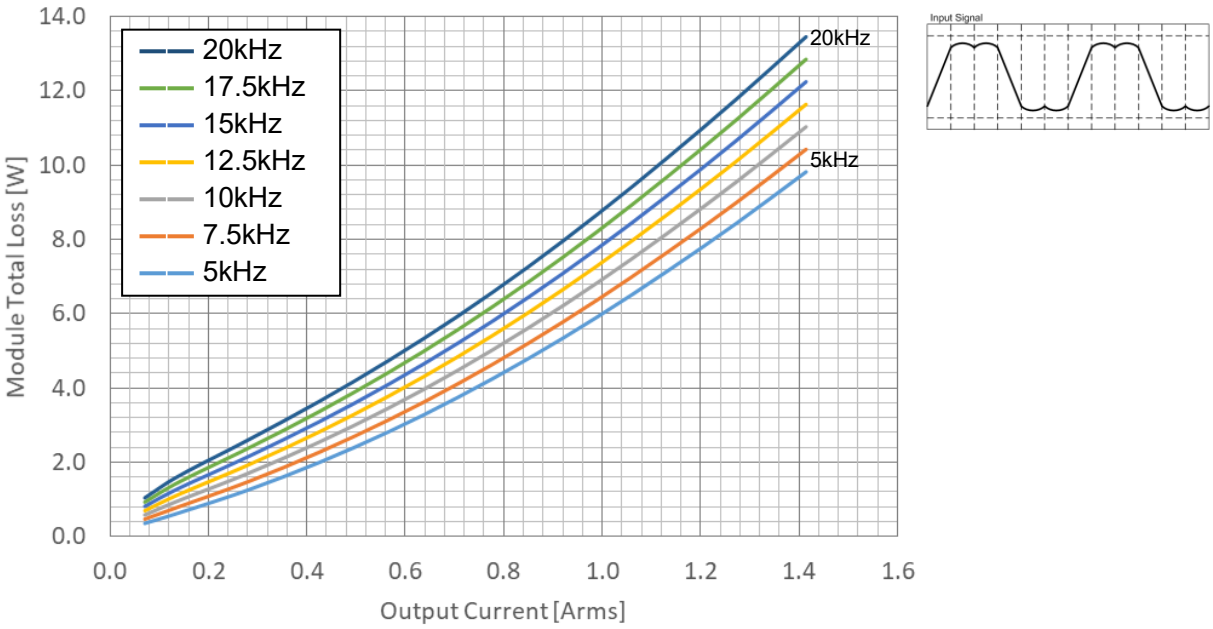


Fig.3-2-4 Carrier frequency characteristics for Total loss vs. Motor current (SVPWM)

(c) 2-phase modulation control

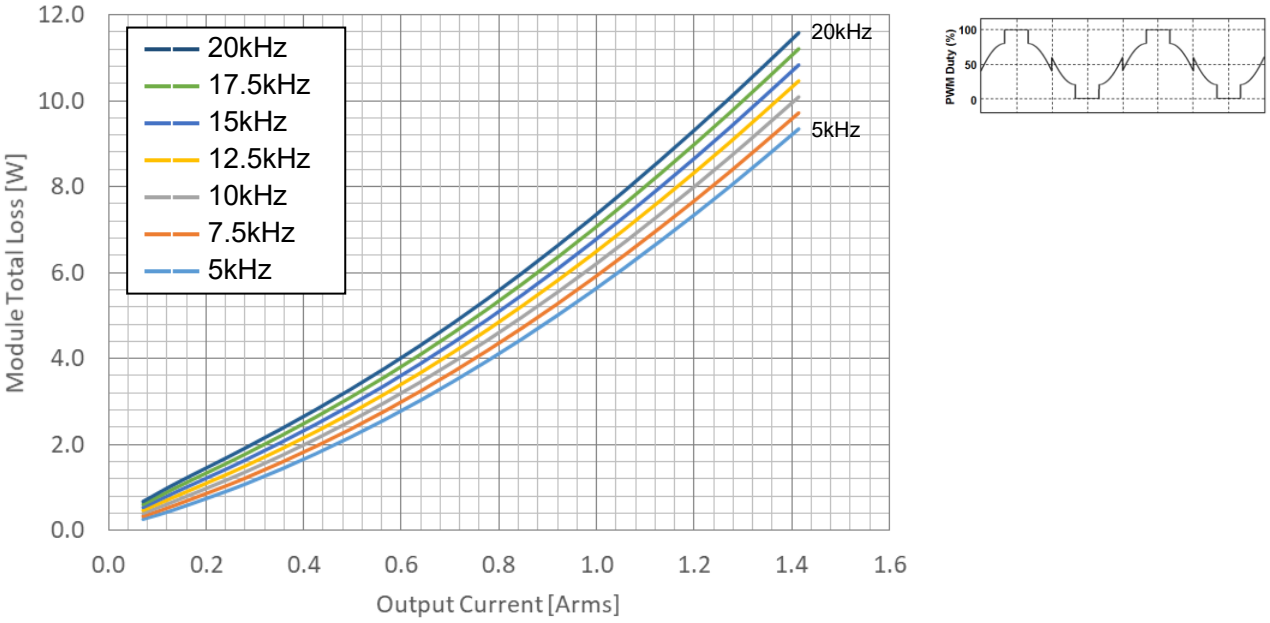


Fig.3-2-5 Carrier frequency characteristics for Total loss vs. Motor current (2-phase modulation control)

(d) 2-phase modulation control(Ⅱ)

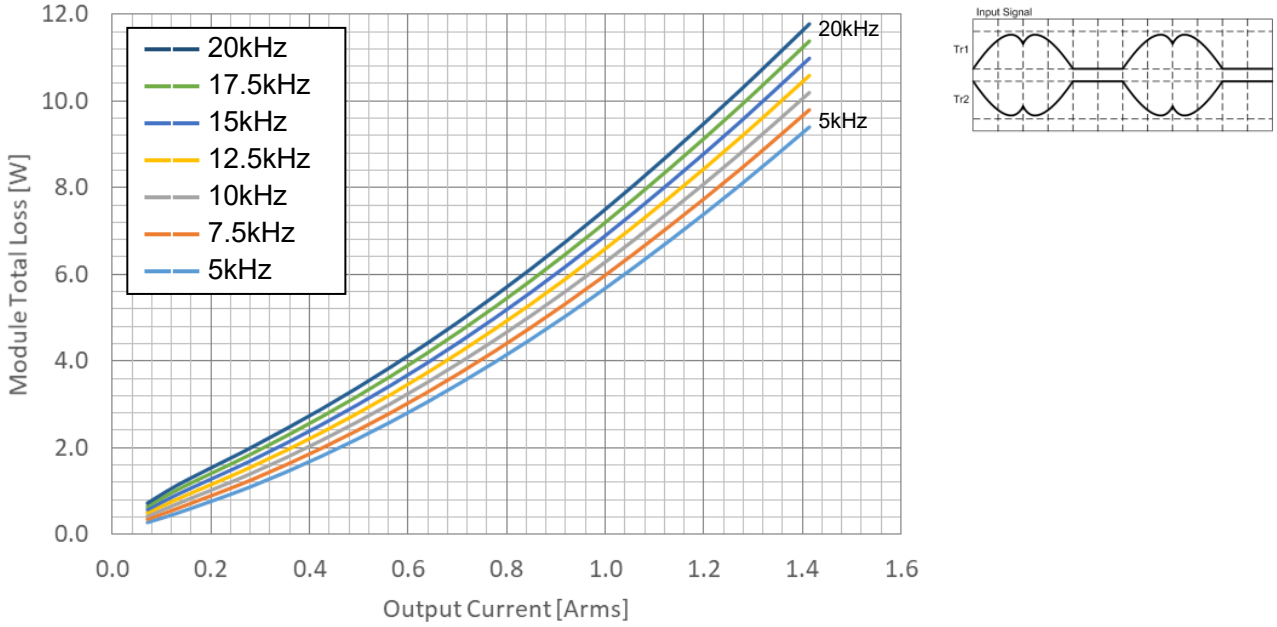


Fig.3-2-6 Carrier frequency characteristics for Total loss vs. Motor current (2-phase modulation control(Ⅱ))

3.2.5 Installation of thermocouple for case temperature monitoring

When operating SOPIPM with a heatsink, its thermal rise should be considered with its power loss, its case temperature Tc and its Junction to case thermal resistance Rth(j-c)Q. It is necessary to mount a thermocouple on the heatsink surface at the defined position to get accurate temperature information.

For measurement of SOPIPM case temperature, installing point of thermocouple in the heatsink is shown in Fig.3-2-7. Tc (case temperature) is defined to be the temperature at center of the case at RC-IGBT chip mounting position.

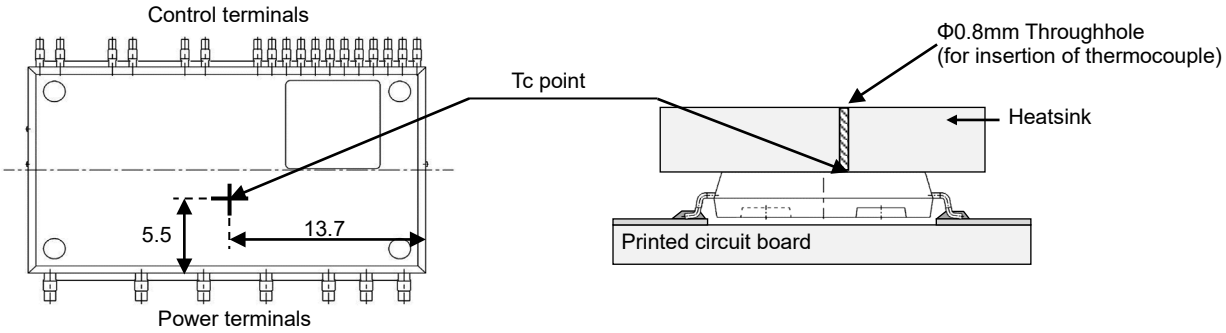


Fig. 3-2-7 Point for installing thermocouple in external heat sink

Installation of thermocouple is shown in Fig. 3-2-8. After making a hole under the chip with largest loss into the heat sink, the thermocouple is inserted in this hole and fixed by hammering around the hole with a centerpunch. After fixing the thermocouple, please sandpaper the thermocouple installing surface to make flat surface.

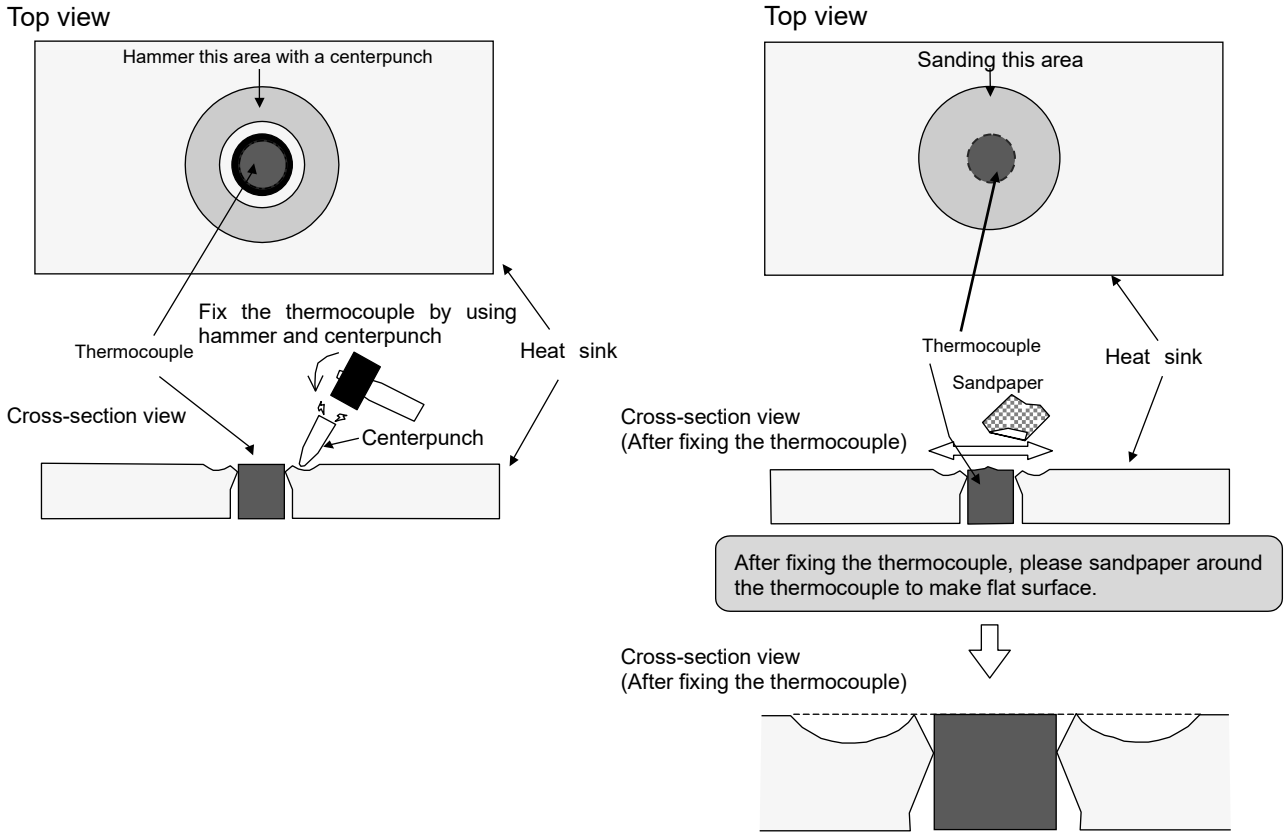


Fig. 3-2-8 Example of installation of thermocouple

3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

SOPIPM series will be confirmed to be with over +/- 2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-3-1. Noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

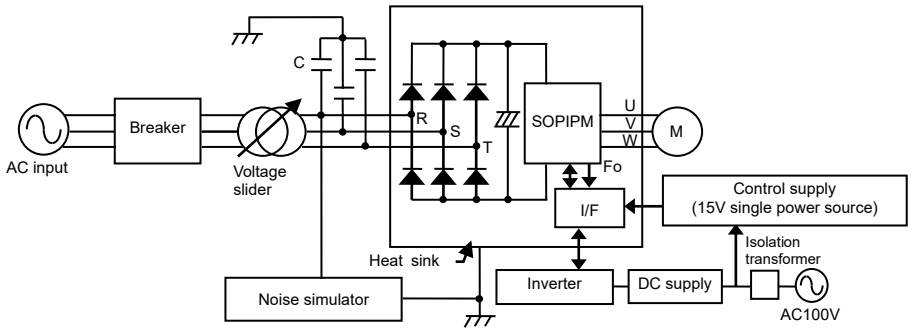


Fig.3-3-1 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using optocouplers, 15V single power supply, Test is performed with IM

Test conditions

V_{CC}=300V, V_D=15V, Ta=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

3.3.2 Countermeasures and Precautions

SOPIPM series improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of SOPIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, below countermeasures are recommended.

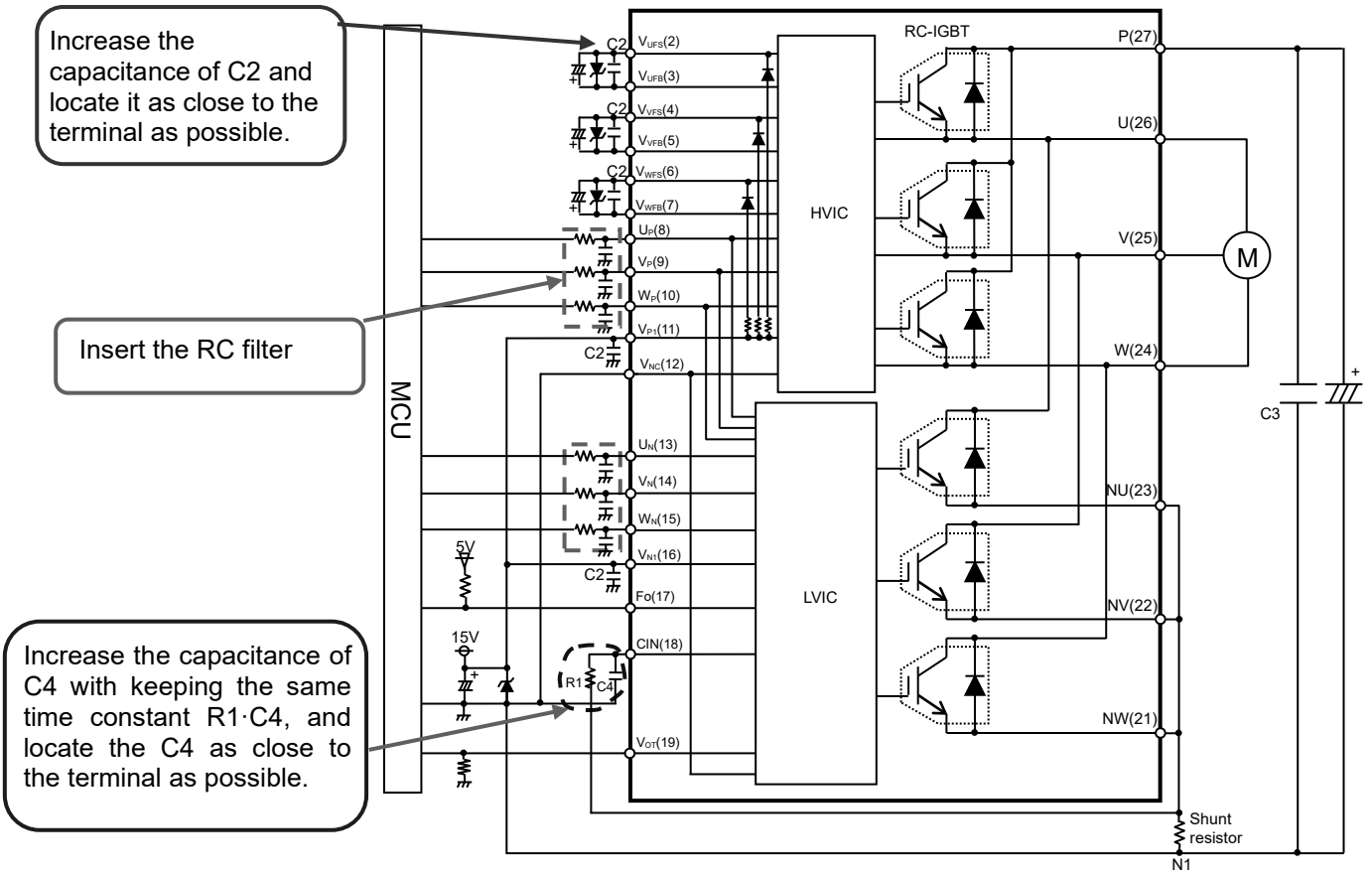


Fig.3-3-2 Example of countermeasures for inverter part

3.3.3 Static Electricity Withstand Capability

SOPIPM series have been confirmed to be with over +/- 1kV static electricity withstand capability.

Test method of static electricity withstand capability by HBM(R=1.5kΩ, C=100pF) is described as below. Surge voltage increases by 0.1kV step and three surge pulses are impressed at each surge voltage. (Limit voltage of surge simulator: ±4.0kV, Judged by change in V-I characteristic)

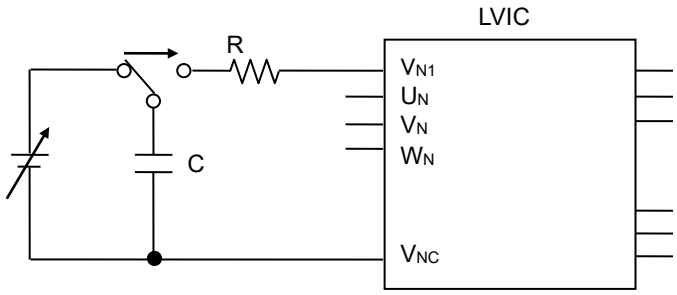


Fig.3-3-3 LVIC terminal Surge Test circuit

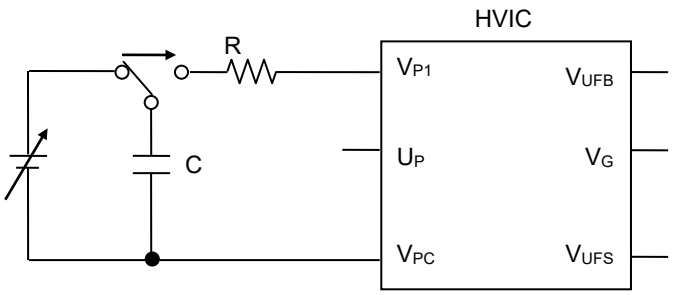


Fig.3-3-4 HVIC terminal Surge Test circuit

CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor. (SOPIPM series integrates BSD and limiting resistor and can make bootstrap circuit by adding outer BSC only.) It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC (Fig.4-1-2). Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIPM and SOPIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, please refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

The BSD characteristics for SOPIPM series and the circuit current characteristics in switching situation of P-side IGBT are described as below.

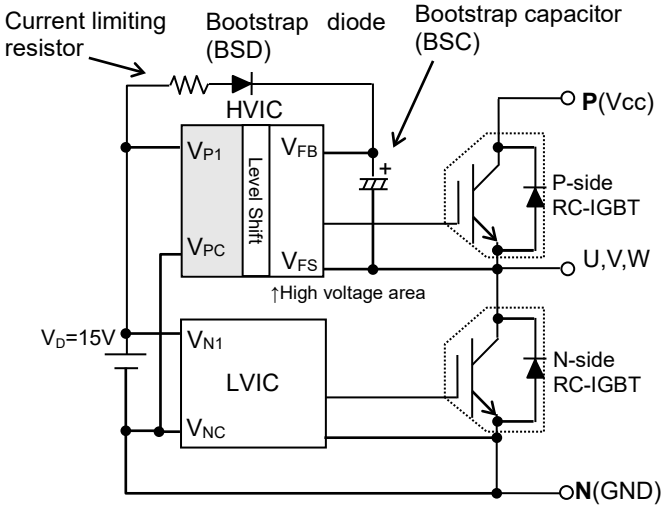


Fig.4-1-1 Bootstrap Circuit Diagram

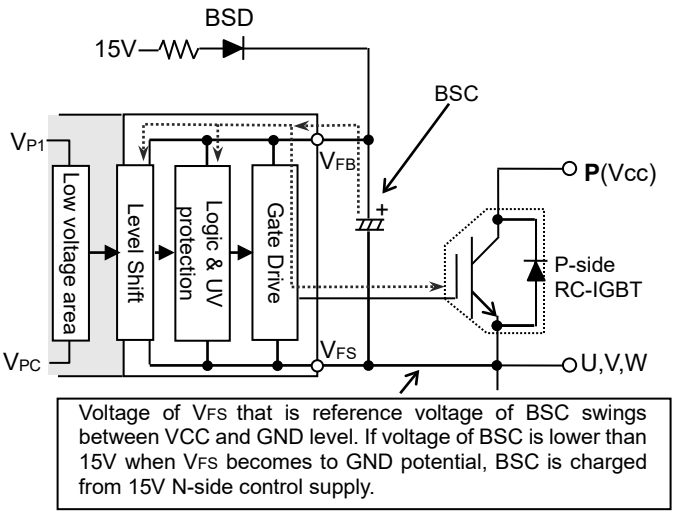


Fig.4-1-2 Bootstrap Circuit Diagram

4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 0.1mA. But at switching state, because gate charge and discharge are repeated by every switching, the circuit current exceeds 0.1mA and increases proportional to carrier frequency. For reference, Fig.4-2-1 shows typical I_{DB} - carrier frequency fc characteristics for each current rating product.

Conditions: V_D=V_{DB}=15V, Vcc=450V, Tj=125°C at which I_{DB} becomes larger

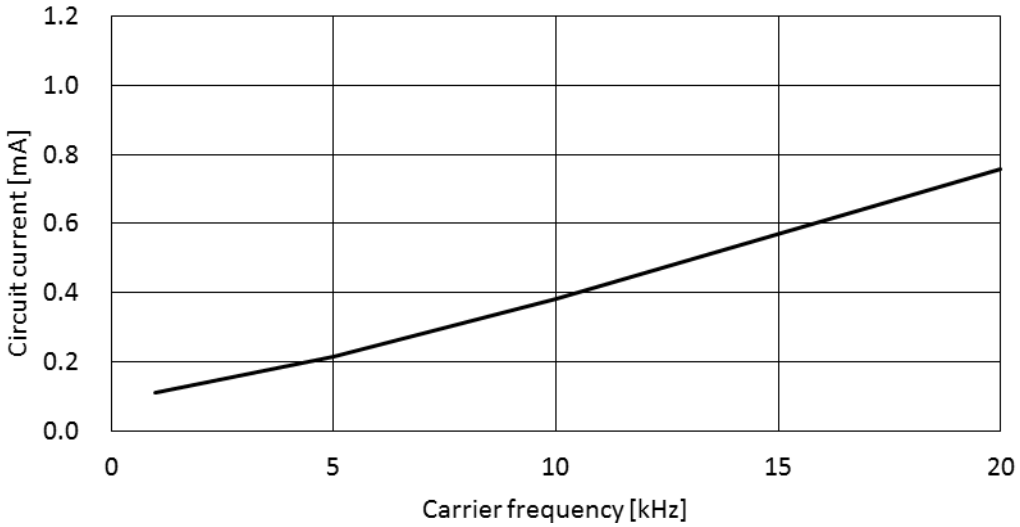


Fig.4-2-1 I_{DB} vs. Carrier frequency for SP2SK

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, please refer the SOPIPM application note "*Bootstrap Circuit Design Manual*"

(1) Bootstrap capacitor

Electrolytic capacitors are generally used for BSC, and ceramic capacitors with large capacitance are also applied recently. But it is necessary to note DC bias characteristic of the ceramic capacitor, especially large capacitance type; when applying DC voltage, it is considerably different from that of electrolytic capacitor. Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-3-1.

Table 4-3-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	•Aluminum type: Low temp.: -10% High temp: +10% •Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on **-70%**~-15%

Electrolytic capacitors have good DC bias characteristic; however it is necessary to note its ripple capability by repetitive charge and discharge, its life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

SOPIPM integrates bootstrap diode for P-side driving supply. This BSD incorporates current limiting resistor. The V_F-I_F characteristics (including voltage drop by built-in current limiting resistor) is shown in Fig.4-3-1 and Table 4-3-2.

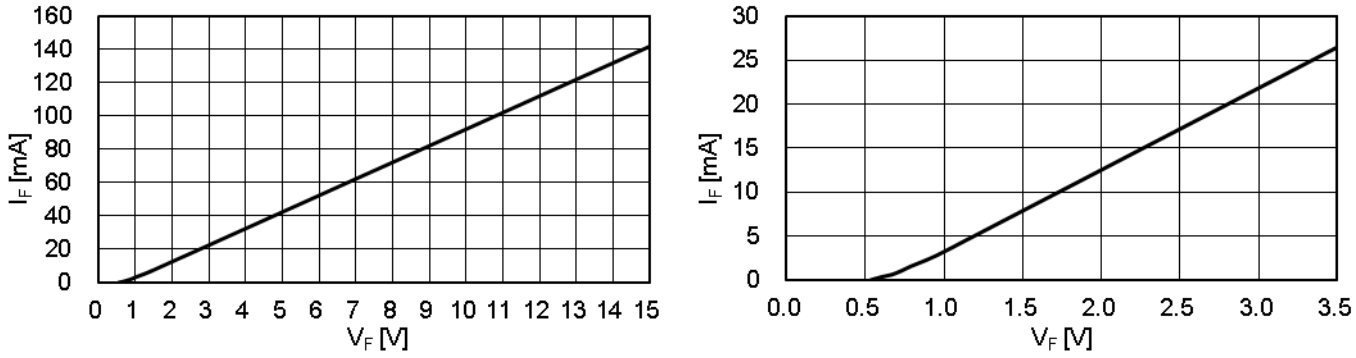


Fig.4-3-1 V_F-I_F curve for bootstrap Diode (typical, the right figure is enlarged view)

Table 4-3-2 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	I_F=10mA including voltage drop by limiting resistor	1.1	1.7	2.3	V
Built-in limiting resistance	R	Included in bootstrap Di	80	100	120	Ω

4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the SOPIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and so on.

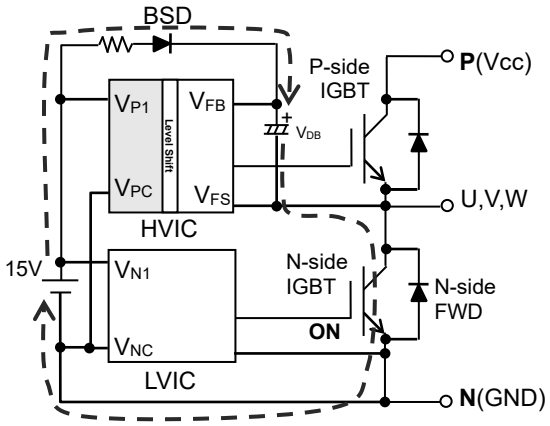


Fig.4-4-1 Initial charging root

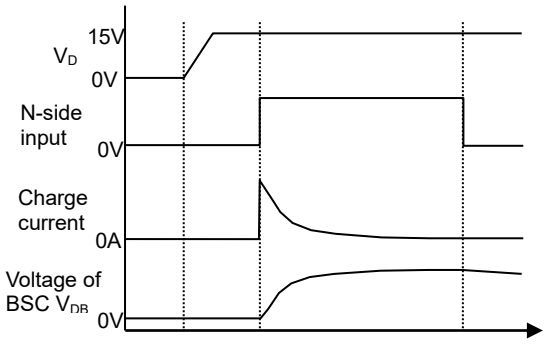


Fig.4-4-2 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (e.g. 0.7μs or more for SP2SK. Please refer the datasheet for each product.)

CHAPTER 5 PACKAGE HANDLING

5.1 Packaging Specification

SOPIPM series are shipped in moisture proof packing with desiccant agent to avoid moisture absorption. The packing specification is as below. Please also refer Chapter 2.4.2 about the storage deadlines in the moisture-proof packing state and after opening the packing state.

The schematic diagrams of the embossed carrier tape and tape reel are shown in Figures 5-1-1 and 5-1-2.

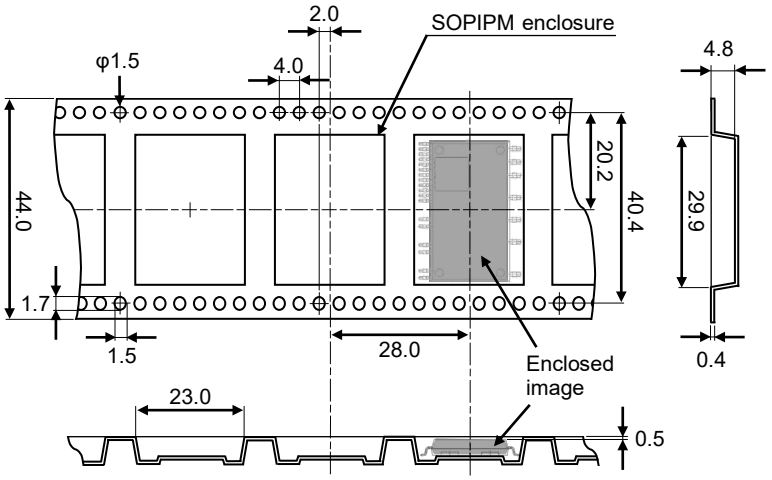


Fig.5-1-1 Embossed carrier tape (Unit:mm)

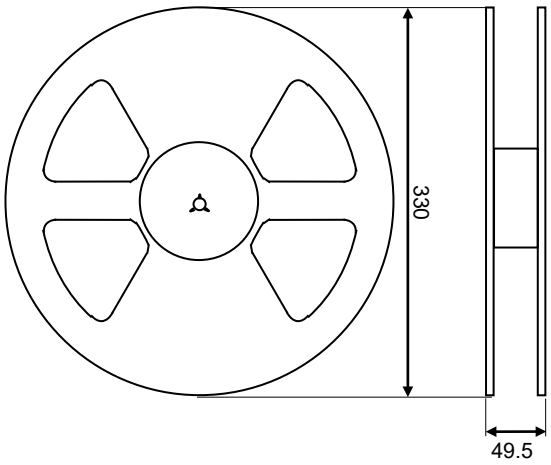


Fig.5-1-2 Tape reel (Unit:mm)

How to pack SOPIPM in the carrier tape is described in the below figure.

Contain SOPIPM in the embossed carrier tape and seal it with top cover tape. Heat and seal on the tape surface, and enclose the SOPIPM in the tape. The tape is wound on a tape reel so that the 1 pin and 2D code are located at the upper left when the tape is pulled out from the reel to the right.

One tape reel contains 450 devices. (There is a possibility of containing mixed lot products in one reel)

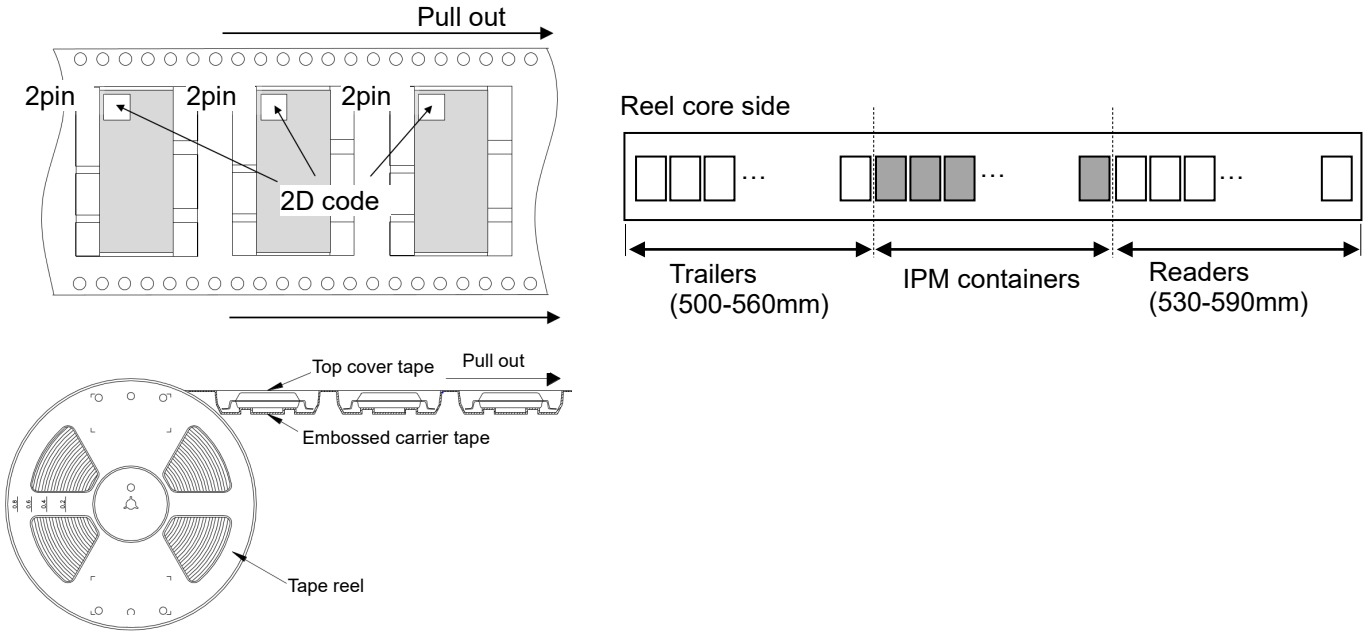
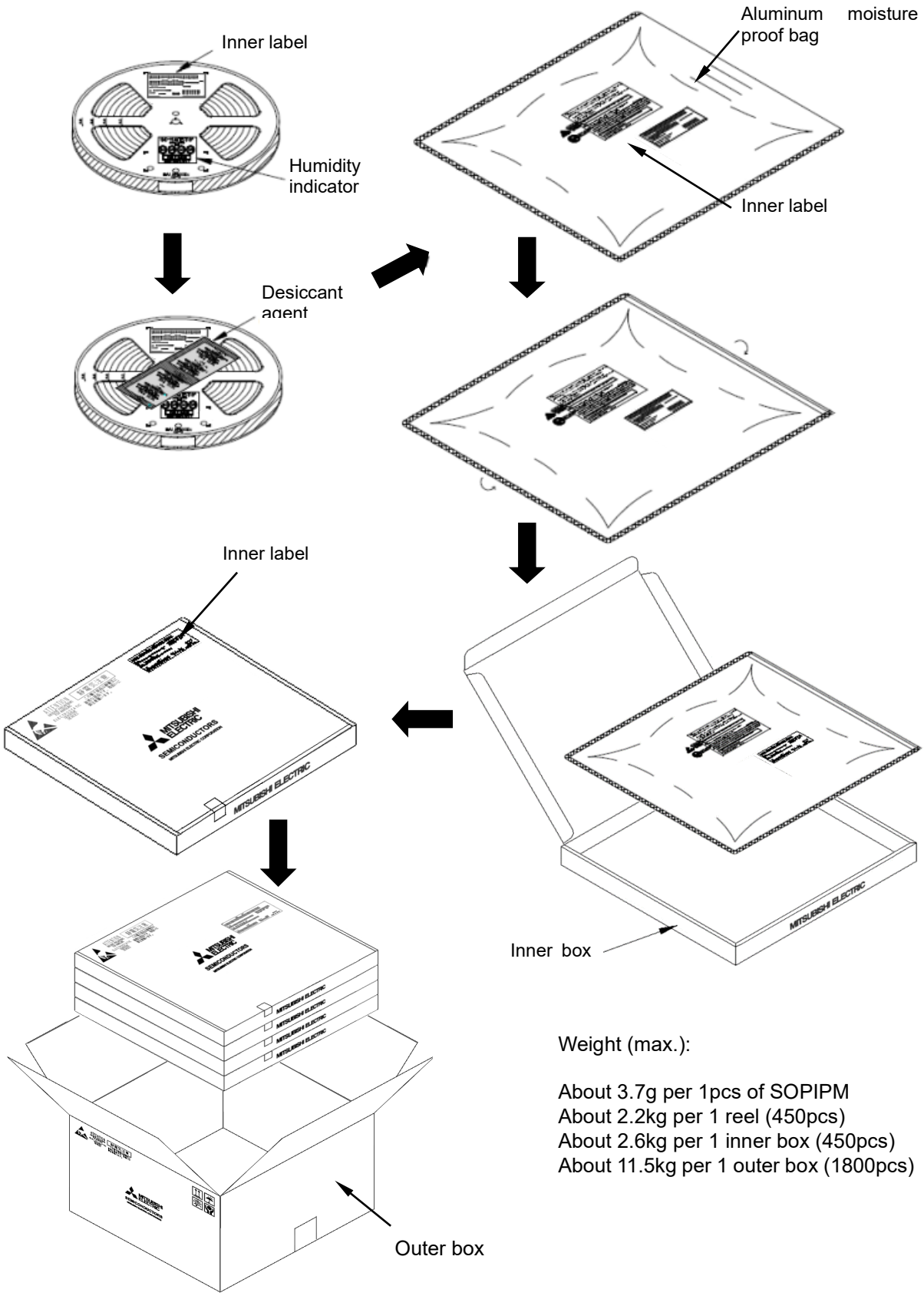


Fig.5-1-3 Carrier tape packing specifications

How to pack the tape reel is described in the below figure.

The tape reel is packed and sealed in aluminum moisture proof bag with desiccant agent. The moisture proof package is put in an inner box individually and the inner boxes are shipped in the outer box.

One outer box contains four inner boxes maximum. Some spacers are added when packing three inner boxes or less.



Weight (max.):

About 3.7g per 1pcs of SOPIPM
About 2.2kg per 1 reel (450pcs)
About 2.6kg per 1 inner box (450pcs)
About 11.5kg per 1 outer box (1800pcs)

Fig.5-1-4 Tape reel packing specifications

5.2 Handling Precautions

⚠ Cautions	
Packing Packaging	・Our device are packed and shipped with dedicated interior and exterior boxes which is designed to withstand certain environmental conditions, but if the package is exposed to external shocks, rainwater, pollution, etc., the package may be broken and the devices may be exposed. Please be careful with handling the package carefully.
Transportation	・Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ・Throwing or dropping the packaging boxes might cause the devices to be damaged. ・Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day. ・Take care about a mechanical shock as much as possible at the time of transportation.
Storage	<The storage deadline when kept in the moisture-proof packing> ・In moisture-proof packing condition, please use within 1 year from moisture proof packing day (label printing date) under storage condition of 5~35°C, 40~75%RH. ・When opening the packing, if the 30% humidity control part of the indicator turns lavender color or pink color, please use them after baking (125°C, 24hours). Since the tape is not heat resistant, please bake them after transferring from tape to a heat-resistant container. <The storage deadline after opening the moisture-proof packing> ・Please refer the below table for the storage deadline after opening the packing. If it is expected to exceed the following allowable time, it is recommended to store them in a drying oven at room temperature (30%RH or less). ・When beyond the below deadline, please use them after baking (125°C, 24hours). Since the tape is not heat resistant, please bake them after transferring from tape to a heat-resistant container. The storage deadline after opening the packing Condition: 30°C or less, 60%RH or less — Storage deadline: Within 168hours
Long storage	・When storing modules for a long time (more than one year), dehumidifying measures should be provided for the storage place. When using devices after a long period of storage, make sure to check the exterior of the devices is free from scratches, dirt, rust, and so on.
Surroundings	・Keep modules away from places where water (including dew condensation) or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	・The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.

⚠ Cautions

Over voltage	<Precautions for Overvoltage failure> ・Be aware of the overvoltage destruction due to the surge propagating to power chips in the IPM when discharging is generated not only to the IPM directly, but also to the external shape of the IPM or even the mounted board indirectly. e.g. hot plugging of the connector to discharge in the in-line test process, contact failure of jig in the insulation test process, and so on.
Static electricity	・ICs and power chips with MOS gate structure are used for the SOPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1) Precautions against the device destruction caused by the ESD When the ESD of human bodies, packaging and etc. are applied to terminal, it may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. ・Containers that charge static electricity easily should not be used for transit and for storage. ・Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. ・Should not be taking out SOPIPM from tubes until just before using SOPIPM and never touch terminals with bare hands. ・During assembly and after taking out SOPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. ・When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. ・If using a soldering iron, earth its tip. (2)Notice when the control terminals are open ・When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction.

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