MITSUBISHI ELECTRIC

< DIPIPM >

DIPIPM+ Series APPLICATION NOTE

PSSxxMC1Fx, PSSxxNC1Fx

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DIPIPM+ Series Application note

CHAPTER 1 : INTRODUCTION

1.1 Feature of DIPIPM+

DIPIPM+ series is our latest transfer molding CIB type IPM(CIB: Converter Inverter Brake, IPM: Intelligent Power Module). It integrates the inverter, converter and brake parts to make up a compact inverter systems for commercial and industrial inverter application like commercial air conditioner, servo and general purpose inverter. We also offers DIPIPM+ without brake type.

General DIPIPM integrates a inverter part only, but recent market demand requires highly integrated IPM products including more functions and peripheral circuits. So we realized this All-in-One DIPIPM, “DIPIPM+”. DIPIPM+ series is well designed transfer molding package from our long term histroy as the pioneer.

DIPIPM+ integrates main compornents for inverter circuit and it will contribute to reduce total cost by smaller mounting area for inverter circuit, shorter designing time and more reasonable assembly cost. It employs low-voltage (LV) and high voltage (HV) control ICs and their corresponding bootstrap circuit for IGBT driving and protection, as same as general DIPIPM series. So DIPIPM+ series enable same system design for its inverter part like general DIPIPM series.

By adopting same structure of heat radiation as Large DIPIPM series which has high thermal conductivity, it is possible to design system with high reliability.

Main features of this series are described as follows;

- ***Newly optimized CSTBT are integrated for improving performance***
- ***1200V series covers from 5A to 35A and 600V has 50A rating product, DIPIPM+ has wide lineup***
- ***Easy to design a PCB pattern wiring by smart terminal layout.***
- ***Incorporating bootstrap diode(BSD) with current limiting resistor for P-side gate driving supply***
- ***Easy to use temperature output function of the sensor integrated on control IC***

Fig.1-1 shows package photograph and Fig.1-2 shows the cross-sectional structure.

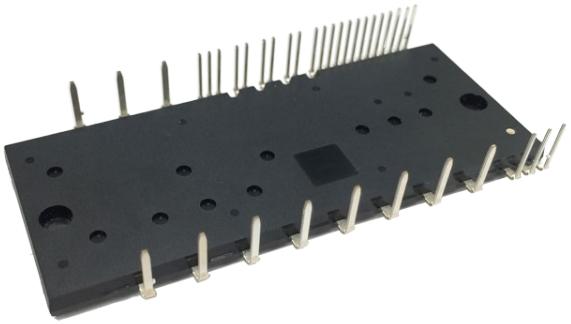


Fig.1-1. Package photograph

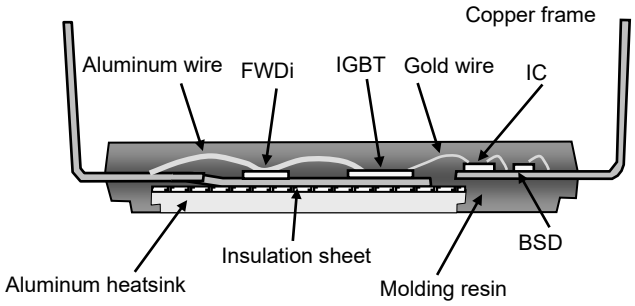


図 1-2 Cross-sectional structure

1.2 Functions

Inverter block

●For P-side IGBT
- Drive circuit
- High voltage level shift circuit
- Control supply under voltage (UV) lockout circuit (without fault signal output)
- Built-in bootstrap diode (BSD) with current limiting resistor

●For N-side IGBTs:
- Drive circuit;
- Short circuit (SC) protection circuit
- Control supply under voltage (UV) lockout circuit (with fault signal output)
- Outputting LVIC temperature by analog signal (No self over temperature protection)

(note) about SC protection
By detecting voltage of external shunt resistor, DIPIPM+ works to protect.

●Fault signal output
- Corresponding to N-side IGBT SC protection and N-side UV protection.

Brake block

●For IGBT
- Drive circuit
- UV protection circuit without fault signal

Common items

●IGBT drive supply
- Single DC15V power supply

●Control input supply
- High active logic with 5V

●UL recognized
- UL1557 File E323585

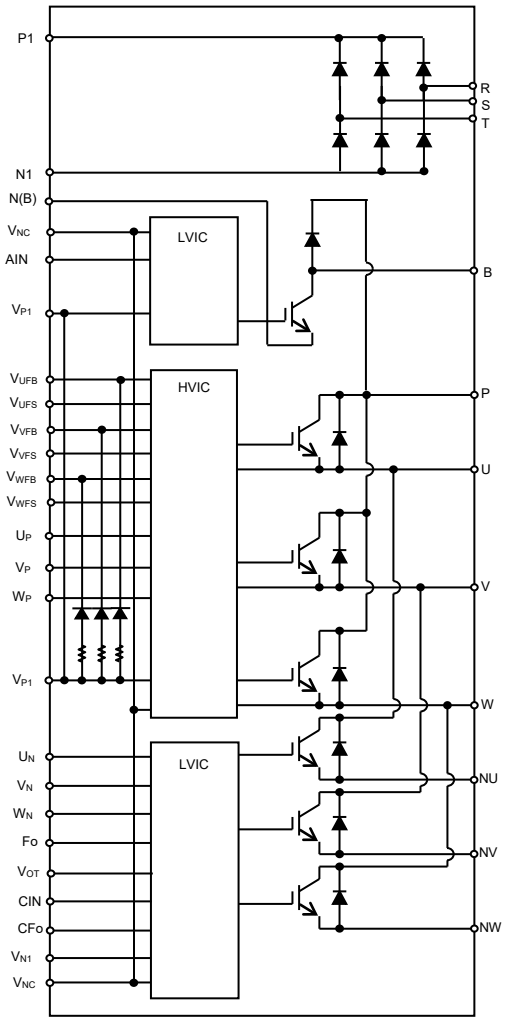


Fig. 1-3 Internal circuit block diagram for DIPIPM+ with Brake circuit

1.3 Applications

Motor drives for low power industrial equipment and commercial equipment such as air conditioners

1.4 Line-up

Line-ups are described as following table 1-1. and 1-2.

Table 1-1. DIPIPM+ with Brake circuit

Type name	Rated current	Rated voltage	Motor ratings (note1)	Brake	Isolation voltage
PSS05MC1FT	5A	1200V	0.75kW/440V_{AC}	Yes	2500Vrms(note2)
PSS10MC1FT	10A		1.5kW/440V_{AC}		
PSS15MC1FT	15A		2.2kW/440V_{AC}		
PSS25MC1FT	25A		3.7kW/440V_{AC}		
PSS35MC1FT	35A		5.5kW/440V_{AC}		
PSS50MC1F6	50A	600V	3.7kW/220V_{AC}		

Table 1-1. DIPIPM+ without Brake circuit

Type name	Rated current	Rated voltage	Motor ratings (note1)	Brake	Isolation voltage
PSS05NC1FT	5A	1200V	0.75kW/440V_{AC}	No	2500Vrms(note2)
PSS10NC1FT	10A		1.5kW/440V_{AC}		
PSS15NC1FT	15A		2.2kW/440V_{AC}		
PSS25NC1FT	25A		3.7kW/440V_{AC}		
PSS35NC1FT	35A		5.5kW/440V_{AC}		
PSS50NC1F6	50A	600V	3.7kW/220V_{AC}		

(note 1)

The motor ratings are described for industrial and general motor capability, and actual ratings are different with application condition.

(note 2)

Isolation voltage is tested under the condition of which all terminals are connected with conductive material and DIPIPM+ is applied 60Hz sinusoidal voltage between the terminals and heatsink for 1minute.

CHAPTER 2 : SPECIFICATIONS and CHARACTERISTICS

2.1 Specification of DIPIPM+

It is representatively described as follows with PSS25MC1FT (25A/1200V,CIB type).
For the other products, please refer each data sheets in details.

2.1.1 Maximum ratings

Maximum ratings are described as following table 2-1-1. (T_j = 25°C, unless otherwise noted)

Table 2-1-1 Maximum rating of PSS25MC1FT (25A/1200V,CIB type)

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	900	V	(1)
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	1000	V	(2)
V_{CES}	Collector-emitter voltage		1200	V	(3)
$\pm I_C$	Each IGBT collector current	T_C= 25°C (Note 1)	25	A	(4)
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, less than 1ms	50	A	
T_j	Junction temperature		-30~+150	°C	(5)

BRAKE PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{CC}	Supply voltage	Applied between P-N(B)	900	V	
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-N(B)	1000	V	
V_{CES}	Collector-emitter voltage		1200	V	
I_C	Each IGBT collector current	T_C= 25°C (Note 1)	15	A	
I_{CP}	Each IGBT collector current (peak)	T_C= 25°C, less than 1ms	30	A	
V_{RRM}	Repetitive peak reverse voltage		1200	V	
I_F	Forward current	T_C= 25°C	15	A	
I_{FP}	Forward current (peak)		30	A	
T_j	Junction temperature		-30~+150	°C	(5)

CONVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{RRM}	Repetitive peak reverse voltage		1600	V	
Io	DC output current	3-phase full wave rectification	25	A	
I_{FSM}	Surge forward current	Peak value of half cycle at 60Hz, Non-repetitive	315	A	
I^2t	I^2t capability	Value for 1 cycle of surge current	416	A^2s	
T_j	Junction temperature		-30~+150	°C	(5)

CONTROL (PROTECTION) PART

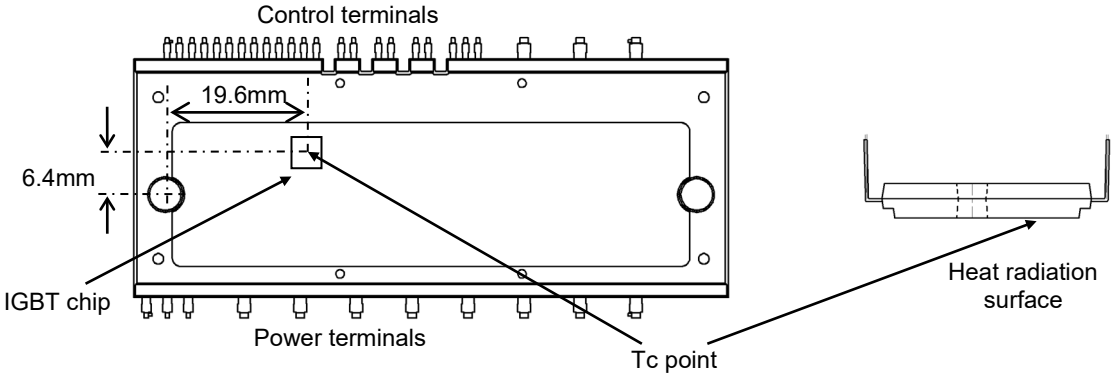
Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P,V_P,W_P,U_N, V_N, W_N, AIN-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	5	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

Note1: Pulse width and period are limited due to junction temperature.

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 125°C, non-repetitive, less than 2μs	800	V	(6)
T_C	Module case operation temperature	(Note 2)	-30~+110	°C	
T_{stg}	Storage temperature		-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}	(7)

Note2: Measurement point of Tc is described in below figure. (8)



No.	Symbol	Description
(1)	V_{CC}	The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.
(2)	$V_{CC(surge)}$	The maximum P-N surge voltage in switching status. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge under this voltage.
(3)	V_{CES}	The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.
(4)	+/- I_C	The allowable continuous current flowing at collect electrode (Tc=25°C) Pulse width and period are limited due to junction temperature.
(5)	Tj	The maximum junction temperature rating is 150°C. But for safe operation, it is recommended to limit the average junction temperature up to 125°C (at Tc is less than 100℃). Repetitive temperature variation ΔTj affects the life time of power cycle, so please refer life time curves for safety design.
(6)	$V_{CC(PROT)}$	The maximum supply voltage for turning off IGBT safely in the case of an SC or OC faults. The power chip might not be protected and break down in the case that the supply voltage is higher than this specification.
(7)	Viso	Isolation voltage is the withstanding voltage between all terminals connected with conductive material and heatsink of heat radiation.
(8)	Tc position	Tc (case temperature) is defined to be the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

Power chips layout

Fig.2-1-1 indicates the position of the each power chips. (This figure is the view from laser marked side.)
In case of PSSxxNC1Fx, Br-IGBT and Br-Di are not built-in.

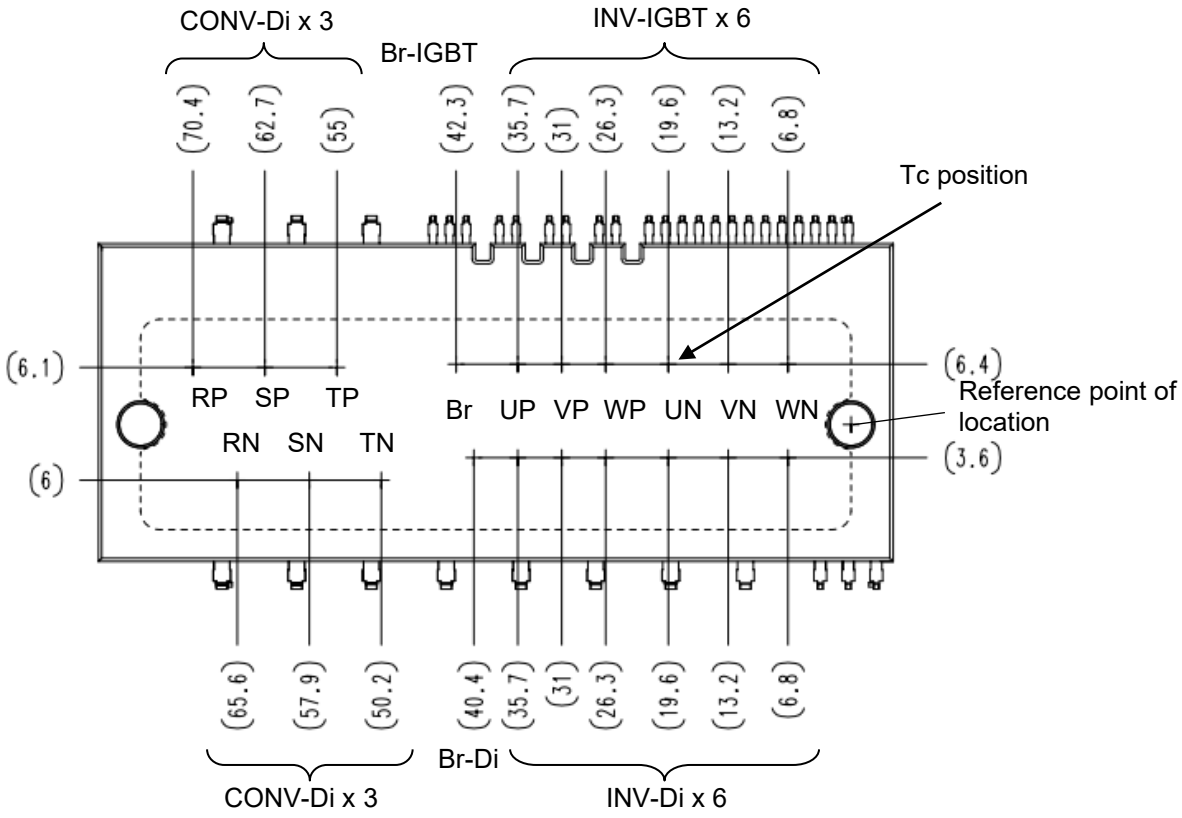


Fig. 2-1-1 Power chips layout (Unit : mm)

2.1.2 Thermal Resistance

Table 2-1-2 shows the thermal resistance between its chip junction and case.

Table 2-1-2. Thermal resistance of PSS25MC1FT (25A/1200V, CIB type)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	-	-	1.15	K/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	-	-	1.65	
$R_{th(j-c)Q}$		Brake IGBT part (per 1module)	-	-	1.45	
$R_{th(j-c)F}$		Brake Di part (per 1module)	-	-	1.65	
$R_{th(j-c)R}$		Converter part (per 1/6module)	-	-	1.10	

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~ +200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.25K/W (per 1chip, grease thickness: 20μm, thermal conductivity: 1.0W/m•K).

The above data shows static state thermal resistance. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-2. Zth(j-c)* is the normalized transient thermal impedance and formulation is described as Zth(j-c)*= Zth(j-c) / Rth(j-c)max. For example, the IGBT transient thermal impedance at 0.2s is 1.15×0.7=0.81K/W. The transient thermal impedance isn't used for constantly current, but for short period current as millisecond order. (e.g. motor starting, motor lock···e.t.c)

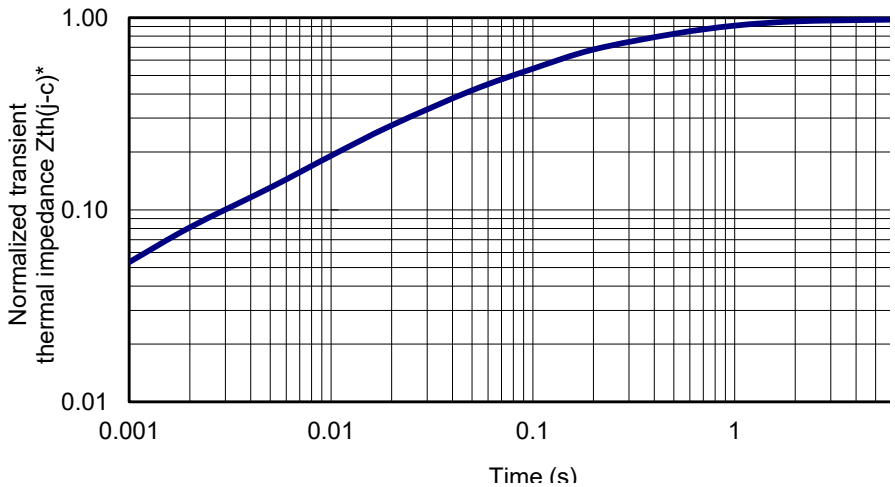


Fig. 2-1-2. Normalized transient thermal impedance

2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics. (T_j = 25°C, unless otherwise noted)

Table 2-1-3 Static characteristics and switching characteristics of PSS25MC1FT(25A/1200V, CIB type)

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB} = 15V, V_{IN}= 5V	I_C= 25A, T_j= 25°C	-	1.50	2.20	V
			I_C= 25A, T_j= 125°C	-	1.80	2.45	
V_{EC}	FWDi forward voltage	V_{IN}= 0V, -I_C= 25A		-	2.40	3.10	V
t_{on}	Switching times	V_{CC}= 600V, V_D= V_{DB}= 15V I_C= 25A, T_j= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		1.10	1.90	2.60	µs
$t_{C(on)}$				-	0.60	0.90	µs
t_{off}				-	2.80	3.80	µs
$t_{C(off)}$				-	0.50	0.90	µs
t_{rr}				-	0.60	-	µs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}	T_j= 25°C	-	-	1	mA
			T_j= 125°C	-	-	10	

BRAKE PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB} = 15V, V_{IN}= 5V	I_C= 15A, T_j= 25°C	-	1.50	2.20	V
			I_C= 15A, T_j= 125°C	-	1.80	2.45	
V_F	Di forward voltage	V_{IN}= 0V, I_F= 15A		-	2.20	2.80	V
t_{on}	Switching times	V_{CC}= 600V, V_D= V_{DB}= 15V I_C= 15A, T_j= 125°C, V_{IN}= 0↔5V, Inductive Load		1.10	1.90	2.60	µs
$t_{C(on)}$				-	0.65	1.00	µs
t_{off}				-	2.60	3.60	µs
$t_{C(off)}$				-	0.40	0.95	µs
t_{rr}				-	0.65	-	µs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}	T_j= 25°C	-	-	1	mA
			T_j= 125°C	-	-	10	

CONVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_{RRM}	Repetitive reverse current	V_R=V_{RRM}, Tj=125°C	–	–	7.0	mA
V_F	Forward voltage drop	I_F=25A	–	1.1	1.4	V

Definition of switching time and performance test topology are shown in Fig.2-1-3 and 2-1-4.
Switching characteristics are measured by half bridge circuit with inductance load.

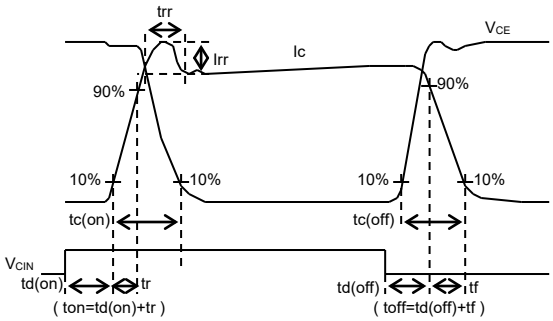


Fig. 2-1-3 Switching time definition

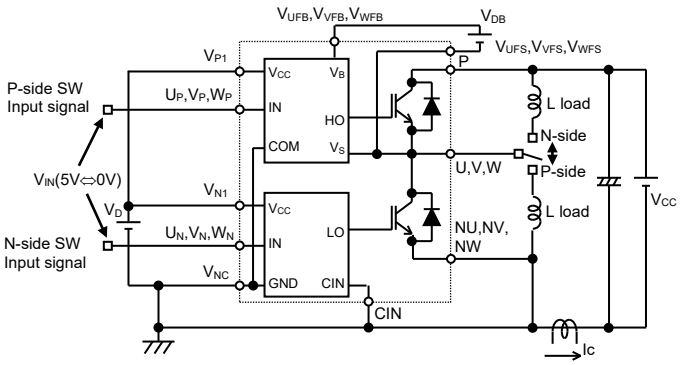


Fig. 2-1-4 Evaluation circuit (inductive load)

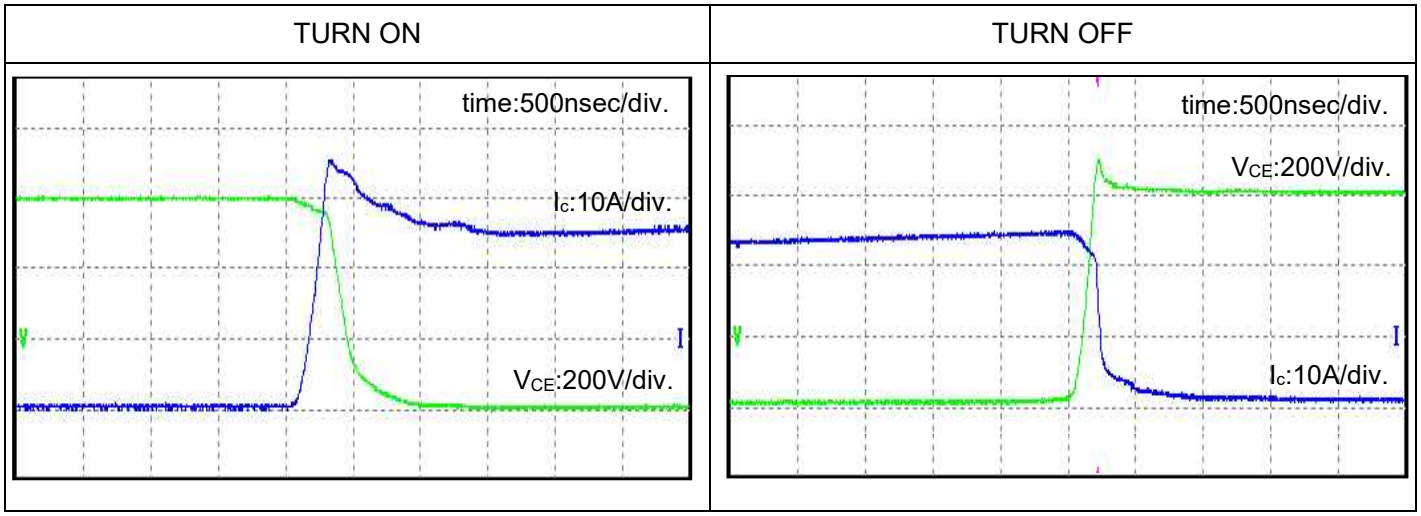


Fig. 2-1-5 Typical switching waveform for PSS25MC1FT (25A/1200V) inverter part
Condition: V_{CC}=600V, V_D=V_{DB}=15V, Ic=25A, Tj=125°C, inductive load half bridge circuit

Table 2-1-4 shows the typical control part characteristics. (T_j = 25°C, unless otherwise noted)

Table 2-1-4. Typical control part characteristics of PSS25MC1FT(25A/1200V, CIB type)

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	5.70	mA
			V_D=15V, V_{IN}=5V	-	-	5.70	
I_{DB}		Each part of V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.55	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.55	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 4)		0.455	0.480	0.505	V
UV_{DBt}	Control supply under-voltage protection(UV) for P-side of inverter part		Trip level	10.0	-	12.0	V
UV_{DBr}			Reset level	10.5	-	12.5	V
UV_{Dt}	Control supply under-voltage protection(UV) for N-side of inverter part and brake part		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature Output	Pull down R=5.1kΩ (Note 5)	LVIC Temperature=100°C	2.89	3.02	3.14	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	In case of C_{Fo}=22nF (Note 6,7)		1.6	2.4	—	ms
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P,V_P,W_P,U_N, V_N, W_N, AIN-V_{NC}		—	—	3.5	V
$V_{th(off)}$	OFF threshold voltage			0.8	—	—	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor			0.9	1.3	V
R	Built-in limiting resistance	Included in bootstrap Di		16	20	24	Ω

Note 4 : SC protection works only for N-side IGBT in inverter part. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. VOT output characteristics is described in Section 2.2.3.

6 : Fault signal Fo outputs when SC or UV protection works for N-side IGBT in inverter part. The fault output pulse-width t_{FO} is depended on the capacitance value of C_{FO} ($C_{FO} = t_{FO} \times 9.1 \times 10^{-6}$ [F]).

7 : UV protection also works for P-side IGBT in inverter part or brake part without fault signal Fo.

Table 2-1-5 shows recommended operation conditions. Please apply and use under the recommended conditions to operate DIPIPM+ series safely. (T_j = 25°C, unless otherwise noted)

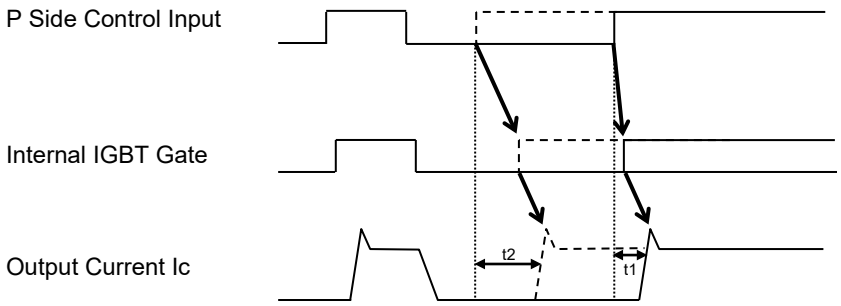
Table 2-1-5. Recommended operation conditions of PSS25MC1FT (25A/1200V, CIB type)

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU,NV,NW		0	600	800	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC},V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			-1	-	1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal		3.0	-	-	μs
f_{PWM}	PWM input frequency	T_C≤100°C, T_j≤125°C		-	-	20	kHz
PWIN(on)	Minimum input pulse width	I_C≤1.7 times of rated current (Note 8)		1.5	-	-	μs
PWIN(off)		0≤V_{CC}≤800V, 13.5≤V_D≤16.5V, 13.0≤V_{DB}≤18.5V, -20≤T_C≤100°C, N line wiring inductance less than 10nH (Note 9)	Less than rated current	3.0	-	-	
			From rated current to 1.7 times of rated current	3.5	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}- NU、NV、NW (including surge)		-5.0	-	+5.0	V
T_j	Junction temperature			-20	-	125	°C

Note 8: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).
9: DIPIPM might make no response or delayed response (P-side IGBT only) for the input signal with off pulse width less than PWIN(off). Please refer below figure about delayed response.

About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P side only)



Real line…off pulse width>PWIN(off); turn on time t1
Broken line…off pulse width<PWIN(off); turn on time t2

[note] About control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

dV/dt ≤ +/-1V/μs, Vripple≤2Vp-p

2.1.4 Mechanical characteristics and specifications

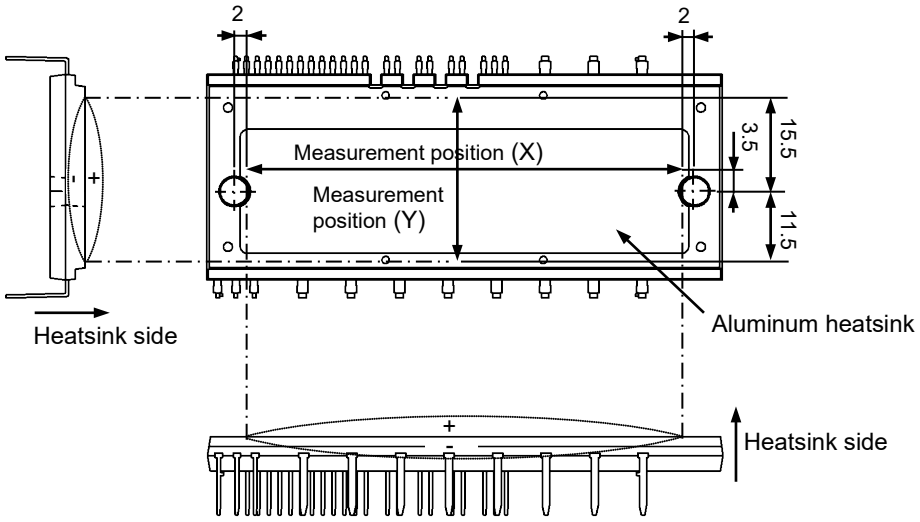
Table 2-1-6 shows mechanical characteristics and specifications. Please also refer section 2.4 for mounting instruction of DIPIPM+.

Table 2-1-6. Mechanical characteristics and specifications of PSS25MC1FT (25A/1200V, CIB type)

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4 (Note 10)	Recommended 1.18N·m	0.98	1.18	1.47	N·m
Terminal pulling strength	20N load	JEITA-ED-4701	10	—	—	s
Terminal bending strength	90deg bending with 10N load	JEITA-ED-4701	2	—	—	times
Weight			—	40	—	g
Heat radiation part flatness		(Note 11)	-50	—	+100	μm

Note 10: Plain washers (ISO 7089~7094) are recommended.
Note 11: Measurement positions of heat radiation part flatness are as below.



2.2 Protection functions and operating sequence

DIPIPM+ has two protection functions of short circuit (SC) and under voltage of control supply (UV). And it has also temperature output function of LVIC (VOT). The operating principle and sequence are described as follows.

2.2.1 Short circuit protection

(1) Outline

DIPIPM+ uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection Vsc(ref) is 0.48V typical.

In case of SC protection works, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output. To prevent DIPIPM+ erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: 1.5μ ~ 2μs) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.

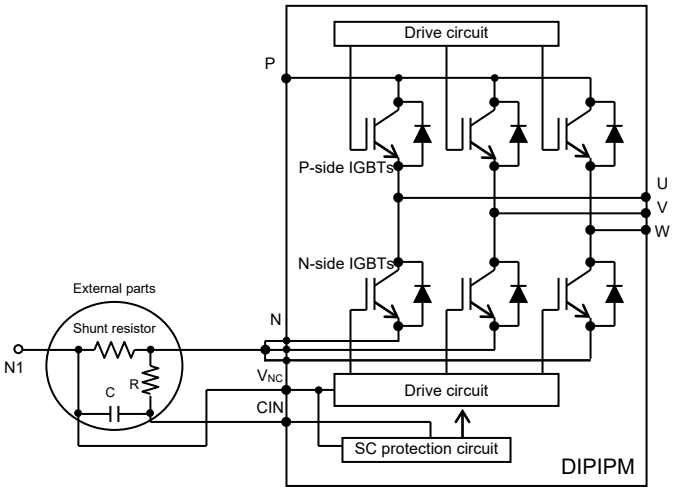


Fig.2-2-1 SC protection circuit

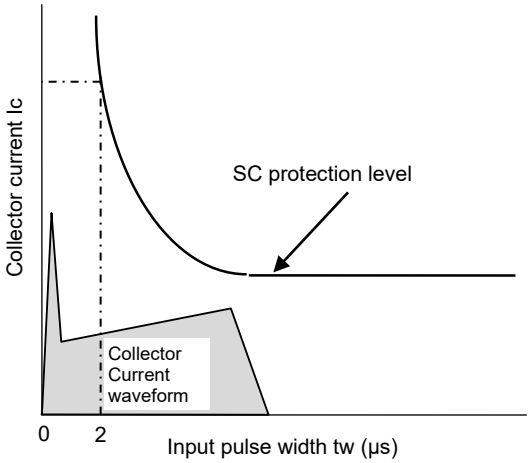


Fig.2-2-2 Filtering time constant setting

(2) SC protection sequence for only low-side with external shunt resistor and RC filter

a1. Normal operation: IGBT ON and outputs current.
a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
a3. All N-side IGBT's gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. LVIC starts outputting fault signal (fault signal output time is controlled by external capacitor C_{FO})
a6. Input = “L”: IGBT OFF
a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: IGBT ON and outputs current.

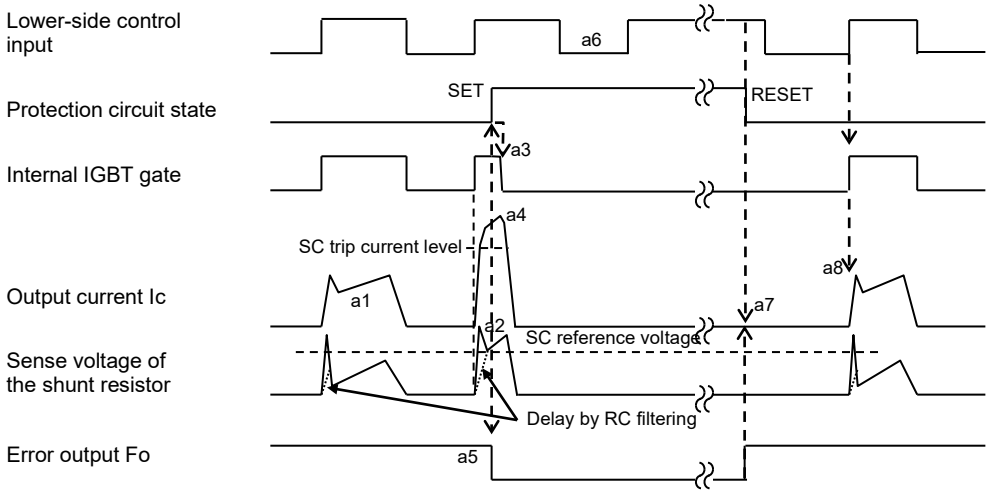


Fig.2-2-3 SC protection timing chart

(3) Calculation of shunt resistance

The value of current sensing shunt resistance for current sensing is calculated by the following formulation:

$R_{Shunt} = V_{SC(ref)}/SC$ where $V_{SC(ref)}$ is the SC trip voltage.

The maximum SC trip level SC(max) should be set less than the IGBT minimum saturation current which is 1.7 times as large as the rated current. For example, the SC(max) of PSS25MC1FT should be set to 25x1.7=42.5A. The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered when designing the SC trip level. The dispersion of DIPIPM+ series is +/-0.025V in the specification of $V_{SC(ref)}$ as shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$

Symbol	Condition	Min	Typ	Max	Unit
$V_{SC(ref)}$	Tj=25°C, V_D=15V	0.455	0.480	0.505	V

Therefore, the range of SC trip level can be calculated by the following descriptions with +/-5% dispersion of shunt resistor :

$R_{Shunt(min)}=V_{SC(ref)\ max}$ /SC(max)

where SC(max) is 1.7 times of rated current, and so 0.95 is due to -5% dispersion of shunt resistor that

$R_{Shunt(typ)}= R_{Shunt(min)}$ / 0.95

Therefore, SC(typ) = $V_{SC(ref)\ typ}$ / $R_{Shunt(typ)}$.

$R_{Shunt(max)}= R_{Shunt(typ)}$ x 1.05* *1.05 is due to +5% dispersion of shunt resistor

Therefore, SC(min)= $V_{SC(ref)\ min}$ / $R_{Shunt(max)}$

In this case, SC trip level is 42.5A,

$R_{Shunt(min)}$= 0.505V / 42.5A = 11.9 mΩ, $R_{Shunt(typ)}$= 11.9mΩ / 0.95 = 12.5 mΩ, $R_{Shunt(max)}$= 12.5 x 1.05 = 13.1mΩ

When the both of SC trip level and shunt resistor will be maximum, typical and minimum, these will be described as follows;

SC(max)= 42.5 A (setting), SC (typ) = 0.480 / 12.5 = 38.4 A, SC(min) = 0.455 / 13.1 = 34.7 A

From the above, the SC trip level range is described as Table 2-2-2.

Table 2-2-2 Operative SC Range

Condition	min.	typ.	max.	Unit
Tj=25°C, V_D=15V	34.7	38.4	42.5	A

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacitance. It is recommended to make a confirmation of the resistance by prototype experiment.

(4) RC filter time constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIPIPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, The time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$

$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

Where Vsc is the CIN terminal input voltage, Ic is the peak current, τ is the RC time constant.

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to IGBT gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	Min	typ	max	Unit
IC transfer delay time	-	-	1.0	μs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:

t_{TOTAL}=t1＋t2

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4. Both P-side, N-side of inverter part and Brake part have UV protecting function. However fault signal(Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-2-4 DIPIPM operating behavior versus control supply voltage

Control supply voltage (V_D, V_{DB})	Operating behavior
0-4.0V (P, N)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally IGBT does not work. But external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4.0-UV_{Dt} (N), UV_{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work.
UV_{Dt} (N)-13.5V UV_{DBt} (P)-13.0V	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N) 13.0-18.5V (P)	Recommended conditions.
16.5-20.0V (N) 18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	The control circuit might be destroyed.

(note) Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

(1) N-side UV Protection Sequence

a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L→H).(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a2. Normal operation: IGBT ON and carrying current.
a3. V_D level dips to under voltage trip level. (UV_{Dt}).
a4. All N-side IGBTs turn OFF in spite of control input condition.
a5. Fo outputs for the period set by the capacitance $C_{FO,}$ but output is extended during V_D keeps below UV_{Dr}.
a6. V_D level reaches UV_{Dr}.
a7. Normal operation: IGBT ON and outputs current.

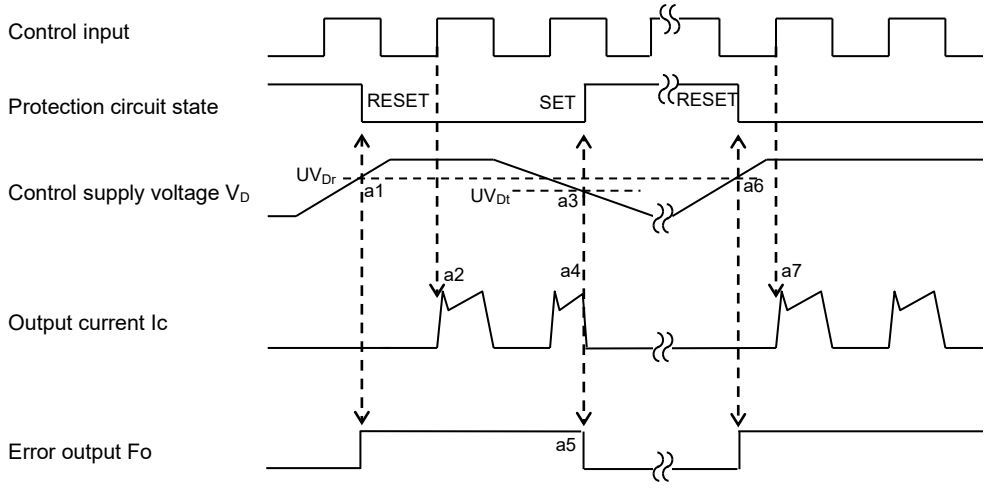


Fig.2-2-4 Timing Chart of N-side UV protection

(2) P-side UV Protection Sequence

a1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, IGBT turns on by next ON signal (L→H).
a2. Normal operation: IGBT ON and outputs current.
a3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
a4. IGBT of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
a5. V_{DB} level reaches UV_{DBr}.
a6. Normal operation: IGBT ON and outputs current.

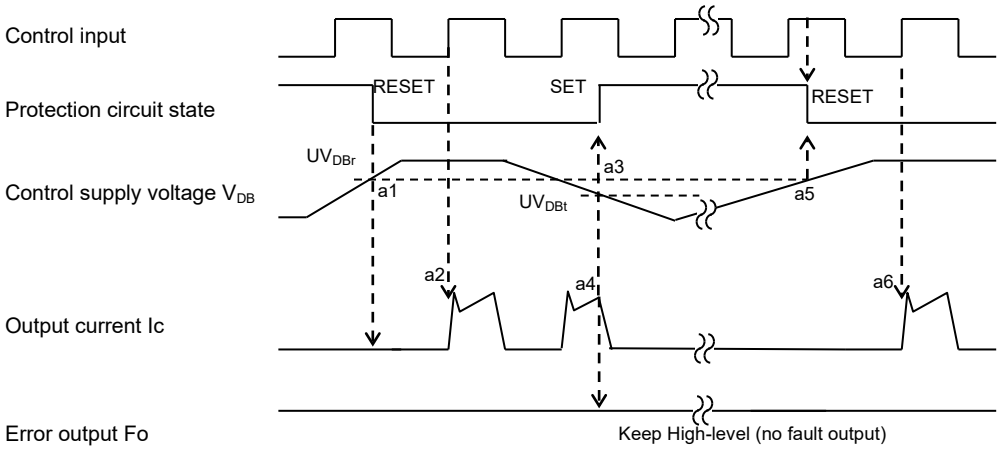


Fig.2-2-5 Timing Chart of P-side UV protection

(3) Brake UV Protection Sequence (with Brake product only : PSSxxMC1Fx)

a1. Control supply voltage V_D rises. After the voltage reaches under voltage reset level UV_{Dr}, IGBT turns on by next ON signal (L→H).
a2. Normal operation: IGBT ON and collector current.
a3. V_D level drops to under voltage trip level (UV_{Dt}).
a4. IGBT of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
a5. V_D level reaches UV_{Dr}.
a6. Normal operation: IGBT ON and outputs current.

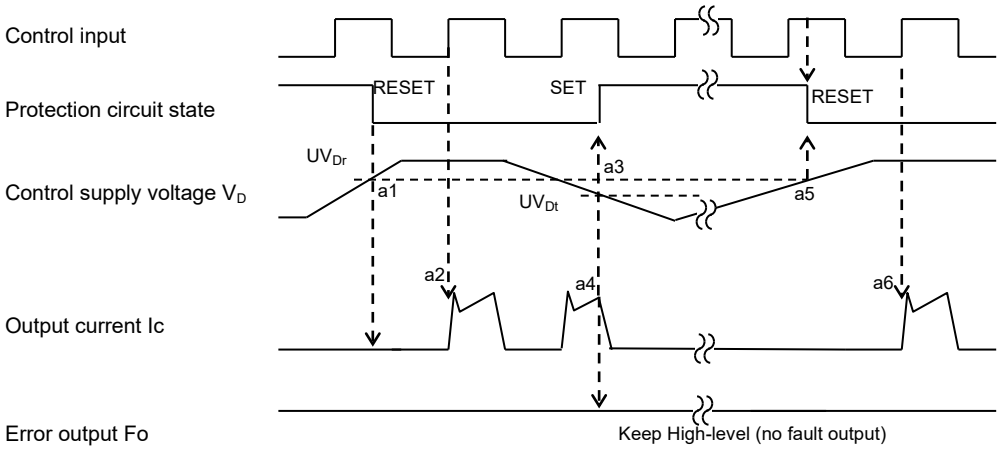


Fig.2-2-6 Timing Chart of brake circuit UV protection

2.2.3 Temperature output function V_{OT}

(1) Usage of this function

This function measures the temperature of control LVIC by built in temperature sensor on LVIC.

The heat generated at IGBT and FWDi transfers to LVIC through molding resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively. (e.g. motor lock, short circuit). It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down and continuance of overload operation.（Replacement from the thermistor which was mounted on outer heat sink currently）

(note)

In this function, DIPIPM cannot shutdown IGBT and output fault signal by itself when temperature rises excessively. When temperature exceeds the defined protection level, controller (MCU) should stop the DIPIPM.

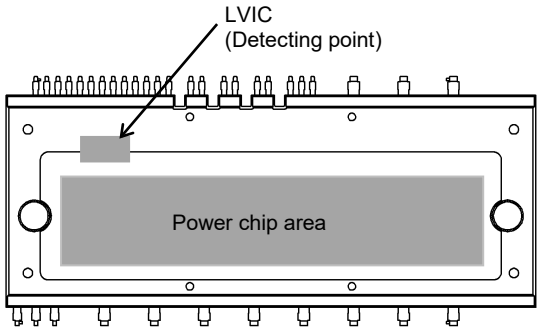


Fig.2-2-7 Temperature detecting point

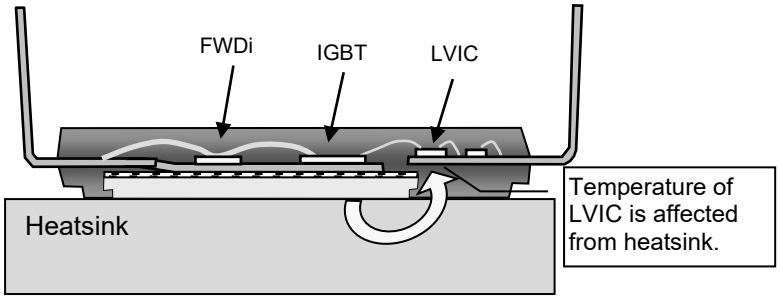


Fig.2-2-8 Thermal conducting from power chips

(2) VOT characteristics

VOT output circuit, which is described in Fig.2-2-9, is the output of OP amplifier circuit. The current capability of VOT output is described as Table 2-2-5. The characteristics of VOT output vs. LVIC temperature is linear characteristics described in Fig.2-2-11. There are some cautions for using this function as follows.

Table 2-2-5 Output capability

(Tc=-20°C ~100°C)

	min.
Source	1.7mA
Sink	0.1mA

Source: Current flow from V_{OT} to outside.

Sink : Current flow from outside to V_{OT}.

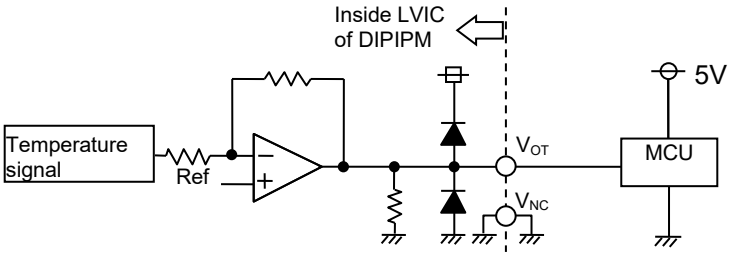


Fig.2-2-9 V_{OT} output circuit

(note) In the case of detecting lower temperature than room temperature

It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

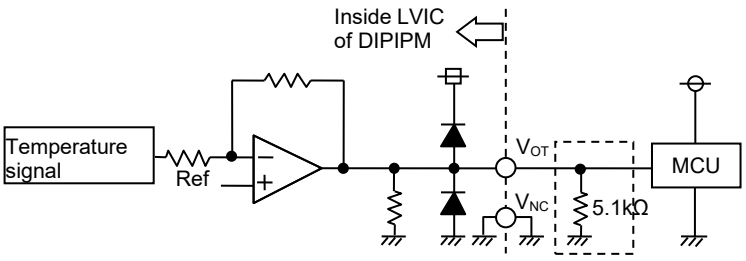


Fig.2-2-10 V_{OT} output circuit in the case of detecting low temperature

Please handle the following characteristics of VOT output vs. LVIC temperature as reference data to set over temperature protection. These curves are based on theoretical designed value excluding specified value in the target specification.

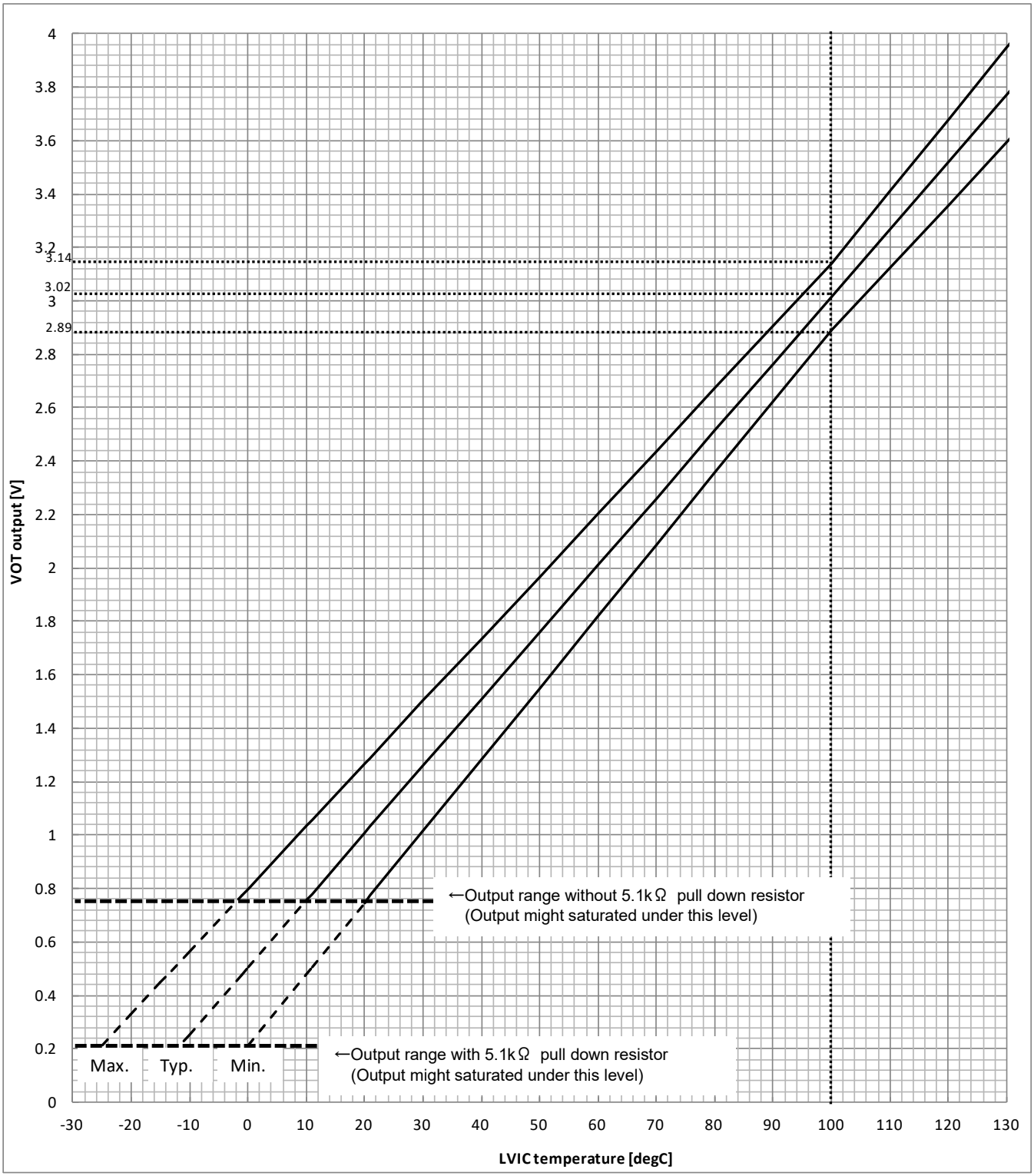


Fig.2-2-11 V_{OT} output vs. LVIC temperature

The heat of power chips transfers to LVIC through the heat sink and package, so the relationship between LVIC temperature: Tic(=V_{OT} output), case temperature: Tc(under the chip defined on datasheet), and junction temperature: Tj depends on the system cooling condition, heat sink, control strategy, etc. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature Tic, it is important to consider the protection temperature keeps Tj ≤150°C.

2.3 Package outline of DIPIPM+

2.3.1 Package outline

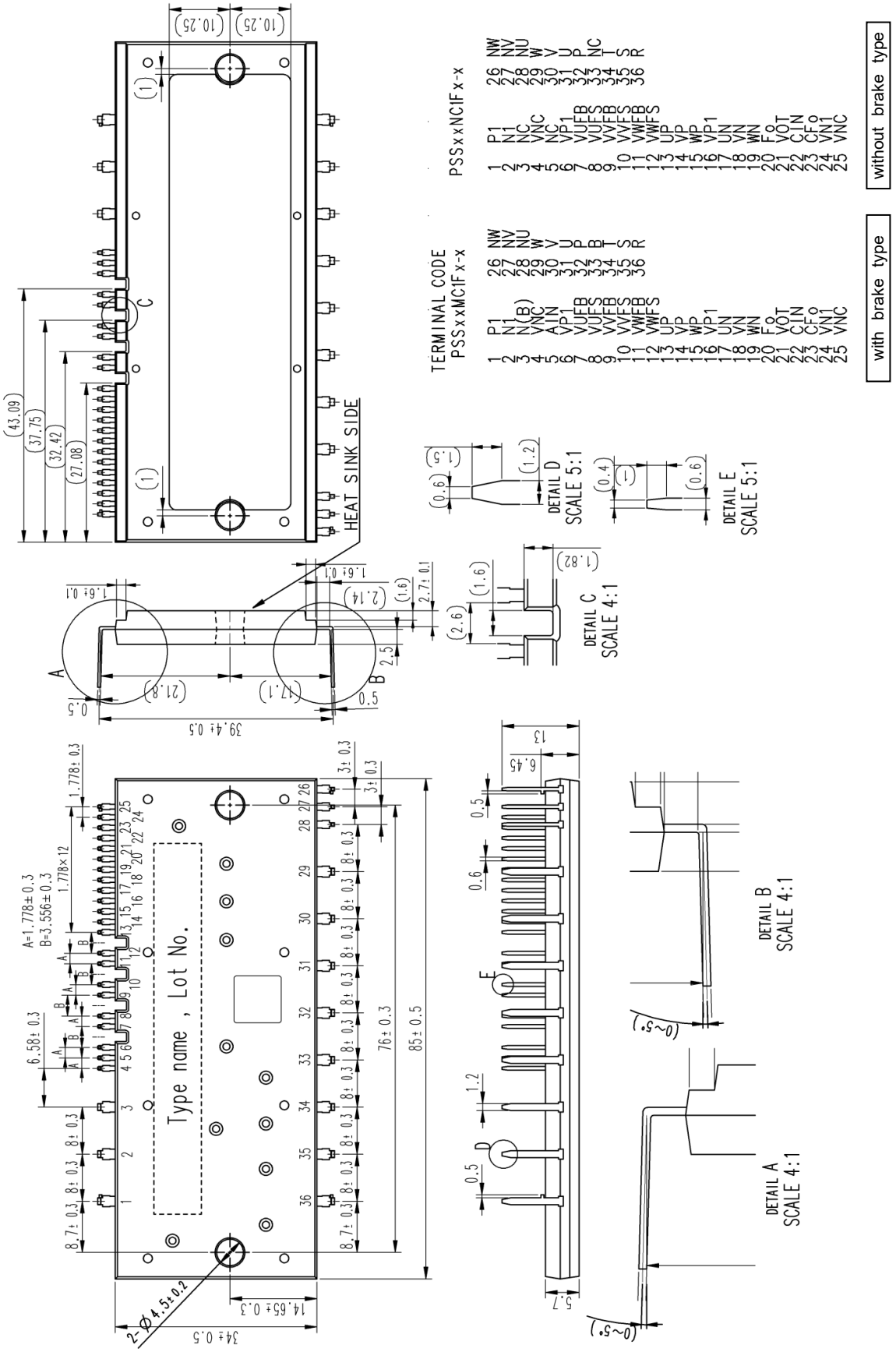


Fig. 2-3-1 Package outline drawing (Dimension in mm)

2.3.2 Marking

The laser marking specifications of DIPIPM+ are described in Fig.2-3-2. Company name, Country of origin, Type name, Lot number, and 2D code are marked on the surface of module.

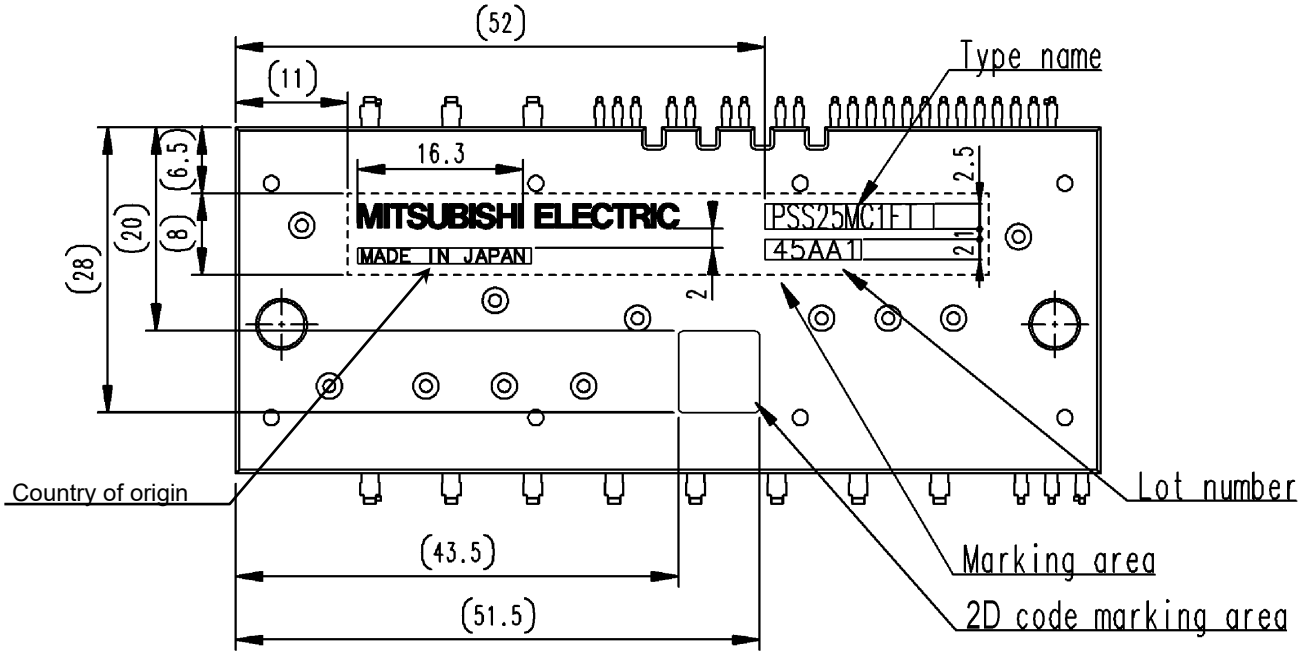


Fig.2-3-2 Laser marking view PSSxxxC1Fx (Dimension in mm)

The Lot number indicates production year, month, running number and country of origin.
The detailed is described as below.

(Example)

6 9 AA1

- AA1 → Running number
- 9 → Product month (however O: October, N: November, D: December)
- 6 → Last figure of Product year (e.g. This case describes the year 201<u>6</u>.)

2.3.3 Terminal Description

Table 2-3-1 Terminal Description

	PSSxxMC1Fx With Brake	PSSxxNC1Fx Without Brake	Description
1	P1	←	Output terminal for converter (+)
2	N1	←	Output terminal for converter (-)
3	N(B)	(NC)	IGBT emitter terminal for brake
4	V_{NC}*1)	←	Control supply GND terminal (Brake part)
5	AIN	(NC)	Brake part control input terminal
6	V_{P1}*2)	←	Control supply positive terminal (+)
7	V_{UFB}	←	U-phase P-side drive supply positive terminal
8	V_{UFS}	←	U-phase P-side drive supply GND terminal
9	V_{VFB}	←	V-phase P-side drive supply positive terminal
10	V_{VFS}	←	V-phase P-side drive supply GND terminal
11	V_{WFB}	←	W-phase P-side drive supply positive terminal
12	V_{WFS}	←	W-phase P-side drive supply GND terminal
13	U_P	←	U-phase P-side control input terminal
14	V_P	←	V-phase P-side control input terminal
15	W_P	←	W-phase P-side control input terminal
16	V_{P1}*2)	←	Control supply positive terminal (+)
17	U_N	←	U-phase N-side control input terminal
18	V_N	←	V-phase N-side control input terminal
19	W_N	←	W-phase N-side control input terminal
20	Fo	←	Fault signal output terminal
21	V_{OT}	←	Temperature output terminal
22	CIN	←	SC current trip voltage detecting terminal
23	CFo	←	Fault pulse output width setting terminal
24	V_{N1}	←	N-side control supply positive terminal (+)
25	V_{NC}*1)	←	GND terminal for brake control supply
26	NW	←	WN-phase IGBT emitter terminal
27	NV	←	VN-phase IGBT emitter terminal
28	NU	←	UN-phase IGBT emitter terminal
29	W	←	W-phase output terminal
30	V	←	V-phase output terminal
31	U	←	U-phase output terminal
32	P	←	Inverter DC-link positive terminal
33	B	(NC)	Brake terminal
34	T	←	AC input terminal
35	S	←	AC input terminal
36	R	←	AC input terminal

NC: No connection

(note)

1) Two V_{NC} terminals (GND terminal for control supply) are connected mutually inside of DIPIPM+, please connect either terminal to GND and make the other terminal leave no connection.
2) Two V_{P1} terminals are connected mutually inside, please connect either terminal to supply and make the other terminal leave no connection.

Table 2-3-2 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}- V_{UFS} V_{VFB}- V_{VFS} V_{WFB}- V_{WFS}	• Drive supply terminals for P-side IGBTs. • By mounting bootstrap capacitor, individual isolated power supplies are not needed for the P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply when potential of output terminal is almost GND level. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability due to ripple or surge. In order to prevent malfunction, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • V_{P1}, and V_{N1} should be connected externally on PCB. In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with good frequency characteristics should be mounted very close to these terminals. • Please design the supply carefully so that the voltage ripple caused by operation keep within the specification. ($dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$) • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Please make sure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N AIN	• Control signal input terminals. This is Voltage input type. • These terminals are internally connected to Schmitt trigger circuit and pulled down by min 3.3kΩ resistor internally • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Please use RC coupling in case of signal oscillation. Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor.
Short-circuit trip voltage detecting terminal	CIN	• For short circuit protection, input the potential of external shuint resistor to CIN terminal through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal for N-side abnormal state(SC or UV). • This output is open drain type. It is recommended to pull up F_O signal line to the 5V supply by 10kΩ when Fo signal is input to MCU directly (Check whether the V_{FO} satisies the threshold level of input of MCU when selecting resistance). • In the case of directly driving opto coupler by Fo output it is needed to set the pull-up resistance so that I_{FO} becomes under 5mA(maximum rating). And pulled up to 15V supply is recommended.(V_{FO} increases in propotion to increasing $I_{FO.}$)
Fault pulse output width setting terminal	C_{FO}	• The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and V_{NC}. When 22nF capacitor is connected, then the Fo pulse width becomes 2.4ms. Because of $C_{FO} = t_{FO} \times 9.1 \times 10^{-6}$ (F)
Temperature output terminal	V_{OT}	• LVIC temperature is ouput by analog signal. It is ouput of OP amplifer internally. • It is recommended to connect 5.1kΩ pulldown resistor if output linearlity is necessary under room temperature.
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P terminal. It is also effective to add small film capacitor with good frequency characteristics for snubber.

(Continue)

Item	Symbol	Description
Inverter DC-link negative terminal	NU, NV, NW	• Emitter terminal of each N-side IGBT • Usually, these terminals are connected to the power GND through individual shunt resistor. • If common emitter circuit (one shunt control) is applied, connect these terminals together at the point as close from the package as possible.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.
AC power supply input terminal	R, S, T	• AC power supply input terminal
Converter positive output terminal	P1	• Converter positive output terminal
Converter GND terminal	N1	• Converter GND terminal

(note)

Use oscilloscope to check voltage waveform of each power supply terminals and P and N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

If there is a surge more than threshold of ratings or superimposed noise, it is necessary to take some counter noise measurements; revising pattern, replacing capacitor, apply zener diode, enhancing filtering and so on.

2.4 Mounting Method

This section are described the electric spacing and mounting precautions of DIPIPM+.

2.4.1 Electric Spacing of DIPIPM+

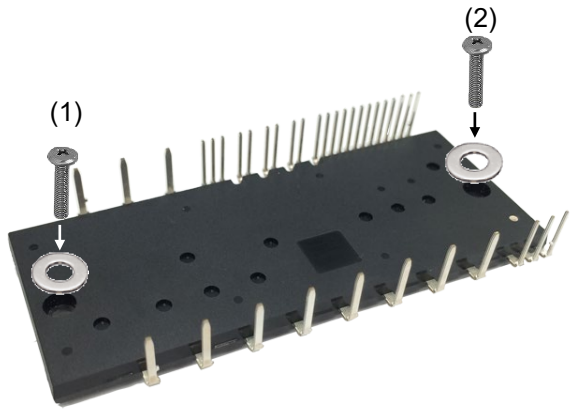
The electric spacing specification of DIPIPM+ is shown in Table 2-4-1.

Table 2-4-1 Minimum insulation distance(minimum value)

Clearance(mm)		Creepage(mm)	
Between power terminals	5.7	Between power terminals	6.0
Between control terminals	2.3	Between control terminals	6.2
Between terminals and heat sink	2.5	Between terminals and heat sink	4.1

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-4-1. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention not to have any foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test (e.g. insulation inspection) on the final product after fixing the DIPIPM with the heatsink.



Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-4-1 Recommended screw fastening order

Table 2-4-2 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Screw : M4	0.98	—	1.47	N·m
Flatness of outer heat sink	Refer Fig.2-4-2	-50	—	+100	μm

(note): Recommend to use plain washer (ISO7089-7094) in fastening the screws.

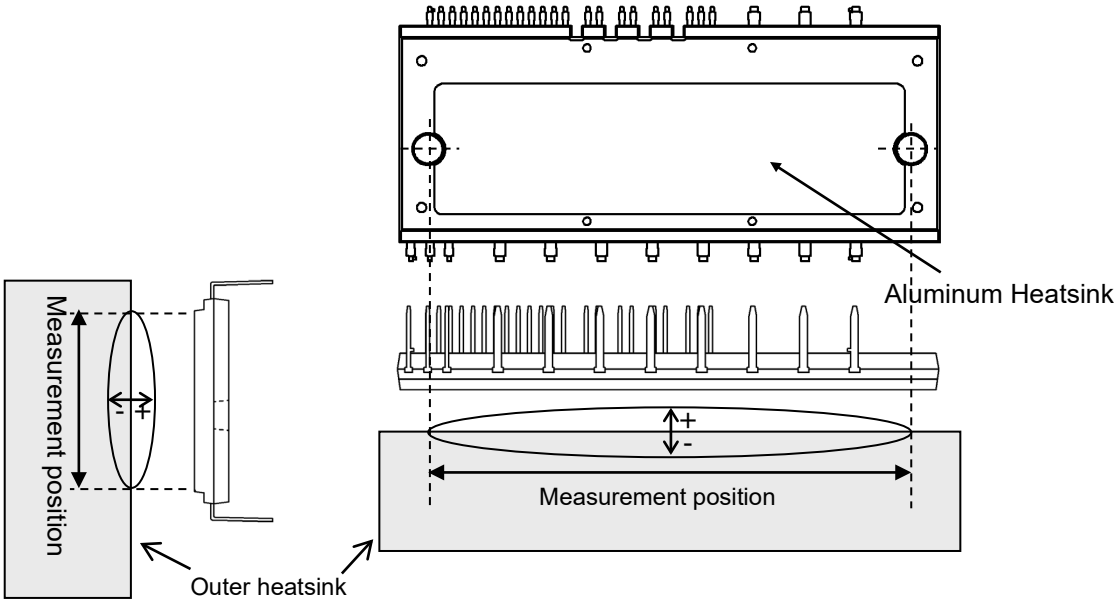


Fig.2-4-2 Measurement positions of heat radiation part flatness

In order to get effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally-conductive grease with 100μ-200μm thickness over the contact surface between a module and a heat sink, which is also useful for preventing corrosion. Furthermore, the grease should be with stable quality and long-term endurance within wide operating temperature range. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.25K/W (per chip, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in Table 2-4-3 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

The actual condition might need some adjustment based on its flow condition of solder, the speed of the conveyer, the land pattern and the through hole shape on the PCB, etc. It is necessary to confirm whether it is appropriate or not for your real PCB finally..

Table 2-4-3 Reliability test specification

Item	Condition
Soldering thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, the unambiguous hand soldering condition cannot be decided.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept less than 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

CHAPTER 3 : SYSTEM APPLICATION GUIDANCE

3.1 Application guidance

This chapter states the DIPIPM+ application method and interface circuit design hints.

3.1.1 System connection

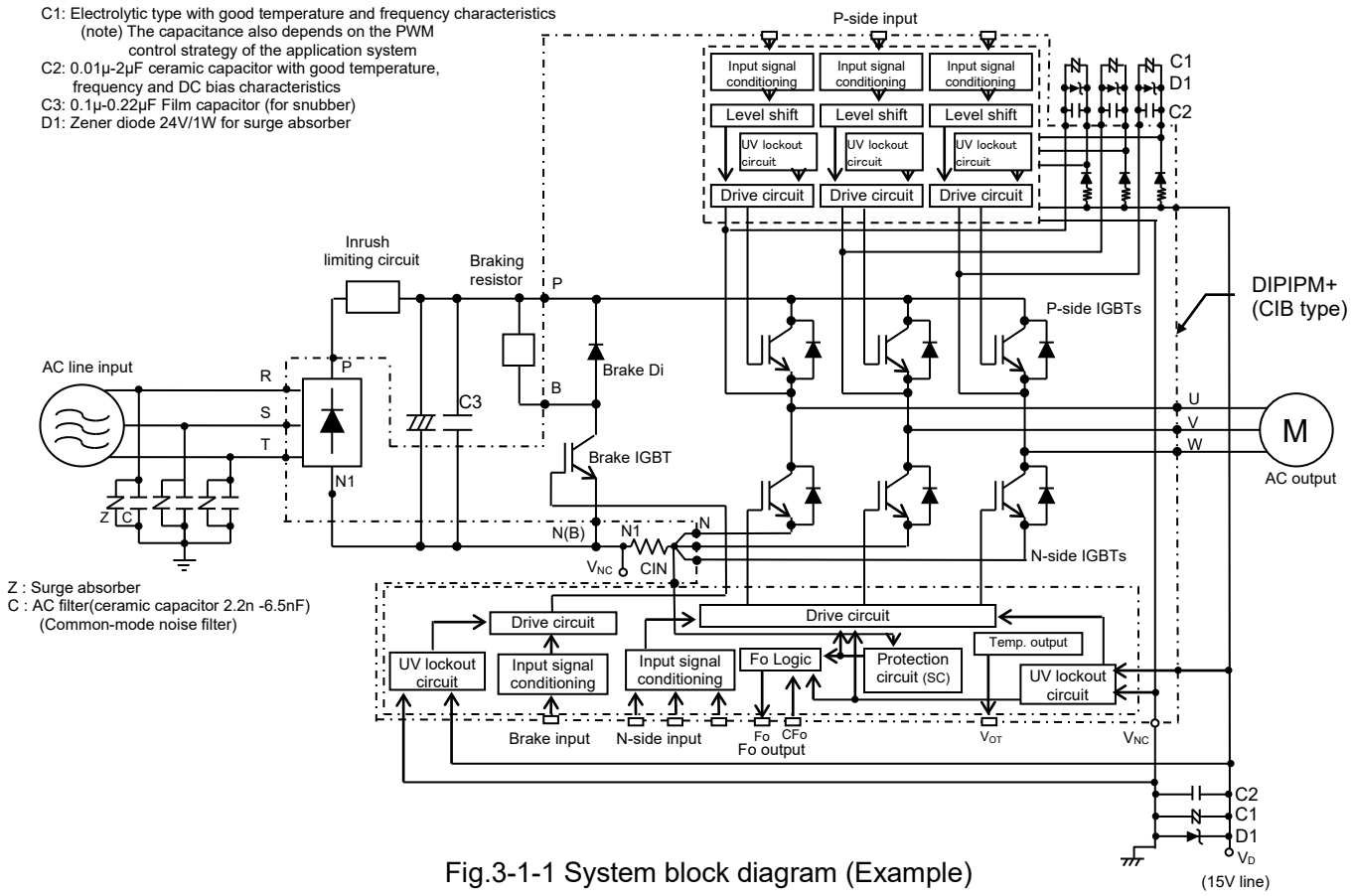


Fig.3-1-1 System block diagram (Example)

3.1.2 Interface Circuit (Direct Coupling Interface example for using one shunt resistor)

Fig.3-1-2 shows a typical application circuit of interface schematic, in which control signals are transferred directly input from a controller (e.g. MCU).

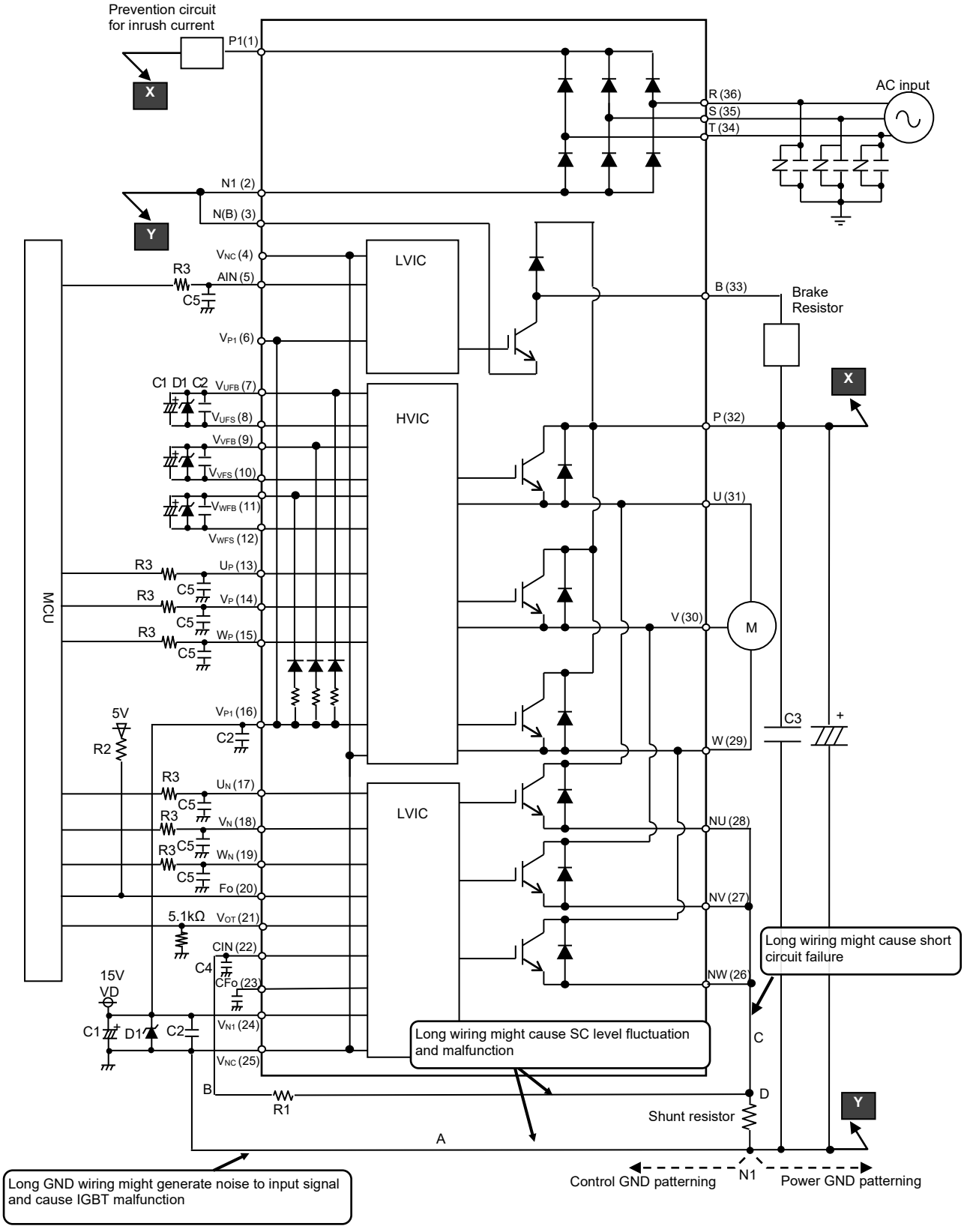


Fig.3-1-2 Interface circuit example in the case of using with one shunt resistor

Note for the previous application circuit:

(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is recommended generally.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected each other at near those three terminals when it is used by one shunt operation. Low inductance SMD type with tight tolerance, temp-compensated type is recommended for shunt resistor.
(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.01μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
(8) Input logic is High-active. There is a 3.3kΩ(min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the input wiring should be as short as possible. When using RC coupling, make the input signal level meet the turn-on and turn-off threshold voltage.
(9) Fo output is open drain type. Fo output will be max 0.95V(@I_{FO}=1mA,25°C), so it should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{FO}up to 1mA. (In the case of pulled up to 5V, 10kΩ is recommended.) About driving opto coupler by Fo output, please refer the application note of this series.
(10) Fo pulse width can be set by the capacitor connected to CFO terminal. C_{FO}(F) = 9.1 x 10^{-6} x t_{FO} (Required Fo pulse width).
(11) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple ≤ 2Vp-p.
(12) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.
(13) No.4 and No.25 V_{NC} terminals (GND terminal for control supply) are connected mutually inside of DIPIPM+ and also No.6 and No.16 V_{P1} terminals are connected mutually inside, please connect either No.4 or No.25 terminal to GND and also connect either No.6 or No.16 terminal to supply and make the unused terminal leave no connection.

3.1.3 Interface circuit (example of opto-coupler isolated interface)

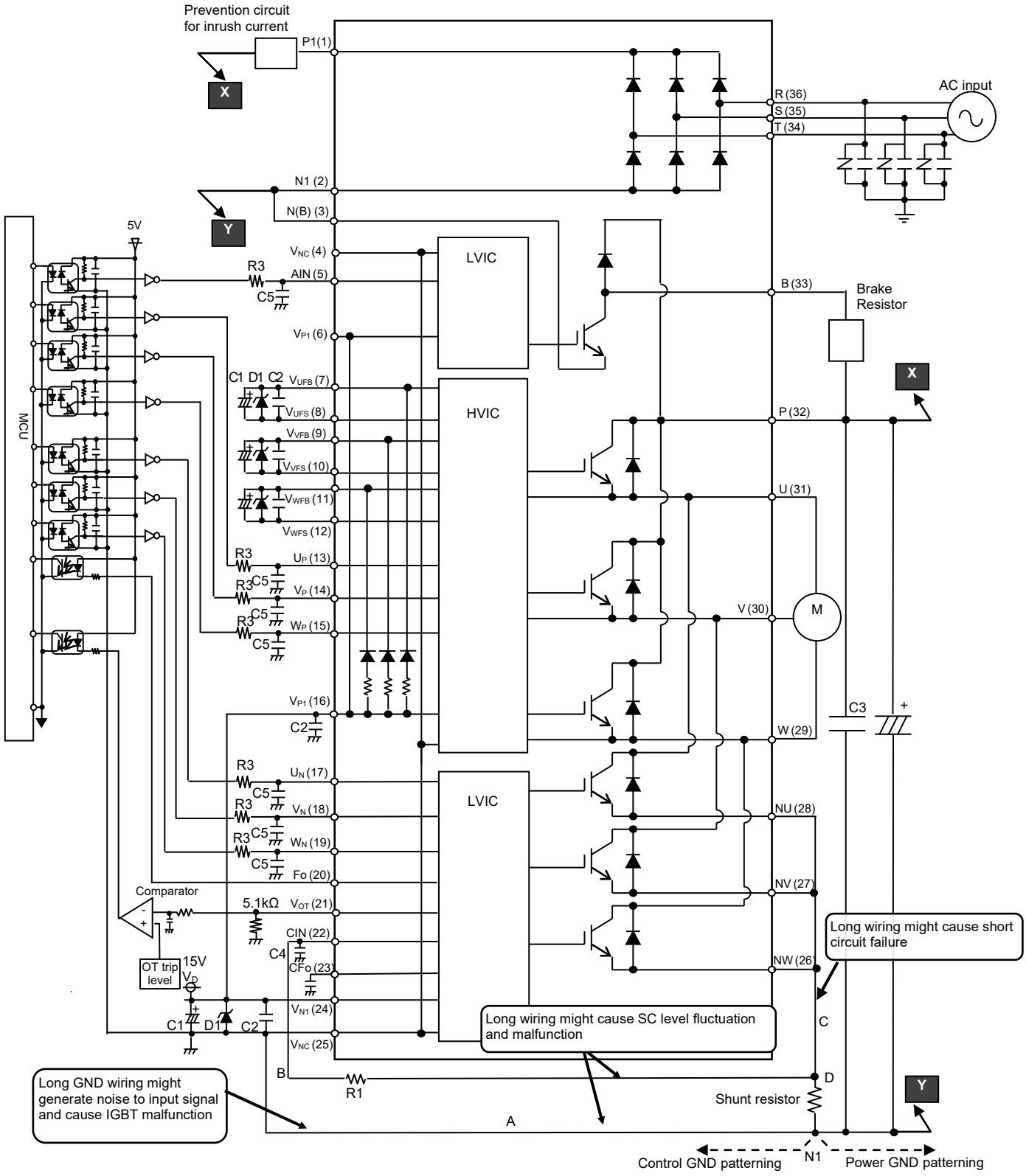


Fig.3-1-3 Interface circuit example with opto-coupler

(note)

(1) High speed (high CMR) opto-coupler is recommended.

(2) Set the current limiting resistance to make Fo sink current I_{FO}=5mA or less when the opto-coupler is driven by Fo output directly. To assure I_{FO}=5mA, it will be needed to pull up to 15V supply since Fo output may be max 4.75V (@I_{FO}=5mA, 25℃).

(3) To prevent malfunction, it is strongly recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet turn-on and turn-off threshold voltage.

(4) About comparator circuit at V_{OT} output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

3.1.4 External SC protection circuit with using three shunt resistors

When using three shunt resistor, protection circuit is described as following Fig.3-1-4.

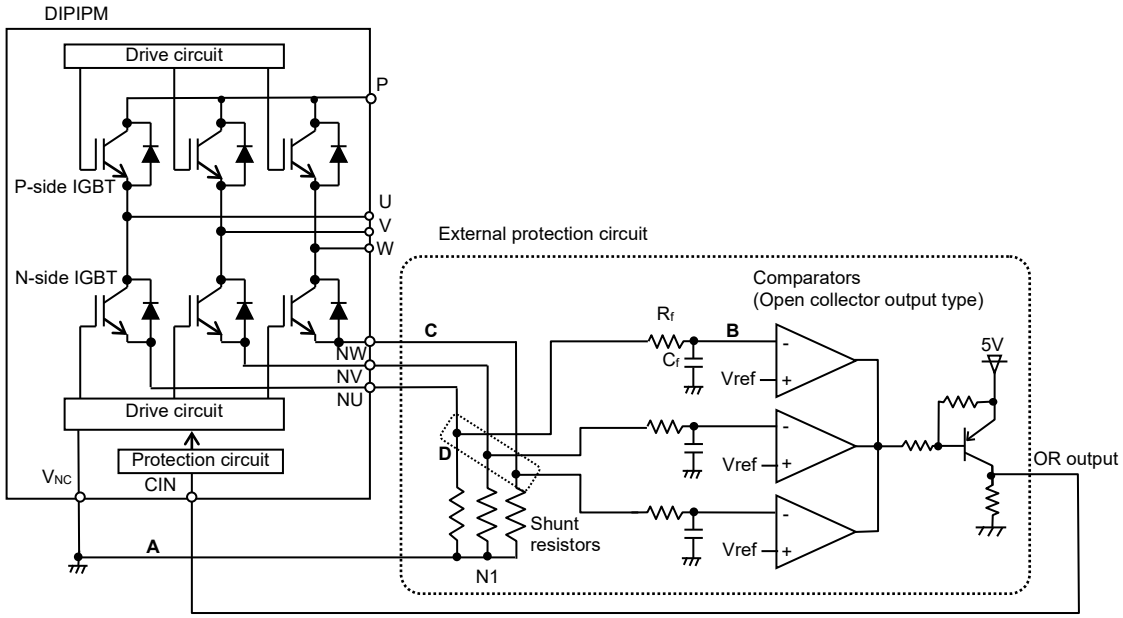


Fig.3-1-4 Interface circuit example

(note)

(1) It is necessary to set the time constant R_fC_f of external comparator input so that IGBT stop within 2μs when short circuit occurs.
(2) SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(3) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.48V).
(4) Select the external shunt resistance so that SC trip-level is less than specified value.
(5) To avoid malfunction, the wiring A, B and C should be designed as short as possible.
(6) The point D at which patterns are branched to each comparator should be closer to the terminal of shunt resistor.
(7) OR output high level should be more than 0.505V (=maximum Vsc(ref)).
(8) GND of Comparator, GND of Vref circuit and Cf should be connected to control GND wiring. (not to power GND)

3.1.5 Circuits of Signal Input Terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

DIPIPM is high-active input logic. 3.3kΩ(min) pull-down resistor is built-in each input circuits of the DIPIPM as shown in Fig.3-1-5 , so external pull-down resistor is not needed.

Furthermore, the turn-on and turn-off threshold voltage of input signal are as shown in Table 3-1-1 .

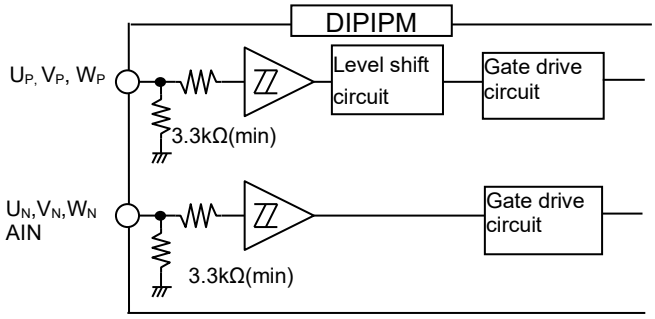


Fig.3-1-5 Internal structure of control input terminals

Table 3-1-1 Input threshold voltage ratings(Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{NC} terminals, U_N,V_N,W_N-V_{NC} terminals, AIN-V_{NC} terminal	—	—	3.5	V
Turn-off threshold voltage	Vth(off)		0.8	—	—	

(note)

(1) The wiring of each input should be patterned as short as possible. If the pattern is long and the noise is imposed on the pattern (e.g. Fig3-1-6), it may be effective to insert RC filter.
(2) There are limits for the minimum input pulse width in the DIPIPM. The DIPIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Table 3-1-2)

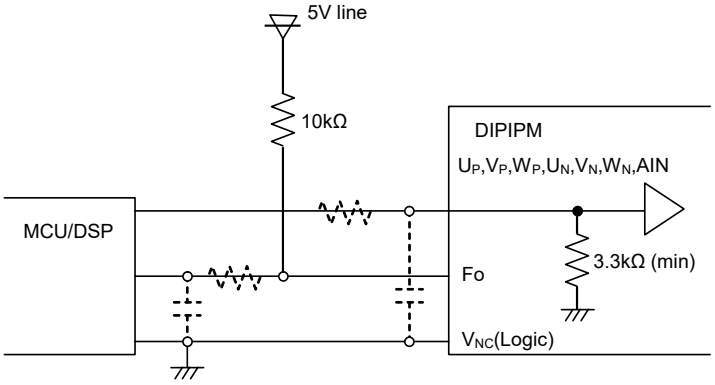


Fig.3-1-6 Control input connection

(note)

(1) The RC coupling (parts shown as broken line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.

(2) The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please be careful to the signal voltage drop at input terminal.

Table 3-1-2 Allowable minimum input pulse width

Item	Symbol	Condition		Min. value	Unit
Allowable minimum input pulse width	PWIN(on)	Up to 1.7 times of rated current		1.5	μs
	PWIN(off)	0≤V_{CC}≤800V(for 1200V series) or 0≤V_{CC}≤350V(for 600V series), 13.5≤V_D≤16.5V, 13.0≤V_{DB}≤18.5V, -20° C ≤Tc≤100° C, N line wiring inductance less than 10nH	Up to rated current	3	
			From rated current to 1.7 times of rated current	3.5	

(note)

(1) Input signal with ON pulse width less than PWIN(on) might make no response.

(2) IPM might make no response or delayed response for the input OFF signal with pulse width less than PWIN(off). (Delay occurs for p-side only.) Please refer the following Fig.3-1-7 of delayed response.

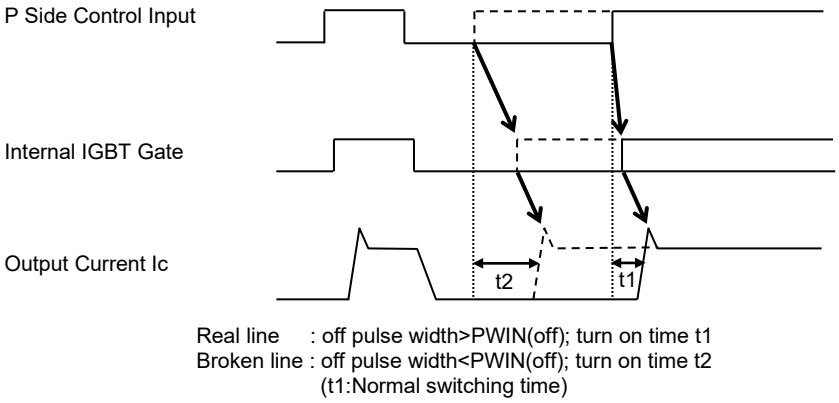


Fig.3-1-7 Delayed response of output operation with inputting less than PWIN(OFF) for P-side

(2) Internal circuit of Fo terminal

Fo terminal is an open drain type. When Fo output is input into MCU(controller) directly, it is necessary to note the dependency of V_{FO} on I_{FO} (V_{FO}=max0.95V @I_{FO}=1mA, 25°C) and set pull up resistance so that Fo signal level fits to the input threshold voltage of MCU. In the case of pulling up to 5V supply, it is recommended to pull up by 10kΩ resistor.

When the opto-coupler is driven by Fo output directly, the maximum Fo sink current becomes 5mA or less. To assure I_{FO}=5mA, it will be needed to pull up to 15V supply since Fo output may be max 4.75V (@I_{FO}=5mA, 25°C).

If max 5mA coupler driving current is not enough, it is necessary to apply buffer circuit for increasing driving current.

Table 3-1-3 shows the typical V-I characteristics of Fo terminal.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V, Fo=10kΩ 5V Pulled-up	4.9	—	—	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA	—	—	0.95	V

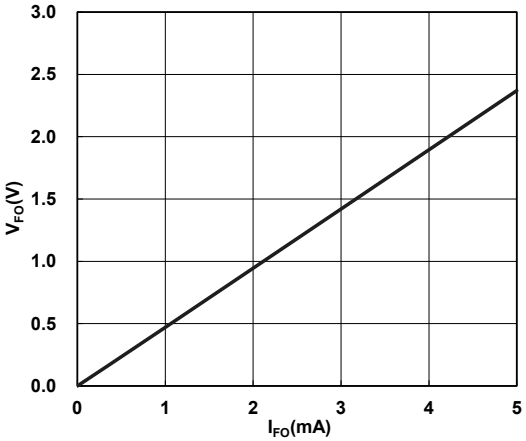


Fig.3-1-8 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.6 Snubber circuit

In order to prevent DIPIPM from destruction by extra surge, the wiring length between the smoothing capacitor and P terminal (DIPIPM) – N1 points (shunt resistor terminal) should be designed as short as possible. Also, a 0.1μ~0.22μF snubber capacitor with high withstanding voltage should be mounted in the DC-link and close to P and N1.

In order to suppress the surge voltage maximally, the wiring at part-A (including shunt resistor parasitic inductance) should be designed as small as possible as shown in Fig.3-1-9.

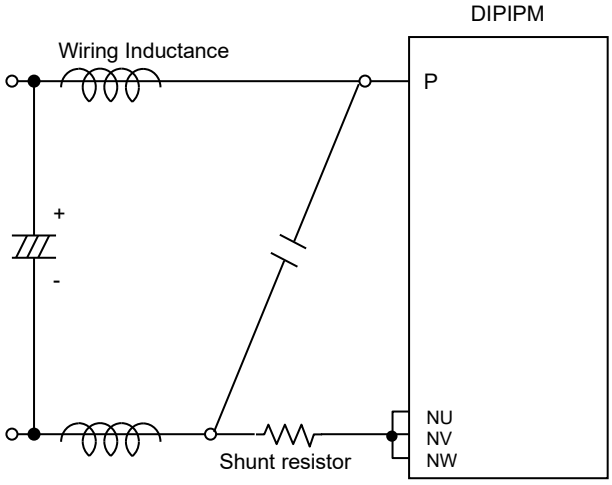


Fig.3-1-9 Recommended snubber circuit location

3.1.7 Recommended wiring method around shunt resistor

External shunt resistor is necessary to detect short-circuit accident. If applied a longer patterning between the shunt resistor and DIPIPM, it causes so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt resistor and DIPIPM should be connected as short as possible and using low inductance resistor such as SMD (Surface Mounted Device) resistor instead of long-lead resistor.

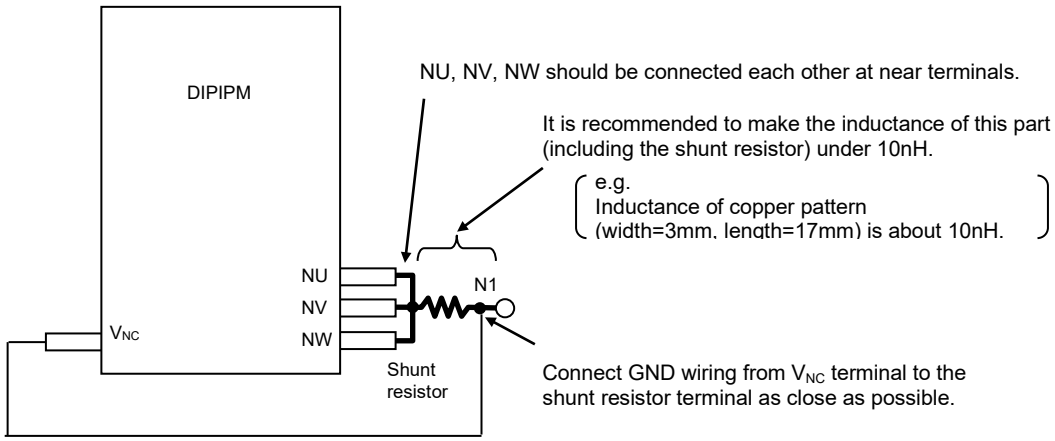


Fig.3-1-10 Wiring instruction (In the case of using with one shunt resistor)

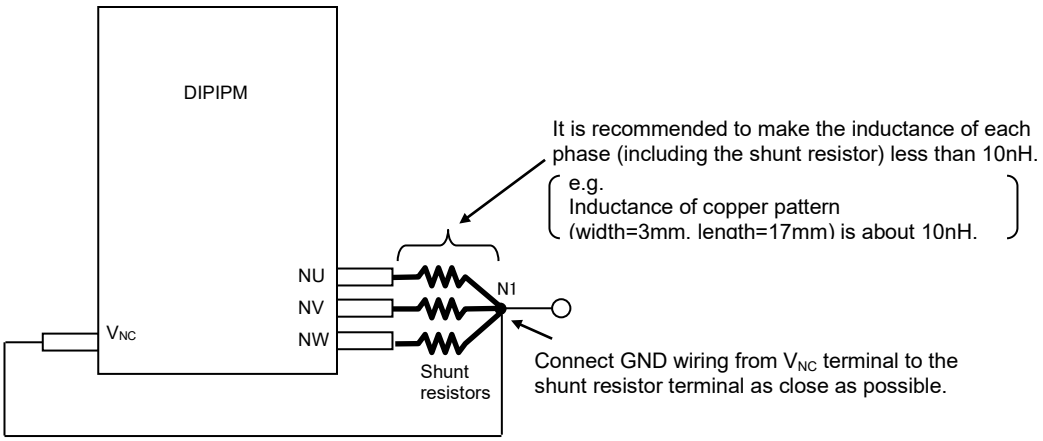


Fig.3-1-11 Wiring instruction (In the case of using with three shunt resistors)

Influence of pattern wiring around the shunt resistor is shown below.

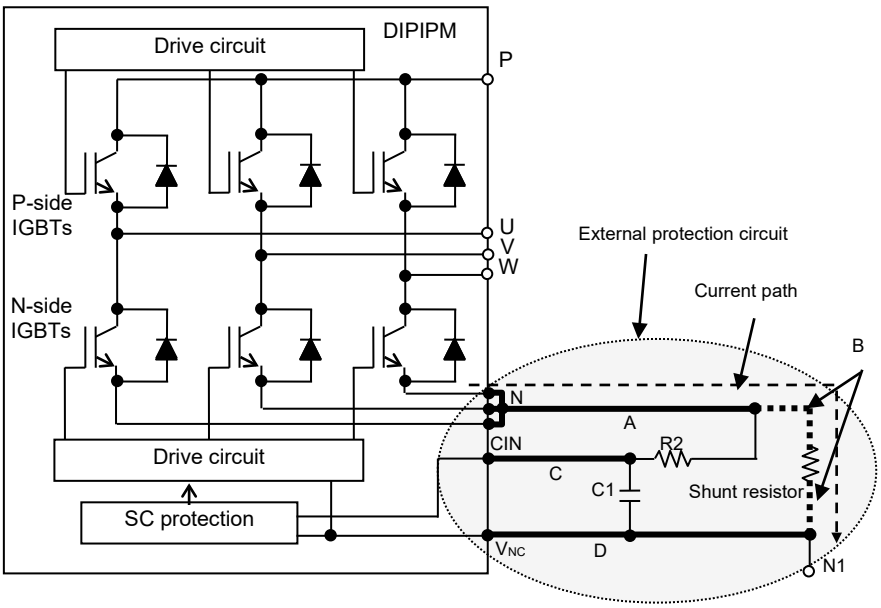


Fig.3-1-12 External protection circuit

(1) Influence of the part-A wiring

The ground of N-side IGBT gate is V_{NC}. If part-A wiring pattern in Fig.3-1-12 is too long, extra voltage generated by the wiring parasitic inductance will result the potential of IGBT emitter variation during switching operation. It is necessary to locate shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring in Fig.3-1-12 affects SC protection level. SC protection works by detecting the voltage of the CIN terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. It is necessary to connect CIN and V_{NC} terminals directly to the two ends of shunt resistor and avoid long wiring.

(3) Influence of the part-C wiring pattern

C1R2 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring in Fig.3-1-12 is too long. It is necessary to install the C1R2 filter near CIN, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern in Fig.3-1-12 gives influence to all the items described above, maximally shorten the GND wiring is expected.

3.1.8 SOA of DIPIPM+ at switching state

The SOA (Safety Operating Area) of DIPIPM+ series are described as follows;

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : DC-link voltage applied on P-N terminals

$V_{CC(surge)}$: Voltage between P and N terminals including surge voltage which will be generated due to wiring inductance between DIPIPM and DC-link capacitor at switching state.

$V_{CC(PROT)}$: Maximum DC-link voltage in which DIPIPM can protect itself when short circuit happens.

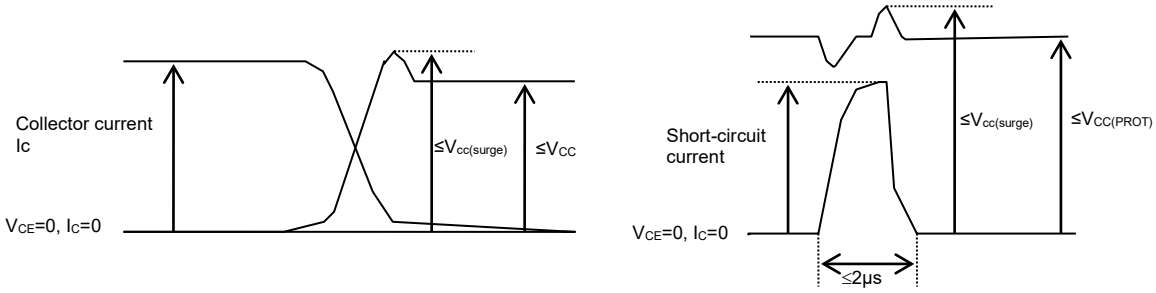


Fig.3-1-13 SOA at switching mode and short-circuit mode

In case of switching

V_{CES} is the maximum voltage rating of IGBTs for 1200V (or 600V) as withstanding voltage. $V_{CC(surge)}$ is specified to maximum 1000V (or 500V) subtracted 200V or less (or 100V or less) of surge voltage by internal wiring inductance of DIPIPM+ from V_{CES}. Furthermore, also V_{CC} is specified to maximum 900V (or 450V) because it should be considered about surge voltage by wiring inductance between DIPIPM+ terminals and DC-link capacitor, then the maximum Vcc is subtracted 100V (or 50V) from $V_{CC(surge)}$ as the margin.

In case of short-circuit

V_{CES} and V_{CC}(surge) are same definition as the case of switching. Vcc is specified to 800V (or 400V) because it should be considered about larger surge voltage by wiring inductance at the turning off short-circuit current, then maximum Vcc is subtracted 200V (or 100V) from $V_{CC(surge)}$ as the margin.

(note)

The above value in parentheses is for 600V rating products.

3.1.9 SCSOA

Fig.3-1-14~19 show the typical SCSOA performance curves of each products.

The measurement condition is described as follows;
(1) for 1200V series, V_{CC}=800V, Tj=125°C at initial state, $V_{CC(surge)}$≦1000V(surge included), non-repetitive,2m load.
(2) for 600V series, V_{CC}=400V, Tj=125°C at initial state, $V_{CC(surge)}$≦500V(surge included), non-repetitive,2m load.

Please refer Fig.3-1-17 for PSS25MC1FT(25A/1200V CIB type), for instance. It shows DIPIPM+ can safely shut down an SC current which is about 10 times of its current rating under above conditions, when the IGBT shuts off by 4.6μs at V_D=16.5V. Since the SCSOA (Short Circuit Safety Operating Area) will vary with the control supply voltage, DC-link voltage, and so on, it is necessary to set time constant of RC filter with a margin.

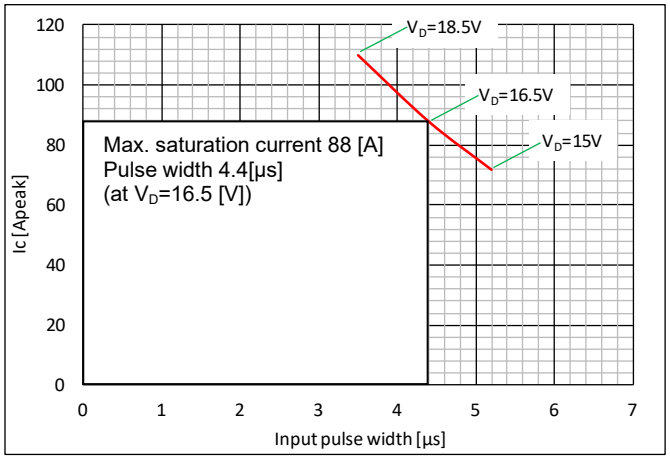


Fig.3-1-14 Typical SCSOA curve of PSS05M(N)C1FT

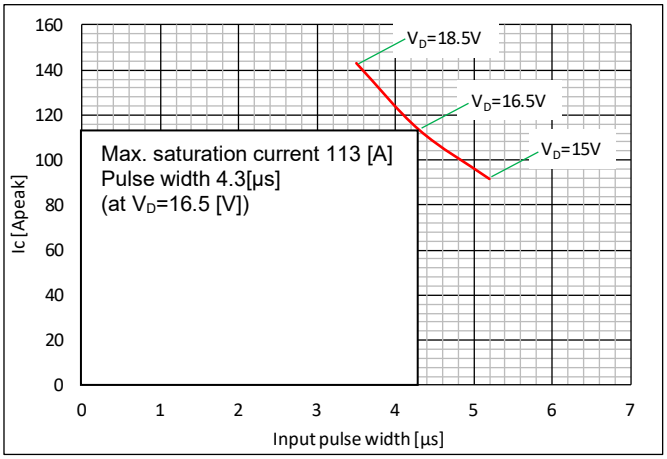


Fig.3-1-15 Typical SCSOA curve of PSS10M(N)C1FT

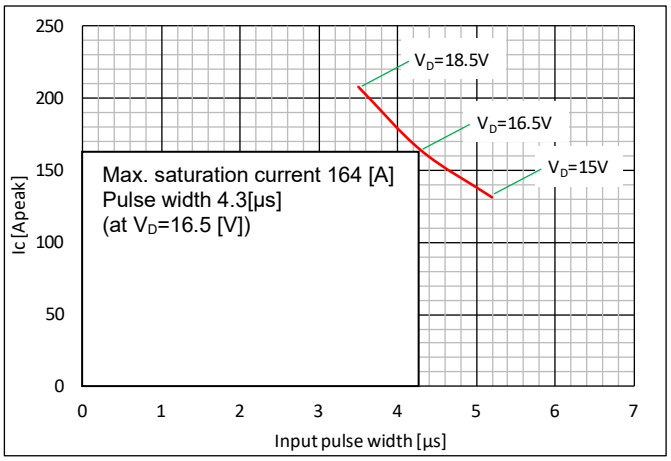


Fig.3-1-16 Typical SCSOA curve of PSS15M(N)C1FT

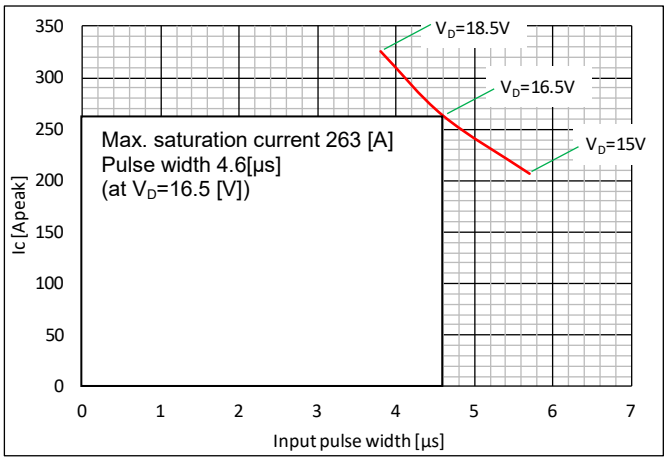


Fig.3-1-17 Typical SCSOA curve of PSS25M(N)C1FT

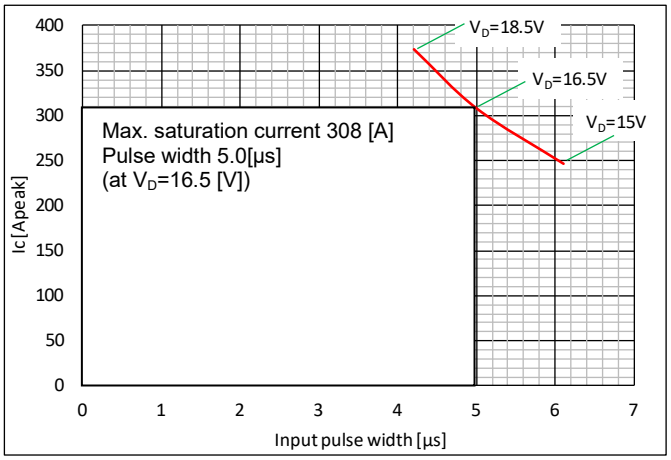


Fig.3-1-18 Typical SCSOA curve of PSS35M(N)C1FT

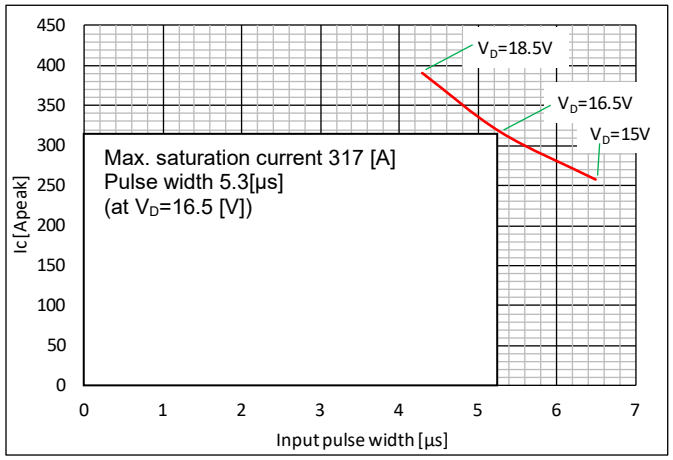


Fig.3-1-19 Typical SCSOA curve of PSS50M(N)C1F6

3.1.10 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-1-20 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj). (The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

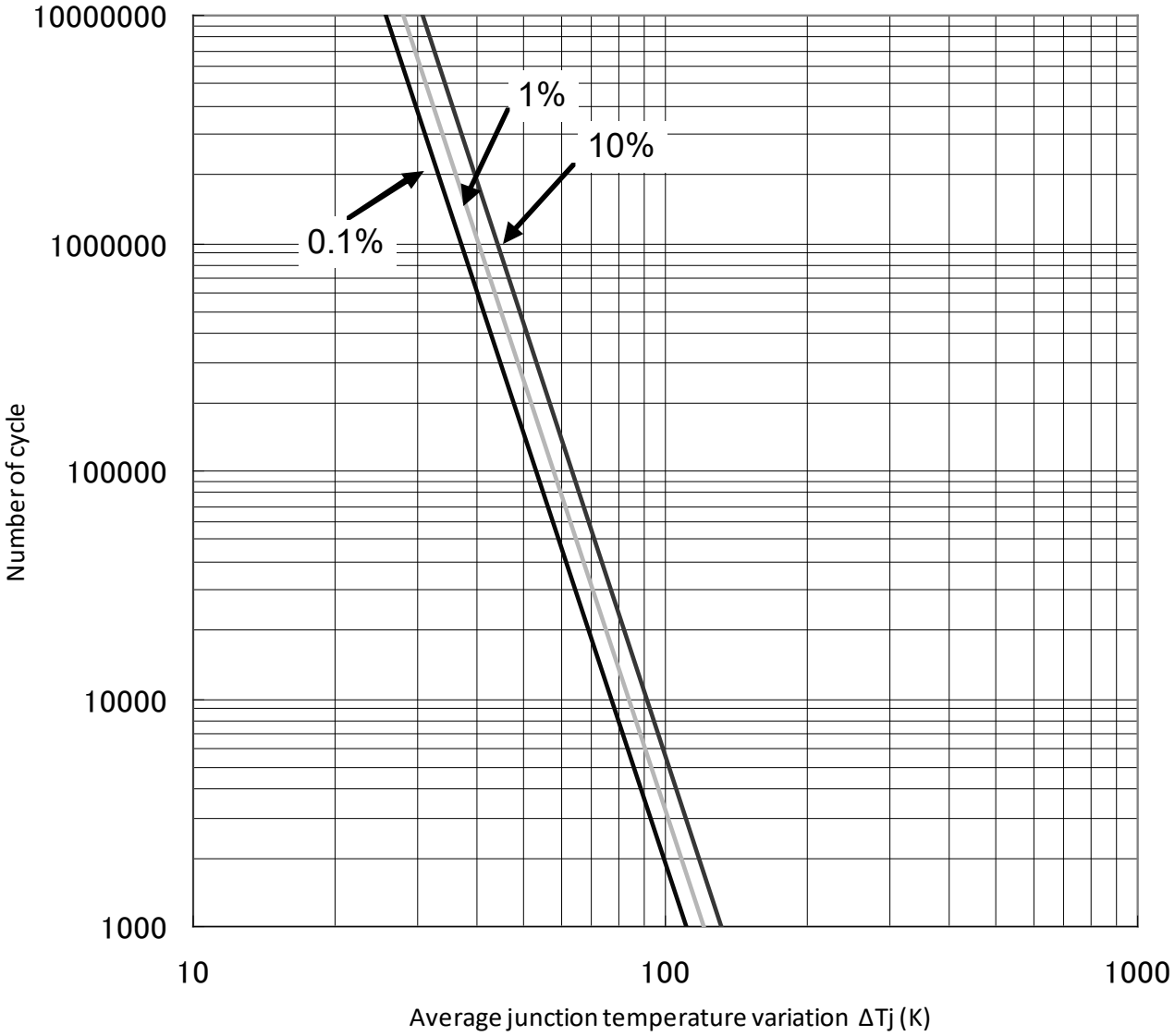


Fig.3-1-20 Power cycle curve

3.2 Power loss and thermal dissipation calculation

3.2.1 Power loss calculation

Simple expressions for calculating average power loss are given as follows;

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$

$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\, Icp \times \sin x)$$
$$Vec = (-1) \times Vec(@\, Iecp(= Icp) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Icp \times \sin x) \times Vce(sat)(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} ((-1) \times Icp \times \sin x)((-1) \times Vec(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Psw(on)(@\, Icp \times \sin x) + Psw(off)(@\, Icp \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

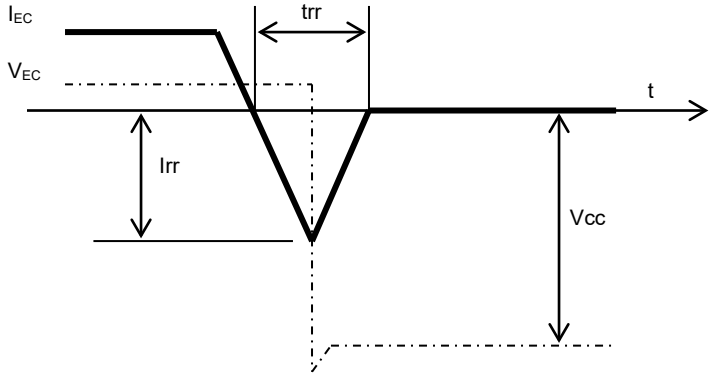


Fig.3-2-1 Ideal FWDi recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

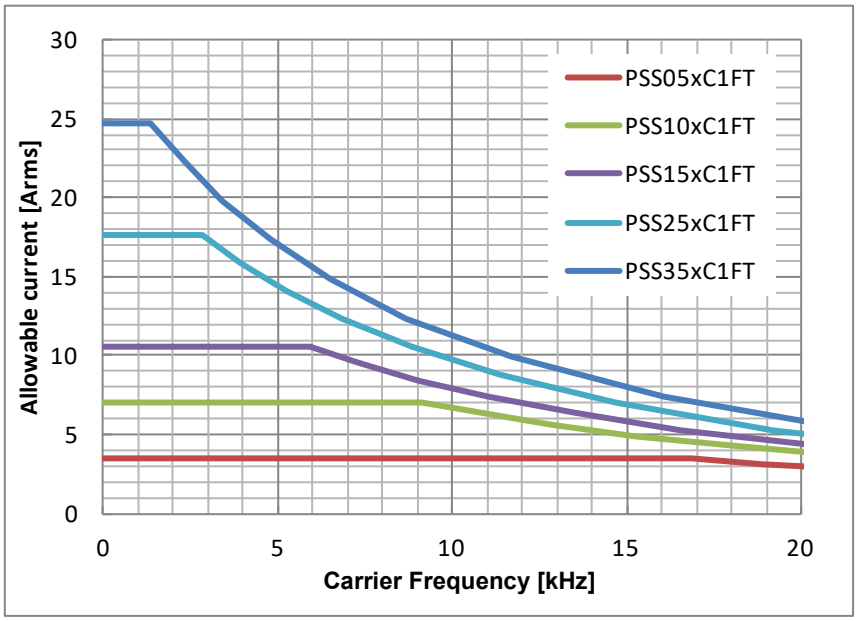
Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x)}{4} \times fc \bullet dx$$
$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at T_j=125°C.

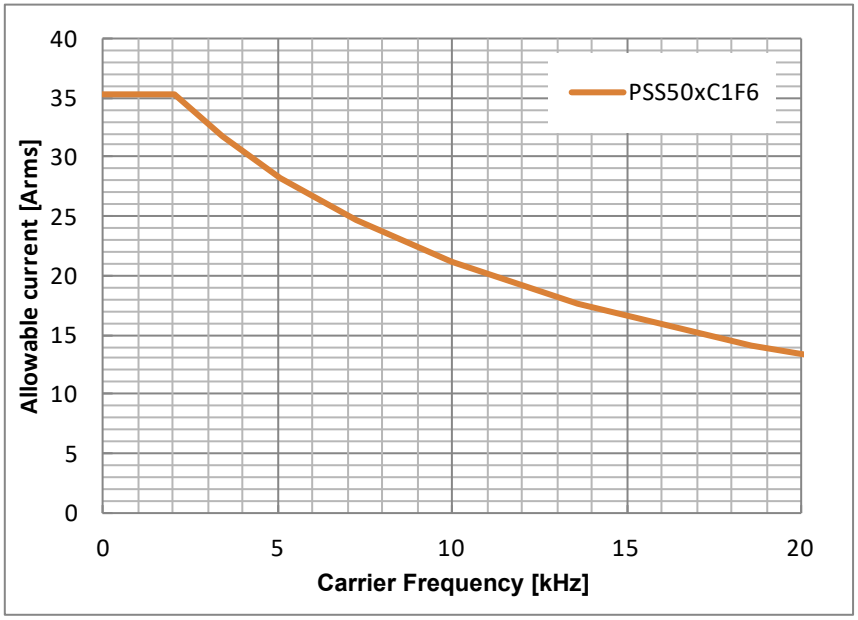
3.2.2 DIPIPM+ performance according to carreir frequency

Fig.3-2-2 shows the typical characteristics of allowable effective current vs. carrier frequency under the following inverter operating conditions based on power loss simulation results for DIPIPM+ 1200V series. And Fig.3-2-3 shows for PSS50xC1F6.



[Calculation condition for PSSxxxC1FT]
V_{CC}=600V, V_D=V_{DB}=15V,
$V_{CE(sat)}$=Typ., Switching loss=Typ.,
T_j=125°C, T_c=100°C, ΔT_{j-c}=25K
$R_{th(j-c)}$=Max.
P.F=0.8, 3-phase PWM modulation,
60Hz sine waveform output

Fig.3-2-2 Effective current-carrier frequency characteristics



[Calculation condition for PSS50xC1F6]
V_{CC}=300V, V_D=V_{DB}=15V,
$V_{CE(sat)}$=Typ., Switching loss=Typ.,
T_j=125°C, T_c=100°C, ΔT_{j-c}=25K
$R_{th(j-c)}$=Max.
P.F=0.8, 3-phase PWM modulation,
60Hz sine waveform output

Fig.3-2-3 Effective current-carrier frequency characteristics

Fig.3-2-2 and Fig.3-2-3 show one of the example of estimating allowable inverter output effective current with different carrier frequency and allowable maximum operating temperature condition (T_c=100°C. T_j=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The inverter loss can be calculated by the free power loss simulation software which is uploaded on the web site.
URL: http://www.MitsubishiElectric.com/semiconductors/

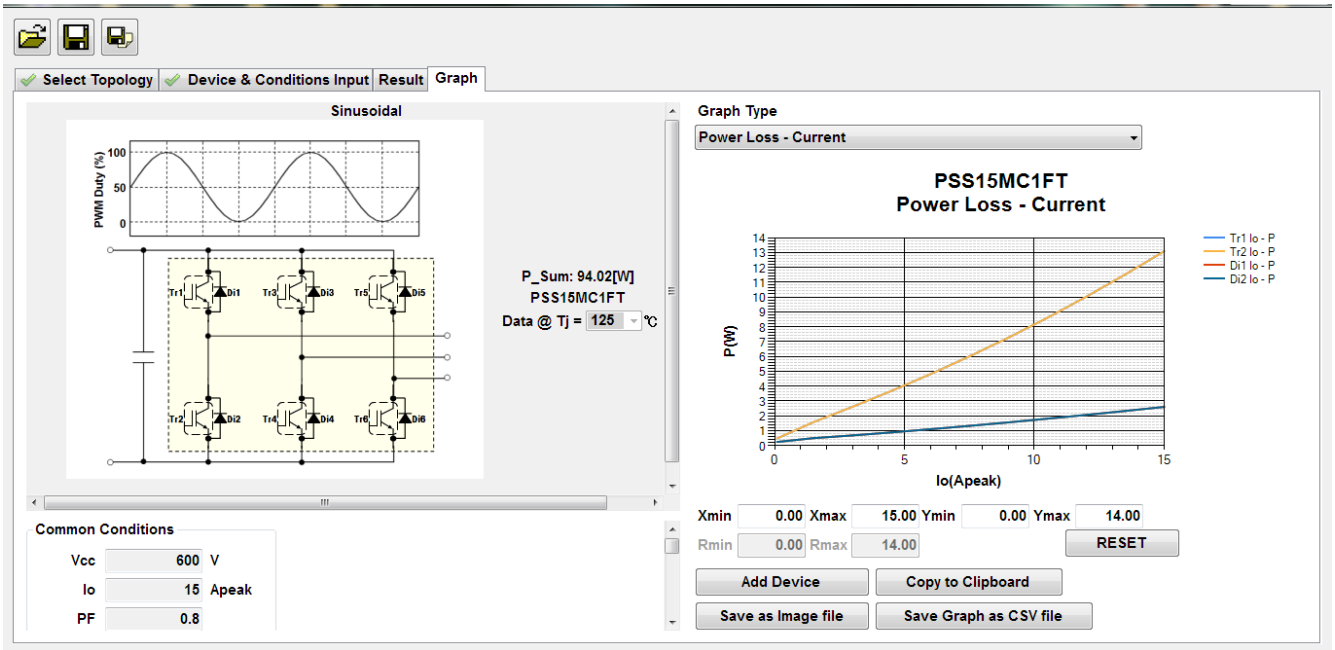


Fig.3-2-4 Loss simulator screen image

3.3 Noise and ESD withstand capability

3.3.1 Evaluation circuit of noise withstand capability

DIPIPM+ series have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-3-1. However noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout and other factors, it is recommended to conduct enough evaluation using prototype product.

[Condition]
(1) For 1200V series; V_{CC}=600V, V_D=15V, T_a=25°C, no load
(2) For 600V series; V_{CC}=300V, V_D=15V, T_a=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

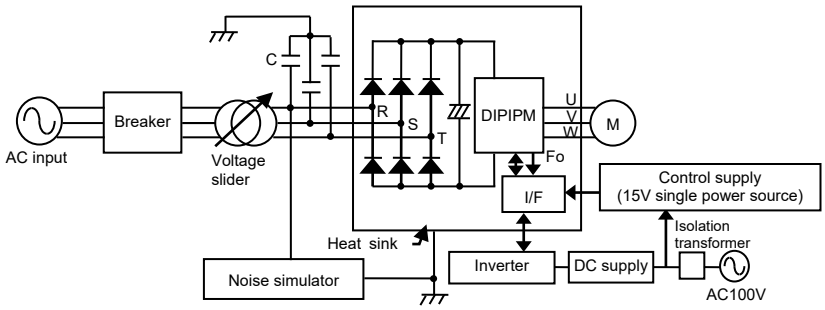


Fig.3-3-1 Noise withstand capability evaluation circuit

(note)
C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

3.3.2 Countermeasures and precautions

DIPIPM+ series are improved of noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, below countermeasures are recommended.

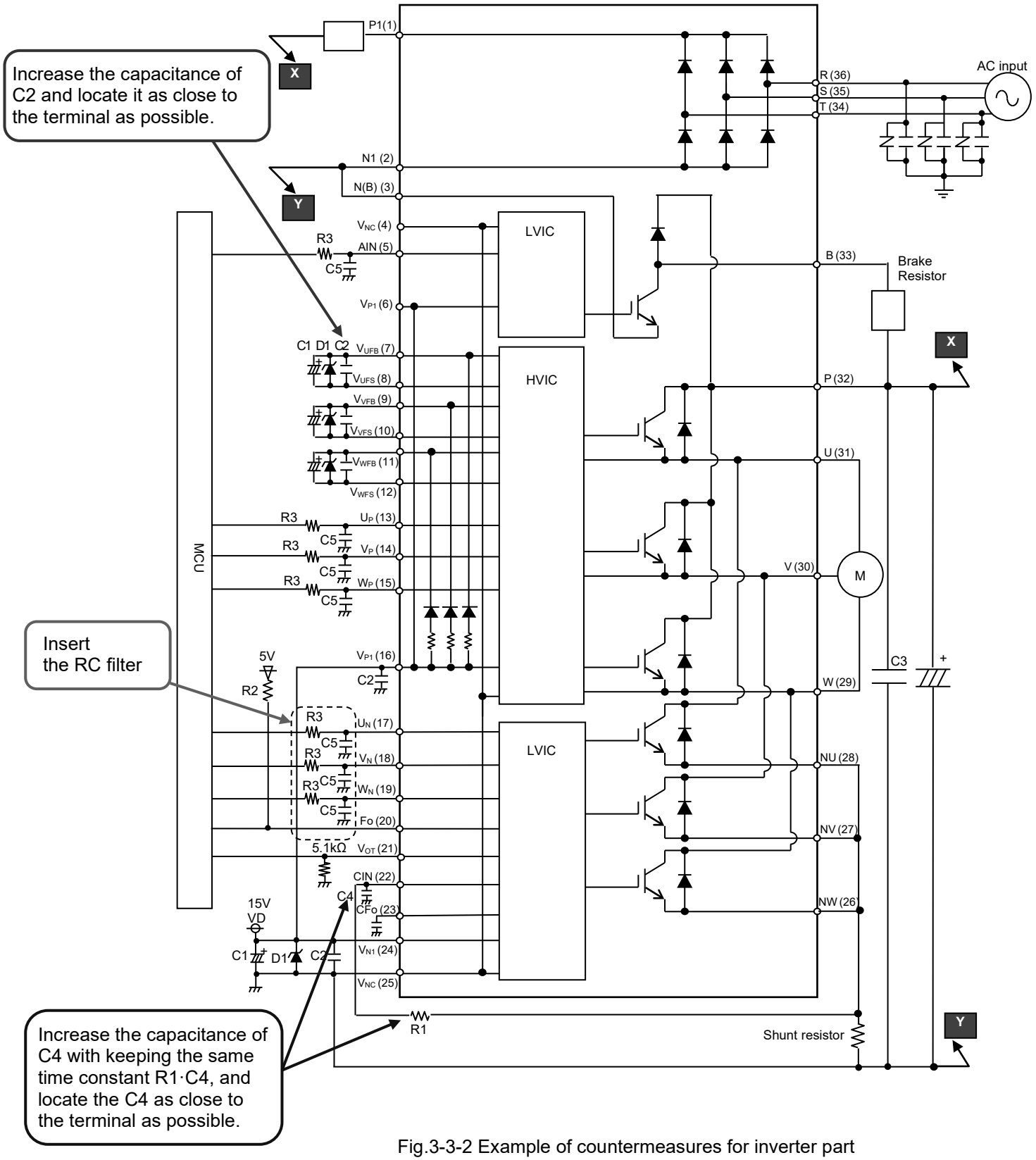


Fig.3-3-2 Example of countermeasures for inverter part

3.3.3 Static electricity withstand capability

Typical static electricity withstand capability by Machine Model(R=0Ω, C=200pF) is described as follows and the result is described as following Table 3-3-1 and 2.

Conditions: Surge voltage increases by degree and one surge pulse is impressed at each surge voltage.
(Limit voltage of surge simulator: ±4.0kV, Judged by change in V-I characteristic)

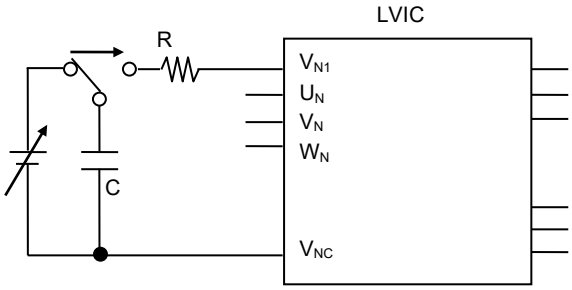


Fig.3-3-3 Surge test circuit example (V_{N1} terminal)

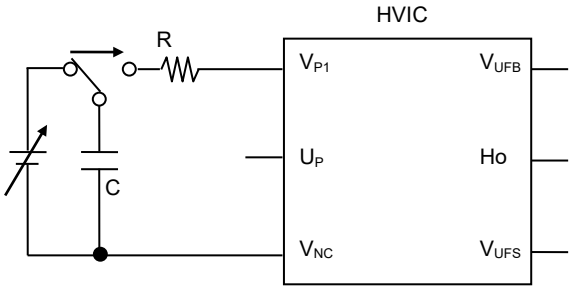


Fig.3-3-4 Surge test circuit example (V_{P1} terminal)

Table 3-3-1 PSSxxxC1Fx Typical ESD capability (MM)

[Control part for Inverter]

Evaluated terminals	+ Polarity	- Polarity	Unit
V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	2.7	2.7	kV
UP, VP, WP-V_{NC}	0.7	0.9	
V_{P1}-$V_{NC(PC)}$	3.0	3.5	
UN, VN, WN-V_{NC}	0.8	0.8	
V_{N1}-V_{NC}	4.0 or more	4.0 or more	
Fo-V_{NC}	0.8	1.2	
CIN-V_{NC}	0.8	1.0	
V_{OT}-V_{NC}	0.9	1.4	
CFo-V_{NC}	1.1	1.2	

[Power part for Inverter]

Evaluated terminals	+ Polarity	- Polarity	Unit
P-NU,NV,NW	4.0 or more	4.0 or more	kV
U-NU, V-NV, W-NW	4.0 or more	4.0 or more	

[Power part for Converter]

Evaluated terminals	+ Polarity	- Polarity	Unit
P1-N1	4.0 or more	4.0 or more	kV
R, S, T-N1	4.0 or more	4.0 or more	

Table 3-3-2 PSSxxMC1Fx Typical ESD capability (MM)

[Control part for Brake]

Evaluated terminals	+ Polarity	- Polarity	Unit
V_{P1}-V_{NC}	3.0	3.5	kV
AIN-V_{NC}	0.8	0.8	

[Power part for Brake]

Evaluated terminals	+ Polarity	- Polarity	Unit
P-N(B)	4.0 or more	4.0 or more	kV
B-N(B)	4.0 or more	4.0 or more	
P-B	2.7	4.0 or more	

CHAPTER 4 : Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, it requires four isolated control supplies for driving three P-side ICs and one N-side IC. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one, it requires N-side control supply only.

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor. DIPIPM+ series integrates BSD and limiting resistor, so it can make bootstrap circuit by adding outer BSC only. The BSC works as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-1-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. The BSC cannot be charged enough depending on its switching condition, BSC capacitance and so on. Deficient charge leads to too low voltage of BSC and might work “under voltage protection” (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "Bootstrap Circuit Design Manual"

The BSD characteristics for DIPIPM+ series and the circuit current characteristics in switching situation of P-side IGBT are described as follows.

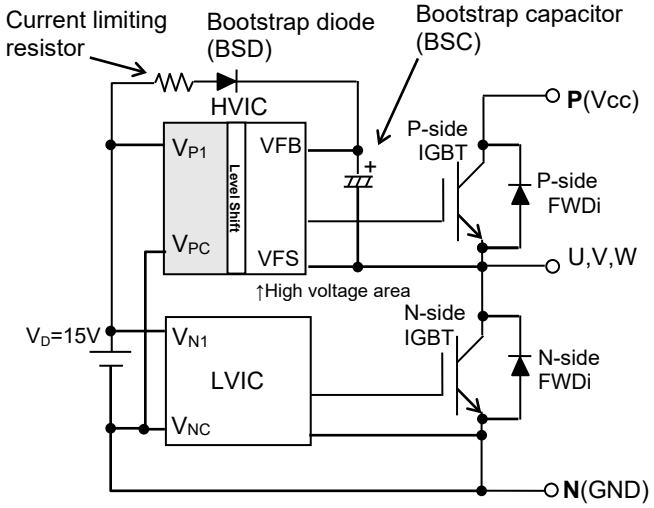


Fig.4-1-1 Bootstrap Circuit Diagram

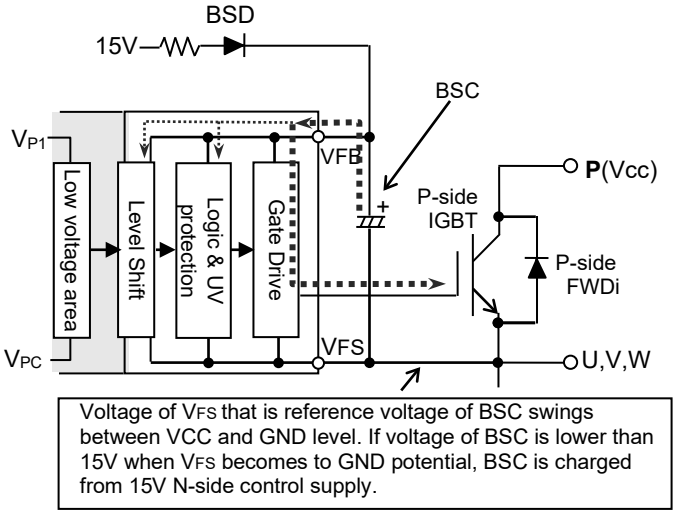


Fig.4-1-2 Bootstrap Circuit Diagram

4.2 Bootstrap supply circuit current at switching state

Bootstrap supply circuit current I_{DB} at steady state is 0.55mA maximum. At switching state, the circuit current exceeds 0.55mA and increases proportional to carrier frequency, because gate charge and discharge are repeated at each switching state. Fig.4-2-1~6 show typical I_{DB} vs. carrier frequency fc characteristics for DIPIPM+ series.

[Condition]
(1) For 1200V series, V_{CC}=800V, V_D=V_{DB}=15V, Tj=125°C, Duty=50%
(2) For 600V series, Vcc=400V, V_D=V_{DB}=15V, Tj=125°C, Duty=50%

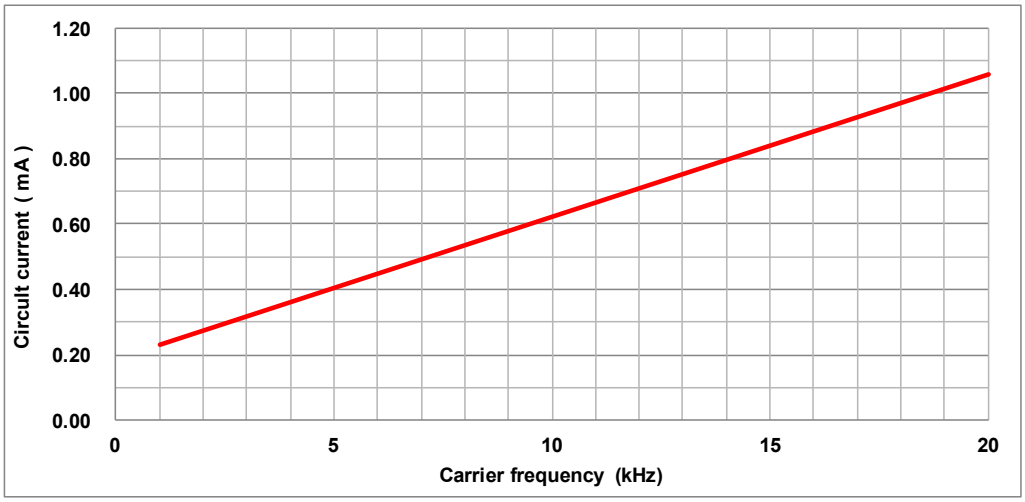


Fig. 4-2-1. I_{DB} vs. Carrier frequency for PSS05M(N)C1FT

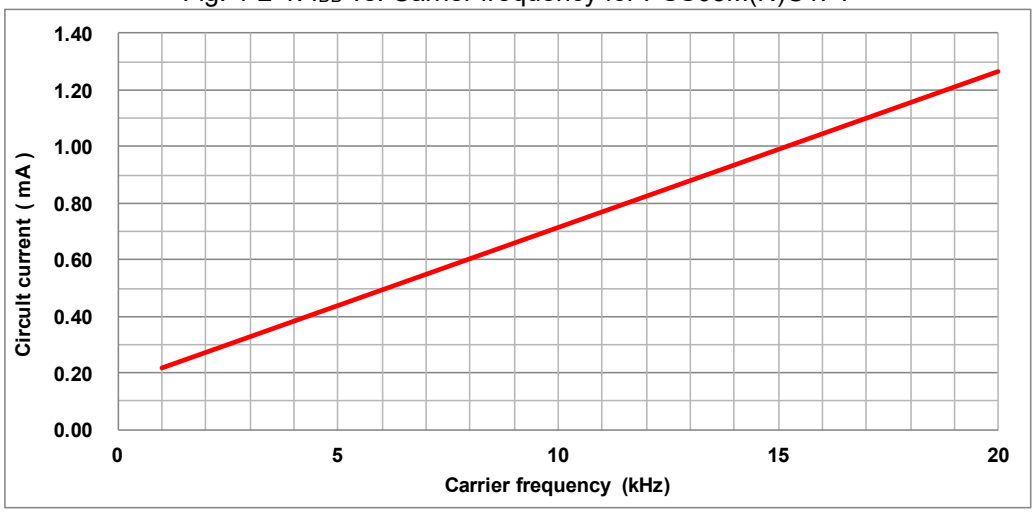


Fig. 4-2-2. I_{DB} vs. Carrier frequency for PSS10M(N)C1FT

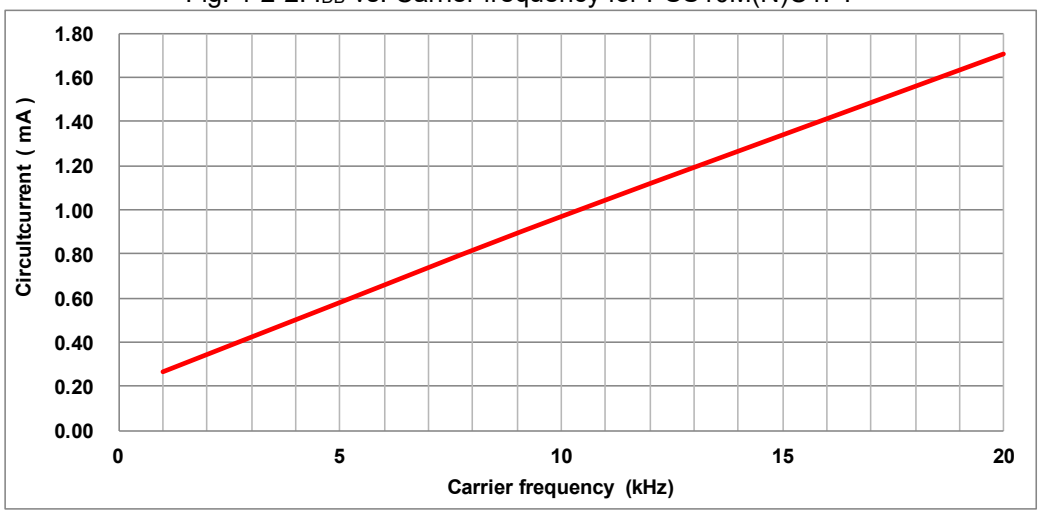


Fig. 4-2-3. I_{DB} vs. Carrier frequency for PSS15M(N)C1FT

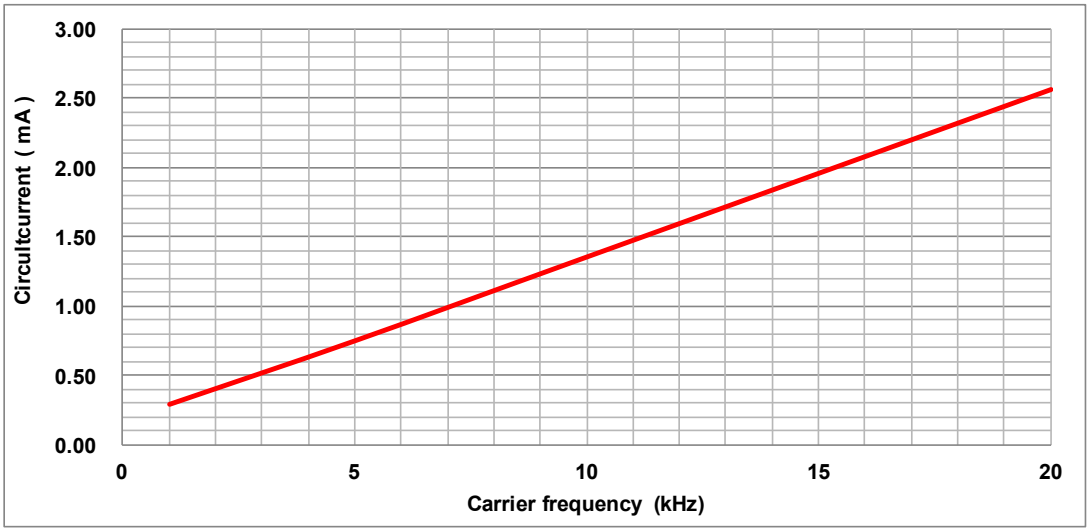


Fig. 4-2-4. I_{DB} vs. Carrier frequency for PSS25M(N)C1FT

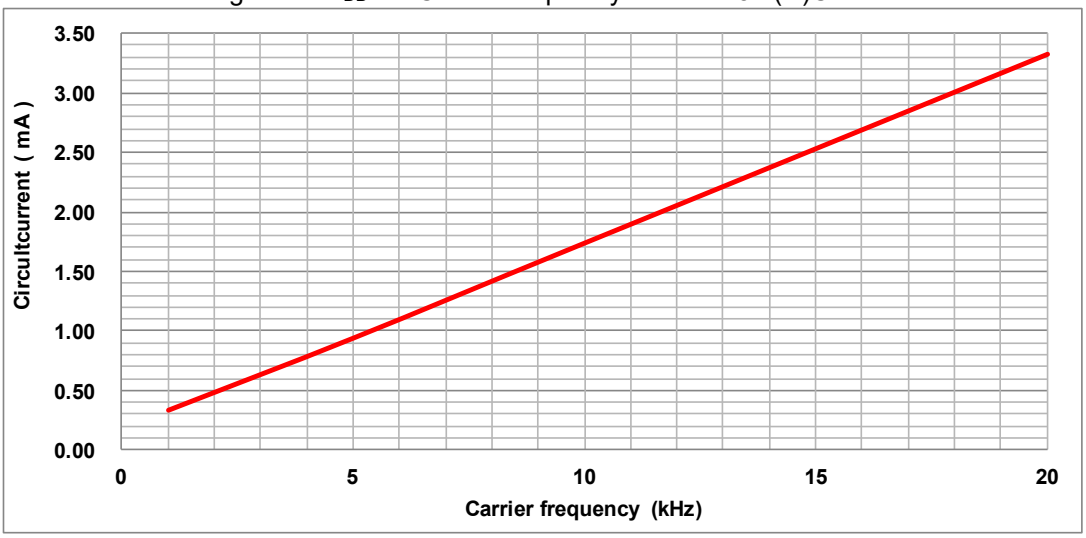


Fig. 4-2-5. I_{DB} vs. Carrier frequency for PSS35M(N)C1FT

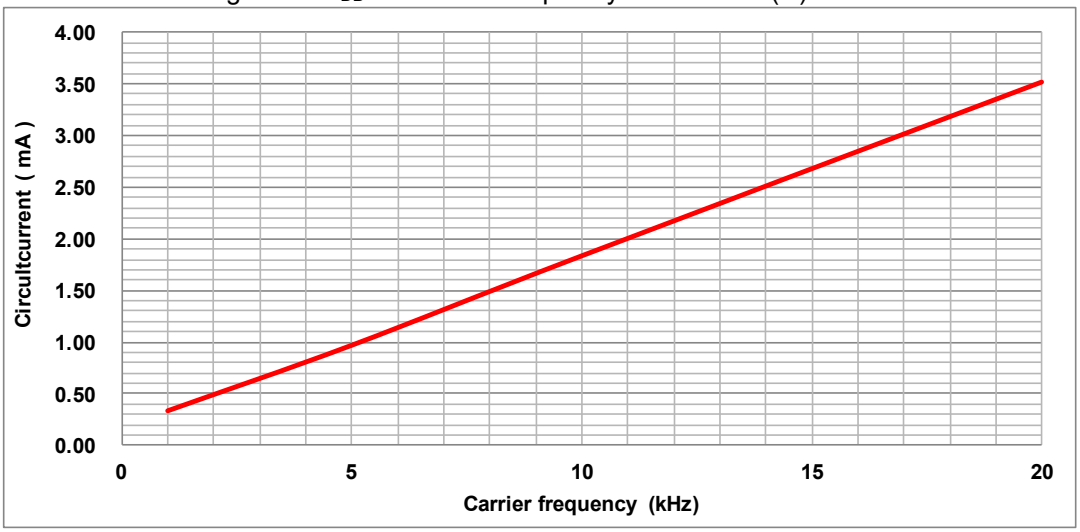


Fig. 4-2-6. I_{DB} vs. Carrier frequency for PSS50M(N)C1F6

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "Bootstrap Circuit Design Manual"

(1) Bootstrap capacitor

BSC employs electrolytic capacitors in general, and recently ceramic capacitor with large capacitance is also applied to it. Please note that DC bias characteristic is considerably different between electrolytic capacitor and of ceramic capacitor when applying DC voltage. Its characteristics especially differ with large capacitance type. Table 4-3-1 shows example of difference between the above two capacitors.

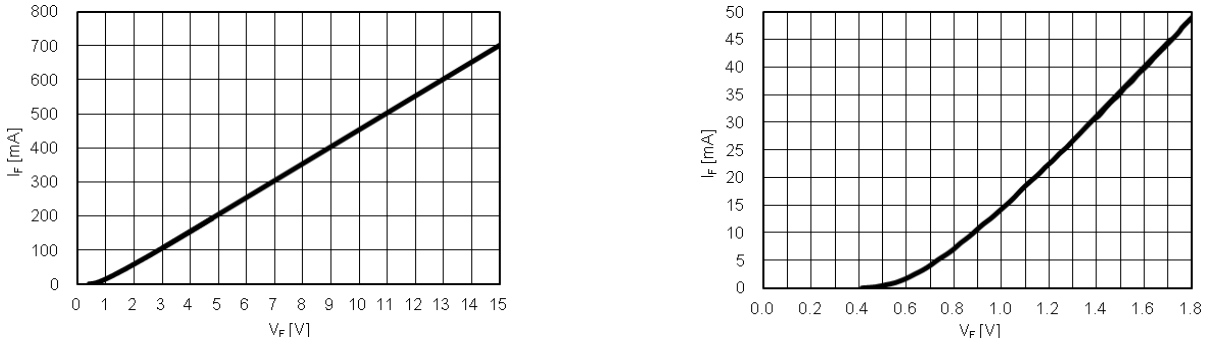
Table 4-3-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	•Aluminum type: Low temp.: -10% High temp: +10% •Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on -70%~-15%

DC bias characteristic of electrolytic capacitor is no problem, however, it is necessary to note its ripple capability by repetitive charge and discharge, its ambient temperature which affects the capacitor's life time greatly, and so on. These above characteristics are just example data which are quoted from the WEB site, so it is recommended to inquiry to the capacitor manufacturers about detailed characteristics.

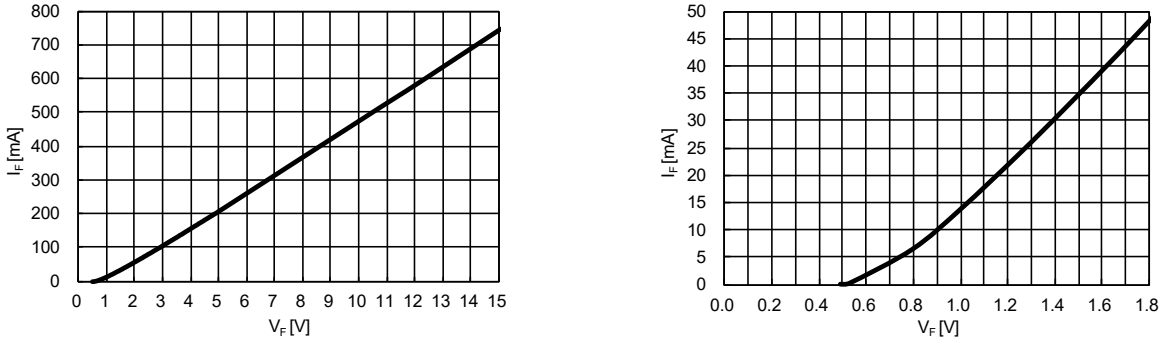
(2) Bootstrap diode

DIPIPM+ integrates bootstrap diodes for P-side driving supply. This BSD incorporates current limiting resistor (typ. 20Ω). The V_F-I_F characteristics (including voltage drop by built-in current limiting resistor) are shown in Fig.4-3-1, 2 and Table 4-3-2.



(a) BSD V_F-I_F characteristics (b) BSD V_F-I_F characteristics (Enlarged view)

Fig.4-3-1 Typical V_F-I_F curve for bootstrap Diode (For PSS**M(N)C1FT)



(a) BSD V_F-I_F characteristics (b) BSD V_F-I_F characteristics (Enlarged view)

Fig.4-3-2 Typical V_F-I_F curve for bootstrap Diode (For PSS**M(N)C1F6)

Table 4-3-2 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	I_F=10mA including voltage drop by limiting resistor	—	0.9	1.3	V
Built-in limiting resistance	R	Included in bootstrap Di	16	20	24	Ω

4.4 Initial charging in bootstrap circuit

In case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may drop down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIPIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and etc.

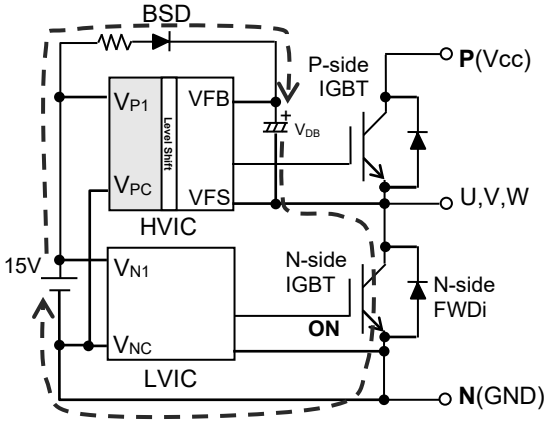


Fig.4-4-1 Initial charging root

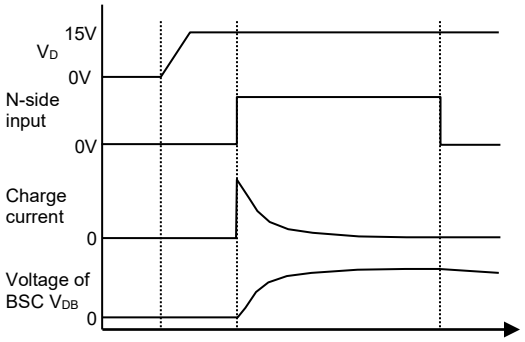


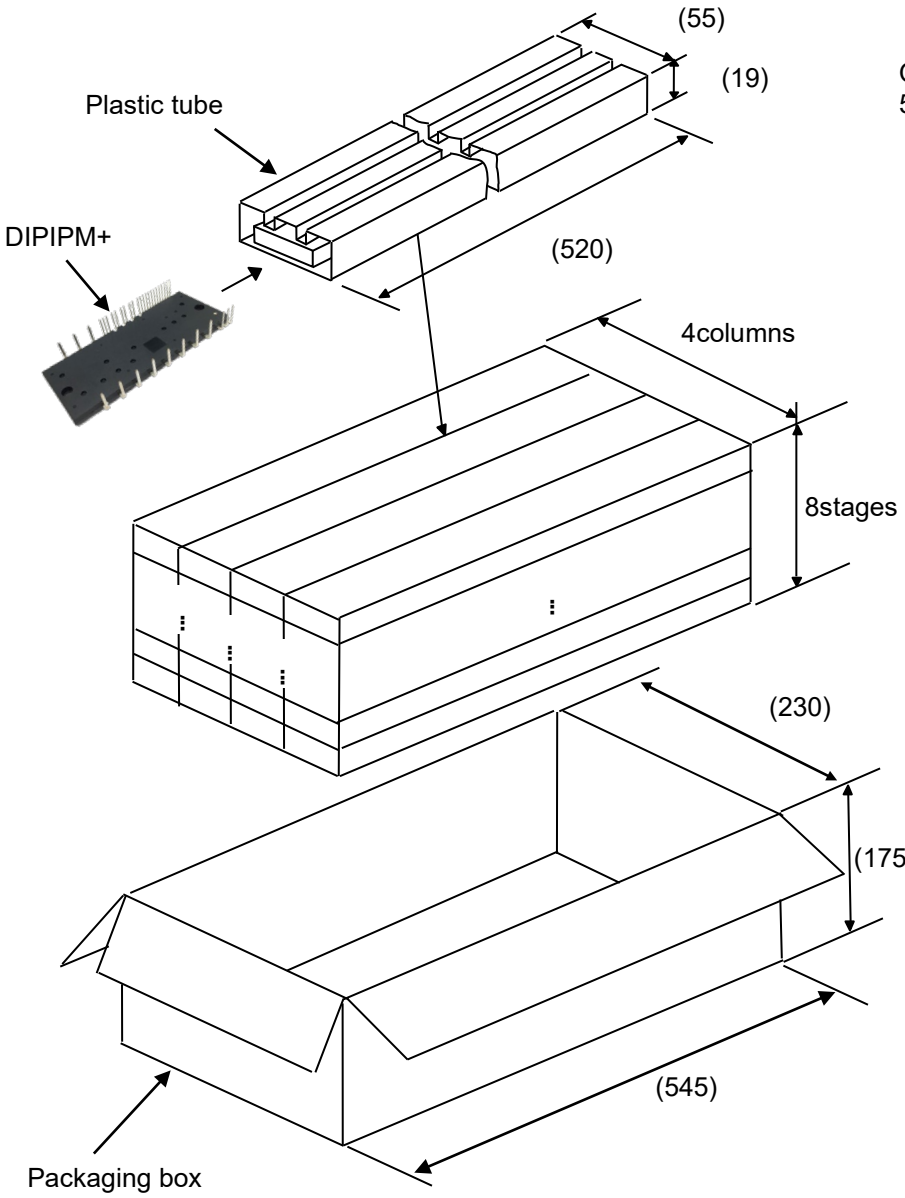
Fig .4-4-2 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds 13V, recommended minimum supply voltage. (It is recommended to charge higher than 13V with consideration for voltage drop from the end of charging to start time of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (1.5μs or more for DIPIPM+. Please refer the datasheet for each product in detail.)

CHAPTER 5 : PACKAGE HANDLING

5.1 Packaging Specification



Quantity:
5 pieces / 1 tube

Total amount in one box (max):
Tube Quantity: 4 × 8=32pcs
IPM Quantity(max.):
5 × 32 ＝160pices

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the spcae of top stage.

Mass:
About 40g / DIPIPM+
About 300g / tube
About 11kg / box

Spacers are put on the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

5.2 Handling Precautions

⚠ Cautions	
Transportation	・Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ・Throwing or dropping the packaging boxes might cause the devices to be damaged. ・Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	・We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	・When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	・Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	・The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	・ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1)Precautions against the device destruction caused by the ESD The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. ・Containers that charge static electricity easily should not be used for transit and for storage. ・Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. ・Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands. ・During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. ・When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. ・If using a soldering iron, earth its tip. (2)Notice when the control terminals are open ・When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. ・Short the terminals before taking a module off.

Important Notice

The information contained in this datasheet shall in no event be regarded as a guarantee of conditions or characteristics. This product has to be used within its specified maximum ratings, and is subject to customer’s compliance with any applicable legal requirement, norms and standards.

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In usage of power semiconductor, there is always the possibility that trouble may occur with them by the reliability lifetime such as Power Cycle, Thermal Cycle or others, or when used under special circumstances (e.g. condensation, high humidity, dusty, salty, highlands, environment with lots of organic matter / corrosive gas / explosive gas, or situations which terminals of semiconductor products receive strong mechanical stress). Therefore, please pay sufficient attention to such circumstances. Further, depending on the technical requirements, our semiconductor products may contain environmental regulation substances, etc. If there is necessity of detailed confirmation, please contact our nearest sales branch or distributor.

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