MITSUBISHI ELECTRIC

DIPIPM Ver.3

APPLICATION NOTE

Aug. 2009

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Table of Contents

CHAPTER 1 DIPIPM PRODUCT OUTLINES

1.1 Product Line-up

Table 1. DIPIPM Ver.3 Product Line-up

Part No.	IGBT Rating (I_C /V_{CES})	Motor Rating	Isolation	Package
PS21562-P	5A / 600V	0.2 kW / 220 VAC	V_{iso} = 2500Vrms (Sinusoidal, 1min)	Mini DIPIPM
PS21563-P	10A / 600V	0.4 kW / 220VAC		
PS21564-P	15A / 600V	0.75 kW / 220 VAC		
PS21865-P/-AP	20A / 600V	1.5 kW / 220 VAC		Large DIPIPM
PS21867-P/-AP	30A / 600V	2.2 kW / 220 VAC		
PS21869-P/-AP	50A / 600V	3.7 kW / 220 VAC		

Note:(1) These motor ratings show general motor capacity of general-purpose inverter for industrial application.
The available motor rating according to application conditions may be different from the above one.
(2) Part No. suffixed by (-A) of DIPIPM(PS21865/867/869) indicates the long terminal with 16mm-length.
(3) Part No. suffixed by (-P) indicates Pb free plating terminal

[Applications]
Motor drive for household electric appliances, such as air conditioners, washing machines, refrigerators, and low power industrial applications as well.

1.2 Functions and Features

1.2.1 Function outlines
Figure 1-1 and 1-2 show the photograph and the internal structure diagram of Large DIPIPM and Mini DIPIPM respectively. The DIPIPM is the ultra-compact intelligent power module, which integrates power parts, driver and protection circuit for AC100-220V class low power motor inverter control into a dual-in-line transfer molded package.

DIPIPM over 20A class has built-in heat sink to reduce the thermal resistance, as shown in Fig. 1(b).

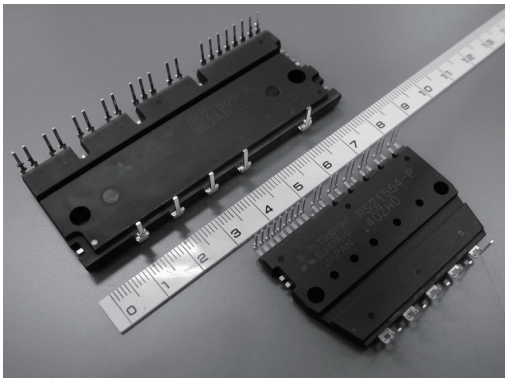


Figure1-1 Photograph

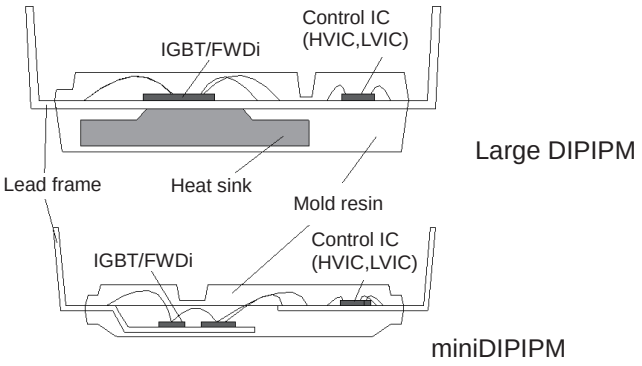
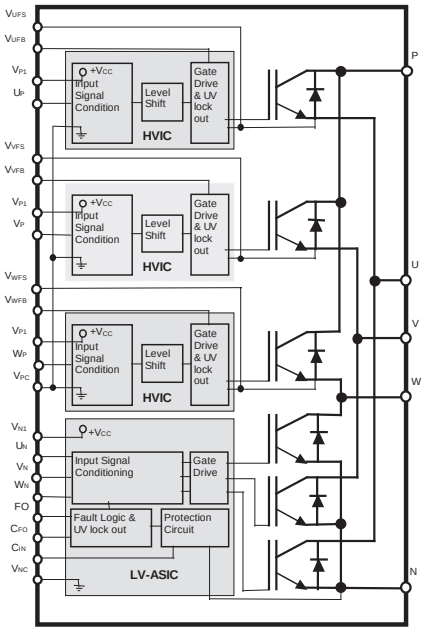
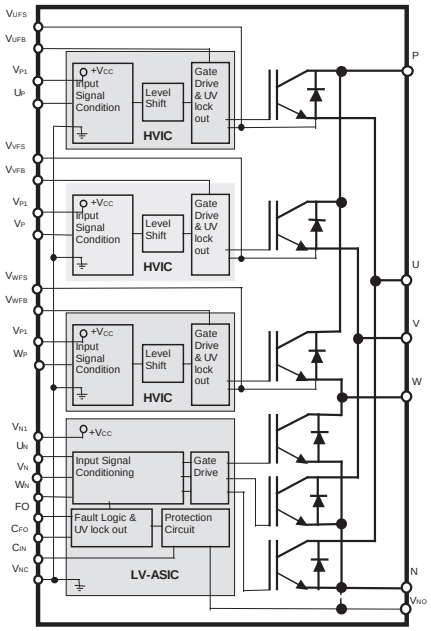


Figure1-2 Internal structure

CHAPTER 1 DIPIPM PRODUCT OUTLINES



Large DIPIPM



MiniDIPIPM

Figure1-3 Internal function block diagram of DIPIPM

1.2.2 Product Features

(1) Integrated IGBT inverter circuit for three-phase AC output, Loss reduction by employing the 5th generation planar IGBT and CSTBT^{TM}(Carrier Stored Trench-gate Bipolar Transistor).
->the 5th generation planar IGBT for 5A-30A DIPIPM.
->the CSTBT for 50A DIPIPM

(2) Single-power-supply drive topology by introducing bootstrap circuit scheme.

(3) Built-in control and protection functions
P-side: Control circuit Under-Voltage (UV) protection (without fault signal output).
N-side: UV and Short-Circuit (SC) protection by means of external shunt resistor (with fault signal output).

(4) By virtue of integrating high voltage IC (HVIC) inside, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(5) By virtue of applying high-active drive logic, the sequence restraint between control supply and control input in turn on and turn off operation has been able to eliminated, which makes the devices to be fail-safe, and furthermore, a direct connection without signal level shift to a 3V MCU or DSP becomes possible.

(6) Pb-free solder (Sn-Cu origin) is used to plate outer terminals.

CHAPTER 2 ELECTRICAL CHARACTERISTICS

2.1 Maximum Ratings

Table 2 shows the Maximum Ratings of PS21865-P (*).

Table 2. Maximum Ratings of PS21865-P

Maximum Ratings (Tj=25°C, unless otherwise noted)

Inverter Part

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	Applied between P-N	450	V
Supply voltage (surge)	$V_{CC(surge)}$	Applied between P-N	500	V
Collector-emitter voltage	V_{CES}		600	V
Each IGBT collector current	$\pm I_C$	Tf=25°C	20	A
Each IGBT collector current (peak)	$\pm I_{CP}$	Tf=25°C, less than 1ms	40	A
Collector dissipation	P_C	Tf=25°C, per 1 chip	52.6	W
Junction temperature	Tj	(Note1)	-20~+125	°C

(Note1) The maximum junction temperature rating of the power chips integrated within the DIPIPM is 150ºC(@Tf≤100ºC) however, to insure safe operation of the DIPIPM, the average junction temperature should be limited to Tj(ave) ≤125ºC (@Tf≤100ºC).

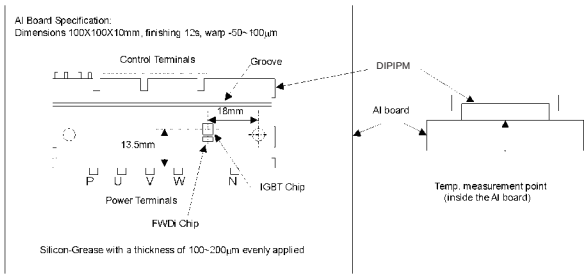
Control (Protection) Part

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V_D	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}	20	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS} , V_{WFB}-V_{WFS}	20	V
Input voltage	V_{IN}	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
Fault output supply voltage	V_{FO}	Applied between Fo-V_{NC}	-0.5~V_D+0.5	V
Fault output current	I_{FO}	Sink current at Fo terminal	1	mA
Current sensing input voltage	V_{SC}	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

Total System

Item	Symbol	Condition	Rating	Unit
Self protection supply voltage limit (short circuit protection capability)	$V_{CC(PROT)}$	V_D=13.5~16.5V, Inverter part Tj=125°C, non-repetitive less than 2μs	400	V
Module case operation temperature	Tf	(Note2)	-20~+100	°C
Storage temperature	Tstg		-40~+125	°C
Isolation voltage	Viso	60Hz, Sinusoidal, AC 1 minute, connecting pins to heat-sink plate	2500	Vrms

(Note2) Tf measurement point



Vcc : the maximum P-N voltage in state of no switching. A brake is necessary if P-N voltage exceeds this specification.
Vcc(surge): the maximum P-N surge voltage in state of no switching. A snubber circuit is necessary if P-N voltage exceeds Vcc(surge).
V_{CES}: the sustained collector-emitter voltage of built-in IGBT.

$\pm I_C$: the allowable DC current continuously flowing at collect electrode (Tf=25℃)

Tj:power cycles will be no less than 10 million on the condition of Tf=100℃ and Tj≤125℃. Although chip will not be damaged right now at Tj=150℃,its power cycles come to be decreased

$V_{CC(PROT)}$: the Maximum supply voltage for IGBT turning off safely in case of SC or OC. The power chip might be damaged if supply voltage exceeds this specification.

Viso: united to 2500Vrms in Ver.3

(*): Unless otherwise noted, the data used in this chapter are all of PS21865-P (20A/600V) as a demonstration example. For other products of DIPIPM ver.3 series, please refer to their individual datasheets.

2.2 Electric Characteristics

2.2.1 Thermal Resistance

Table 3 show the thermal resistance of PS21865-P and PS21563-P.

Table 3-1 Thermal resistance of PS21865-P

Thermal Resistance						
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to fin thermal resistance (Note3)	$R_{th(j-f)Q}$	Inverter IGBT part (per 1/6 module)	-	-	1.90	°C/W
	$R_{th(j-f)F}$	Inverter FWD part (per 1/6 module)	-	-	3.00	

(Note3) Grease with good thermal conductivity should be applied evenly with a thickness of about +100μm~+200μm on the contact surface of DIPIPM and heat-sink.

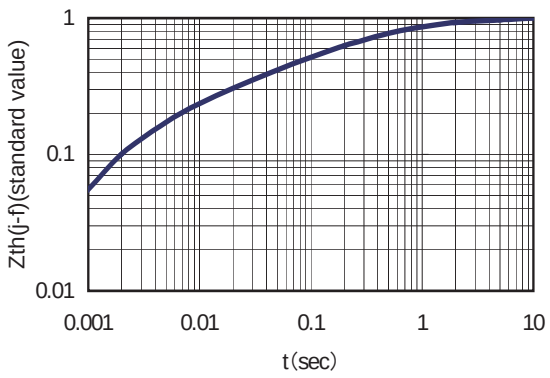
The steady thermal resistance corresponding to the unite "1" in figure 2-1.
Example:
The transient thermal resistance in 0.1sec of PS21865 is 1.90 × 0.5=0.95 °C/W.

Table 3-2 Thermal resistance of PS21563-P

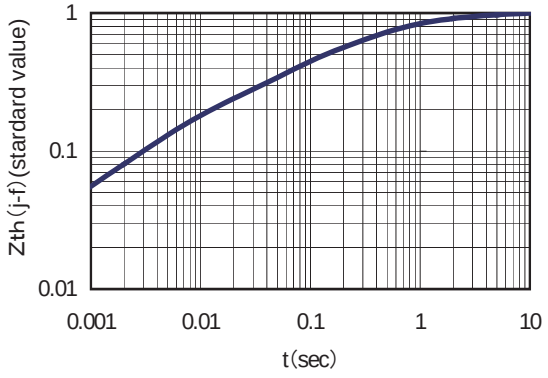
Thermal Resistance						
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to fin thermal resistance (Note3)	$R_{th(j-f)Q}$	Inverter IGBT part (per 1/6 module)	-	-	5.0	°C/W
	$R_{th(j-f)F}$	Inverter FWD part (per 1/6 module)	-	-	6.5	

(Note3) Grease with good thermal conductivity should be applied evenly with a thickness to about +100μm~+200μm on the contact surface of DIPIPM and heat-sink.

Table 3 shows the steady thermal resistance between Junction and Fin. The thermal resistance goes into saturation in about 10 seconds. Figure 2-1 shows the transient resistance Zth(j-f) curve within 10 seconds.



(a) Large DIPIPM Zth(j-f) characteristic



(b) Mini DIPIPM Zth(j-f) characteristic

Figure 2-1. DIPIPM Zth(j-f) characteristic curve(IGBT/FWDi)

2.2.2 Static Characteristics and Switching Characteristics

(1) Static Characteristics

Table 4 show the typical static characteristics and switching characteristics of PS21865-P and PS21563-P

Table 4-1 Static characteristics and switching characteristic of PS21865-P

Electrical Characteristics (Tj=25°C, unless otherwise noted) Inverter Part							
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_D=V_{DB}=15V$, $V_{IN}=5V$	I_C=20A, Tj=25°C	-	1.6	2.1	V
			I_C=20A, Tj=125°C	-	1.7	2.2	
FWD forward voltage	V_{EC}	Tj=25°C, $-I_C$=20A, V_{IN}=0V		-	1.5	2.0	V
Switching times	t_{on}	V_{CC}=300V, $V_D=V_{DB}$=15V		0.7	1.3	1.9	μs
	t_{rr}	I_C=20A		-	0.3	-	
	$t_{c(on)}$	Tj=125°C		-	0.4	0.6	
	t_{off}	Inductive load (upper-lower arm)		-	1.6	2.2	
	$t_{c(off)}$	V_{IN}=0<->5V		-	0.5	0.8	
Collector-emitter cut-off current	I_{CES}	$V_{CE}=V_{CES}$	Tj=25°C	-	-	1	mA
			Tj=125°C	-	-	10	

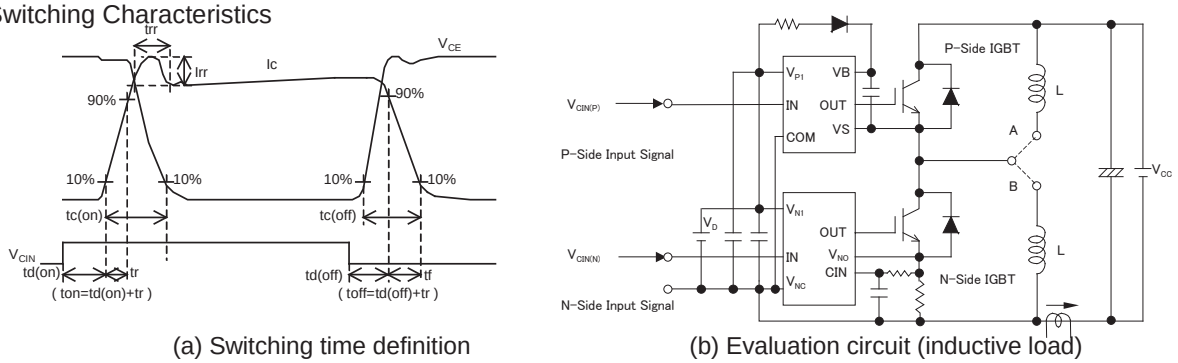
CHAPTER 2 ELECTRICAL CHARACTERISTICS

Table 4-2 Static characteristics and switching characteristic of PS21563-P

Electrical Characteristics (Tj=25°C, unless otherwise noted)
Inverter Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_D=V_{DB}$=15V, V_{IN}=5V	I_C=10A, Tj=25°C	-	1.60	2.10	V
			I_C=10A, Tj=125°C	-	1.70	2.20	
FWD forward voltage	V_{EC}	Tj=25°C, -I_C=10A, V_{IN}=0V		-	1.50	2.00	V
Switching times	t_{on}	V_{CC}=300V, $V_D=V_{DB}$=15V, I_C=10A, Tj=125°C, Inductive load (upper-lower arm), V_{IN}=0<->5V		0.60	1.20	1.80	μs
	t_{rr}			-	0.30	-	
	$t_{c(on)}$			-	0.40	0.60	
	t_{off}			-	1.40	2.10	
	$t_{c(off)}$			-	0.50	0.80	
Collector-emitter cut-off current	I_{CES}	$V_{CE}=V_{CES}$	Tj=25°C	-	-	1	mA
			Tj=125°C	-	-	10	

(2) Switching Characteristics



(a) Switching time definition (b) Evaluation circuit (inductive load)

Figure 2-2. Half-bridge evaluation circuit diagram

Conditions : V_{CC}=300V, $V_D=V_{DB}$=15V, Tj=125°C, Ic=20A, Inductive load half-bridge circuit

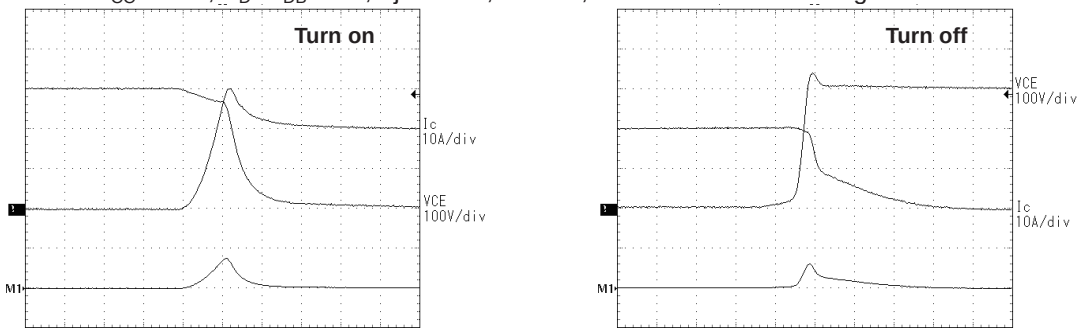


Figure 2-3. Typical switching waveform (PS21865-P N-side)

Conditions : V_{CC}=300V, $V_D=V_{DB}$=15V, Tj=125°C, Ic=10A, Inductive load half-bridge circuit

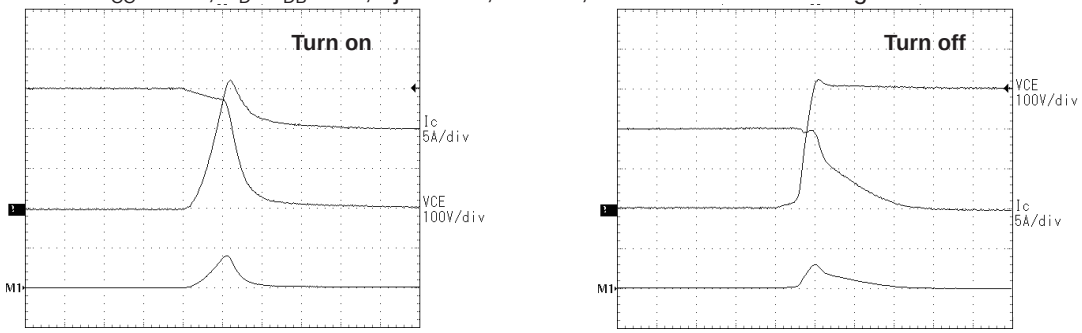


Figure 2-4. Typical switching waveform (PS21563-P N-side)

2.2.3 Control (Protection) Characteristics

Table 5-1 Control (Protection) characteristics of PS21865-P

Control (Protection) Part :

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I_D	$V_D=V_{DB}$=15V	Total of V_{P1}-V_{PC},V_{N1}-V_{NC}	-	-	7.00	mA
		V_{IN}=5V	V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	-	-	0.55	mA
		$V_D=V_{DB}$=15V	Total of V_{P1}-V_{PC},V_{N1}-V_{NC}	-	-	7.00	mA
		V_{IN}=0V	V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	-	-	0.55	mA
Fo output voltage	V_{FOH}	V_{SC}=0V, Fo circuit pull-up to 5V with 10kΩ		4.9	-	-	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA		-	-	0.95	V
Input current	I_{IN}	V_{IN}=5V		1.0	1.5	2.0	mA
Short circuit trip level	$V_{SC(ref)}$	Tf=-20~100°C, V_D=15V (Note4)		0.45	-	0.52	V
Supply circuit under-voltage protection	UV_{DBt}	Tj≤125°C	Trip level	10.0	-	12.0	V
	UV_{DBr}		Reset level	10.5	-	12.5	V
	UV_{Dt}		Trip level	10.3	-	12.5	V
	UV_{Dr}		Reset level	10.8	-	13.0	V
Fault output pulse width	t_{FO}	C_{FO}=22nF (Note5)		1.0	1.8	-	ms
ON threshold voltage	Vth(on)	Applied between U_P,V_P,W_P-V_{PC},		2.1	2.3	2.6	V
OFF threshold voltage	Vth(off)	U_N,V_N,W_N-V_{NC}		0.8	1.4	2.1	

(Note4) Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 40A

(Note5) Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : C_{FO}= 12.2 × 10^{-6} × t_{FO} [F]

In the case of previous PS21865(Pb solder plating type), these value ware 5.0mA & 0.4mA respectively

In the case of previous PS21865, This range was from 0.43V to 0.53V

In the case of previous PS21865, this value was 34A(rated current X1.7)

Same parts are changed about PS21867-P/-AP and PS21869-P/-AP too. (Please refer each datasheets.)

Table 5-2 Control (Protection) characteristics of PS21563-P

Control (Protection) Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I_D	$V_D=V_{DB}$=15V	Total of V_{P1}-V_{NC},V_{N1}-V_{NC}	-	-	5.00	mA
		V_{IN}=5V	V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	-	-	0.40	mA
		$V_D=V_{DB}$=15V	Total of V_{P1}-V_{NC},V_{N1}-V_{NC}	-	-	7.00	mA
		V_{IN}=0V	V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	-	-	0.55	mA
Fo output voltage	V_{FOH}	V_{SC}=0V, Fo circuit pull-up to with 10kΩ		4.9	-	-	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA		-	-	0.95	V
Input current	I_{IN}	V_{IN}=5V		1.0	1.5	2.0	mA
short circuit trip level	$V_{SC(ref)}$	Tf=-20~100°C, V_D=15V (Note4)		0.45	-	0.52	V
Supply circuit under-voltage protection	UV_{DBt}	Tj≤125°C	Trip level	10.0	-	12.0	V
	UV_{DBr}		Reset level	10.5	-	12.5	V
	UV_{Dt}		Trip level	10.3	-	12.5	V
	UV_{Dr}		Reset level	10.8	-	13.0	V
Fault output pulse width	t_{FO}	C_{FO}=22nF (Note5)		1.0	1.8	-	ms
ON threshold voltage	Vth(on)	Applied between U_P,V_P,W_P-V_{NC},		2.1	2.3	2.6	V
OFF threshold voltage	Vth(off)	U_N,V_N,W_N-V_{NC}		0.8	1.4	2.1	

(Note4) Short circuit protection is functioning only at the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 20A

(Note5) Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : C_{FO}= 12.2 × 10^{-6} × t_{FO} [F]

In the case of previous PS21865, This range was from 0.43V to 0.53V

In the case of previous PS21563, this value was 17A(rated current X1.7)

Same parts are changed about PS21562-P, PS21564-P too. (Please refer each datasheets.)

2.3 Recommended Operation Conditions

Table 6-1 Recommended operating conditions of PS21865-P.

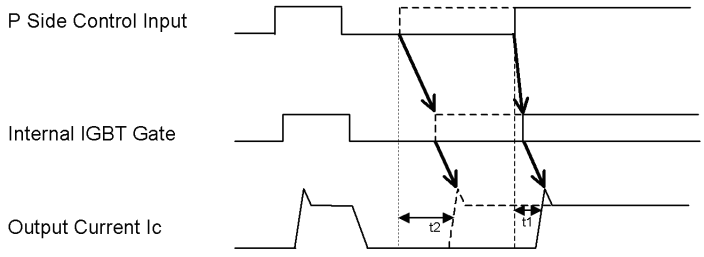
Recommended Operation Conditions

Item	Symbol	Condition		Recommended Min.	Recommended Typ.	Recommended Max.	Unit
Supply voltage	V_{CC}	Applied between P-N		0	300	400	V
Control supply voltage	V_D	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
Control supply variation	ΔV_D, ΔV_{DB}			-1	-	1	V/μs
Arm-shoot-through blocking time	t_{dead}	For each input signal, Tf≤100°C		2	-	-	μs
PWM input frequency	f_{PWM}	Tf≤100°C, Tj≤125°C		-	-	20	kHz
Allowable r.m.s. current	I_O	V_{CC}=300V, V_D=V_{DB}=15V, P.F=0.8, sinusoidal PWM, Tj≤125°C, Tf≤100°C (Note7)	f_{PWM}=5kHz	-	-	14	Arms
			f_{PWM}=15kHz	-	-	9.5	
Minimum input pulse width	PWIN(on)	(Note8)		0.3	-	-	μs
	PWIN(off)	200≤V_{CC}≤350V, 13.5≤V_D≤16.5V, 13.0≤V_{DB}≤18.5V, -20°C≤Tf≤100°C, N-line wiring inductance less than 10nH (Note9)	Below rated current	1.4	-	-	
			Between rated current and 1.7 times of rated current	2.5	-	-	
			Between 1.7 times of rated current and 2.0 times of rated current	3.0	-	-	
V_{NC} variation	V_{NC}	between V_{NC}-N (including surge)		-5.0	-	5.0	V

This condition is added to previous PS21865 (Pb solder plating type)

(Note7) The Allowable r.m.s. current value depends on the actual application conditons.
(Note8) Input signal with ON pulse width less than PWIN(on) might make no response.
(Note9) IPM might make delayed response (less than 2 sec) or no response for the input signal with off pulse width less than PWIN(off).

Current output when input signal is less than allowable minimum input pulse with $P_{WIN(off)}$ (P-side only)



Real line…off pulse width＞PWIN(off); turn on time t1
Broken line…off pulse width＜PWIN(off); turn on time t2

Same part is changed about PS21867-P/-AP and PS21869-P/-AP too. (Please refer each datasheets.)

CHAPTER 2 ELECTRICAL CHARACTERISTICS

Table 6-2 Recommended operating conditions of PS21563-P.

Recommended Operation Conditions

Item	Symbol	Condition		Recommended Min.	Recommended Typ.	Recommended Max.	Unit
Supply voltage	V_{CC}	Applied between P-N		0	300	400	V
Control supply voltage	V_D	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
Control supply variation	ΔV_D, ΔV_{DB}			-1	-	1	V/μs
Arm-shoot-through blocking time	t_{dead}	For each input signal, Tf≤100°C		1.5	-	-	μs
PWM input frequency	f_{PWM}	Tf≤100°C, Tj≤125°C		-	-	20	kHz
Allowable r.m.s. current	I_O	V_{CC}=300V, V_D=V_{DB}=15V, P.F=0.8, sinusoidal PWM, Tj≤125°C, Tf≤100°C (Note7)	f_{PWM}=5kHz	-	-	6.5	Arms
			f_{PWM}=15kHz	-	-	4.0	
Minimum input pulse width	PWIN(on)	(Note8)		0.3	-	-	μs
	PWIN(off)	200≤V_{CC}≤350V, 13.5≤V_D≤16.5V, 13.0≤V_{DB}≤18.5V, -20°C≤Tf≤100°C, N-line wiring inductance less than 10nH (Note9)	Below rated current	0.5	-	-	
			Between rated current and 1.7 times of rated current	0.5	-	-	
			Between 1.7 times of rated current and 2.0 times of rated current	0.7	-	-	
V_{NC} variation	V_{NC}	between V_{NC}-N (including surge)		-5.0	-	5.0	V

(Note7) The allowable r.m.s. current value depends on the actual application conditons.
(Note8) Input signal with ON pulse width less than PWIN(on) might make no response.
(Note9) IPM might not work properly or make response for the Input signal with OFF pulse width less than PWIN(off).

This condition is added to previous PS21563 (Pb solder plating type)

Same part is changed about PS21562-P, PS21564-P too. (Please refer each datasheets.)

Note: Although DIPIPM is able to operate at high frequency upto 20kHz, the allowable r.m.s current will vary according to the temperature condition,control method (PWM scheme). PWM control signal should be determined on the basis of power loss and thermal evaluation. The above values are only for reference.

CHAPTER 3 PACKAGE OUTLINE

3.1 Package Outline

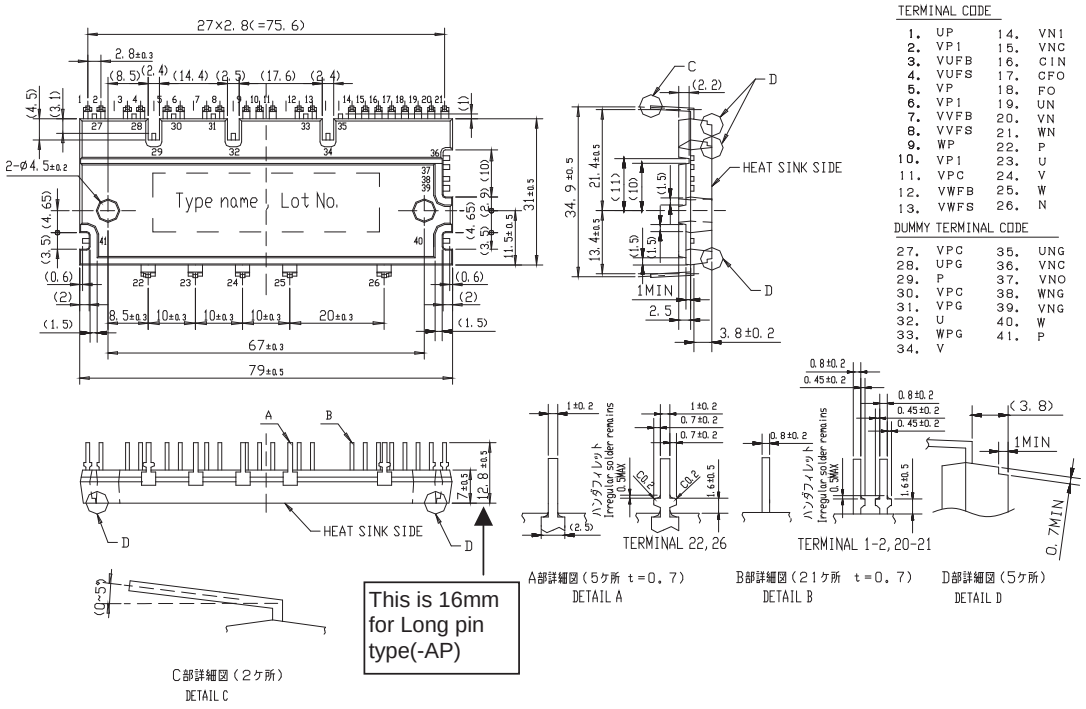


Figure 3-1 Package outline drawing of Large DIPIPM Ver.3(PS2186X-P)

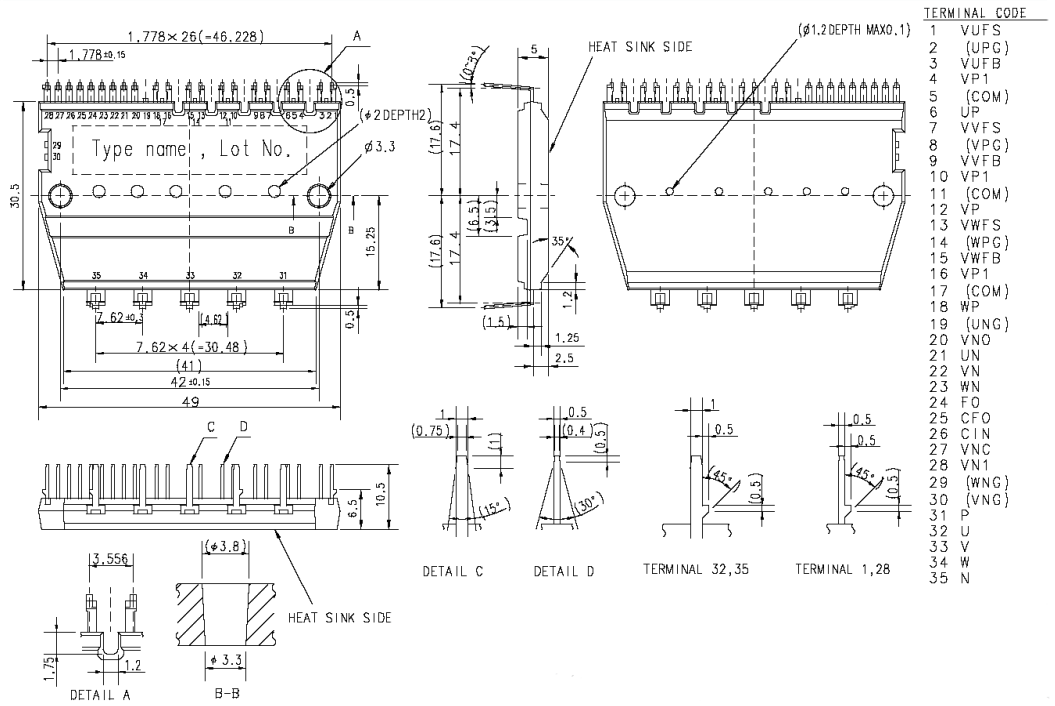


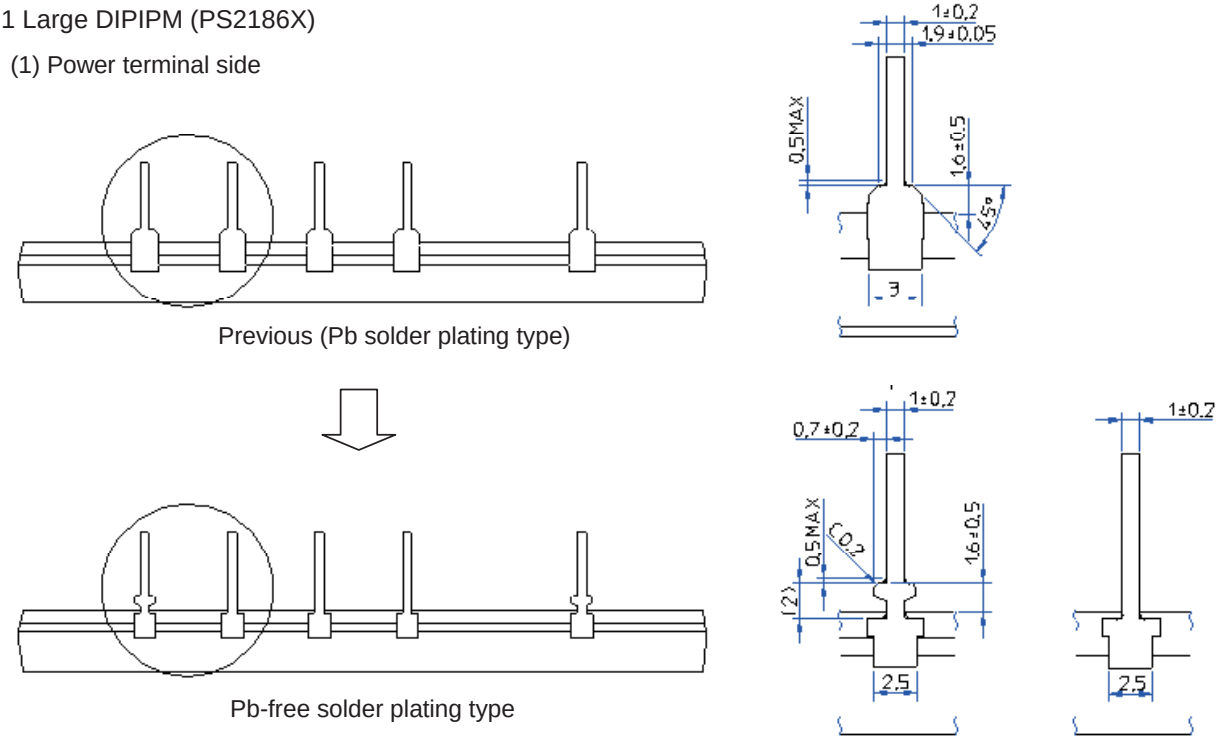
Figure 3-2 Package Outline Drawing of mini DIPIPM(PS2156X-P)

3.2 Outline differential between Pb-free solder plating type(-P/-AP) and Pb solder plating type

Terminal shapes are changed at Pb-free type (-P/-AP).

3.2.1 Large DIPIPM (PS2186X)

(1) Power terminal side



(2) Control terminal side

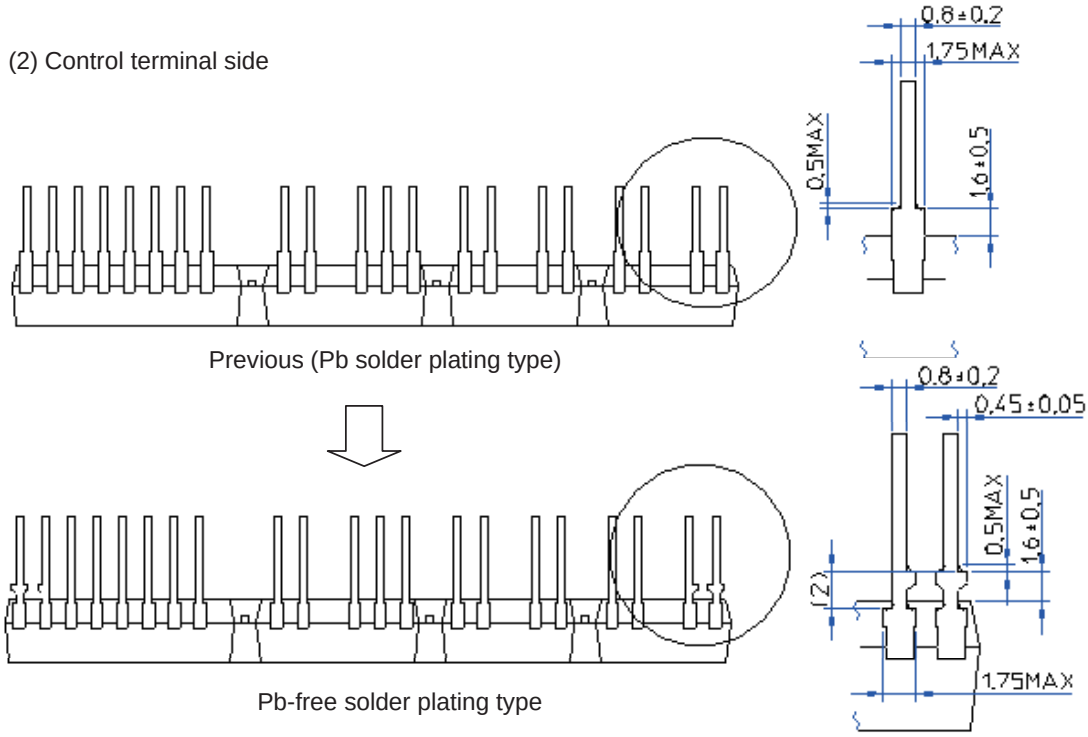
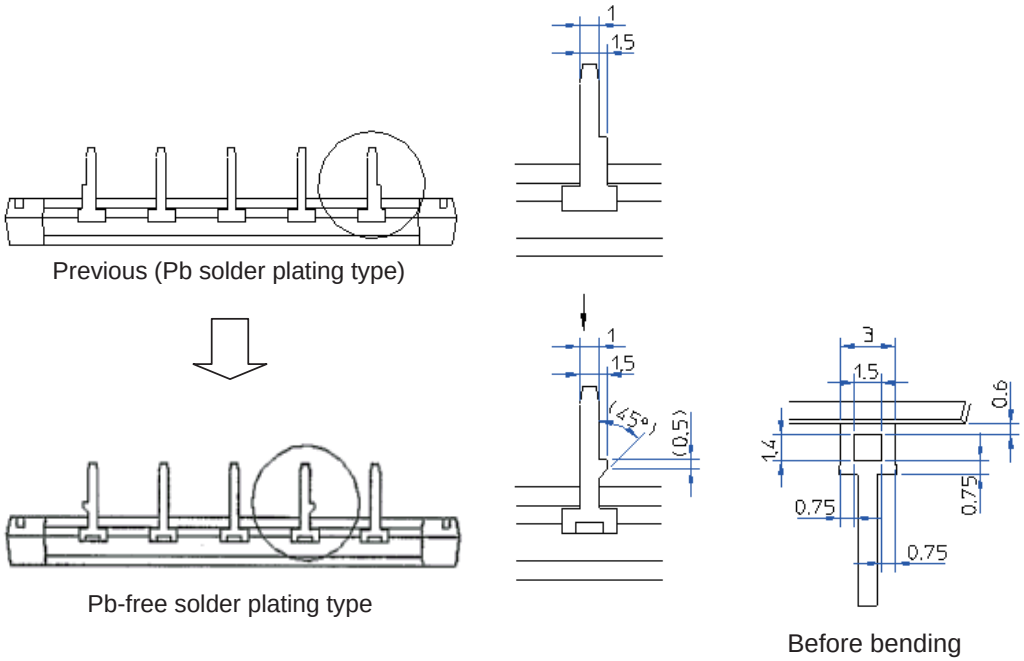


Figure 3-3 Package outline differential of Large DIPIPM

3.2.2 Mini DIPIPM (PS2156X)

(1) Power terminal side



(2) Control terminal side

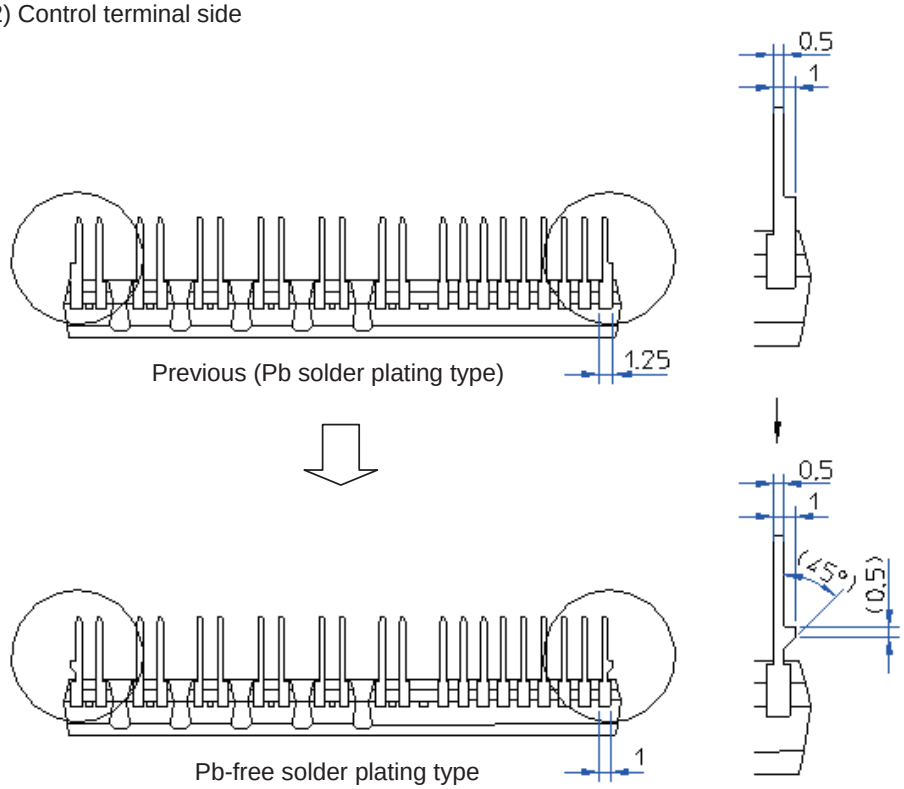


Figure 3-4 Package outline differential of Mini DIPIPM

3.3 Isolation

Table 7. Isolation distance of Large DIPIPM

Clearance(mm)		Creepage(mm)	
Between Power terminals	6.6	Between Power terminals	6.6
Between Control terminals	3.55	Between Control terminals	3.55
Between Terminals and heat sink	3.6	Between Terminals and heat sink	4.0

Table 8. Isolation distance of Mini DIPIPM

Clearance(mm)		Creepage(mm)	
Between Power terminals	4.0	Between Power terminals	4.0
Between Control terminals	1.8	Between Control terminals	4.0
Between Terminals and heat sink	2.3	Between Terminals and heat sink	2.3(4.0*)

* Except creepage distance between dummy terminals and heat sink

About creepage between dummy terminals and heat sink of Mini DIPIPM

The creepage between dummy terminal and heat sink (gate potential of VN IBGT and WN IGBT) on the side of DIPIPM is min.2.3mm. Also, the creepage (X) between screw or washer and terminal may be under 4mm, if their size would be so big.

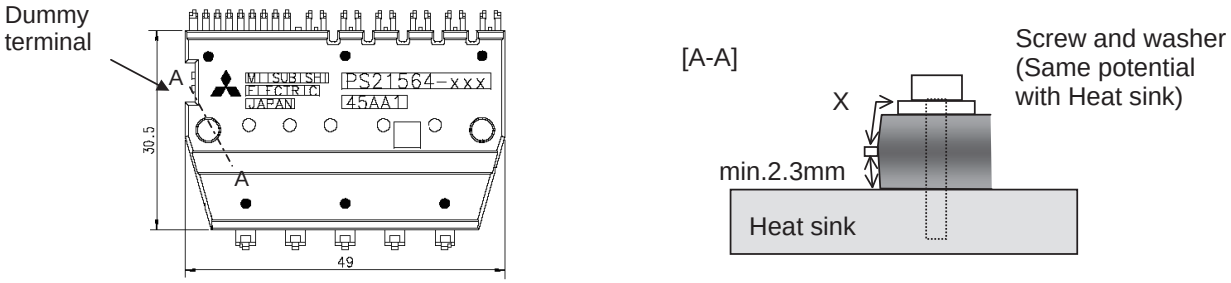
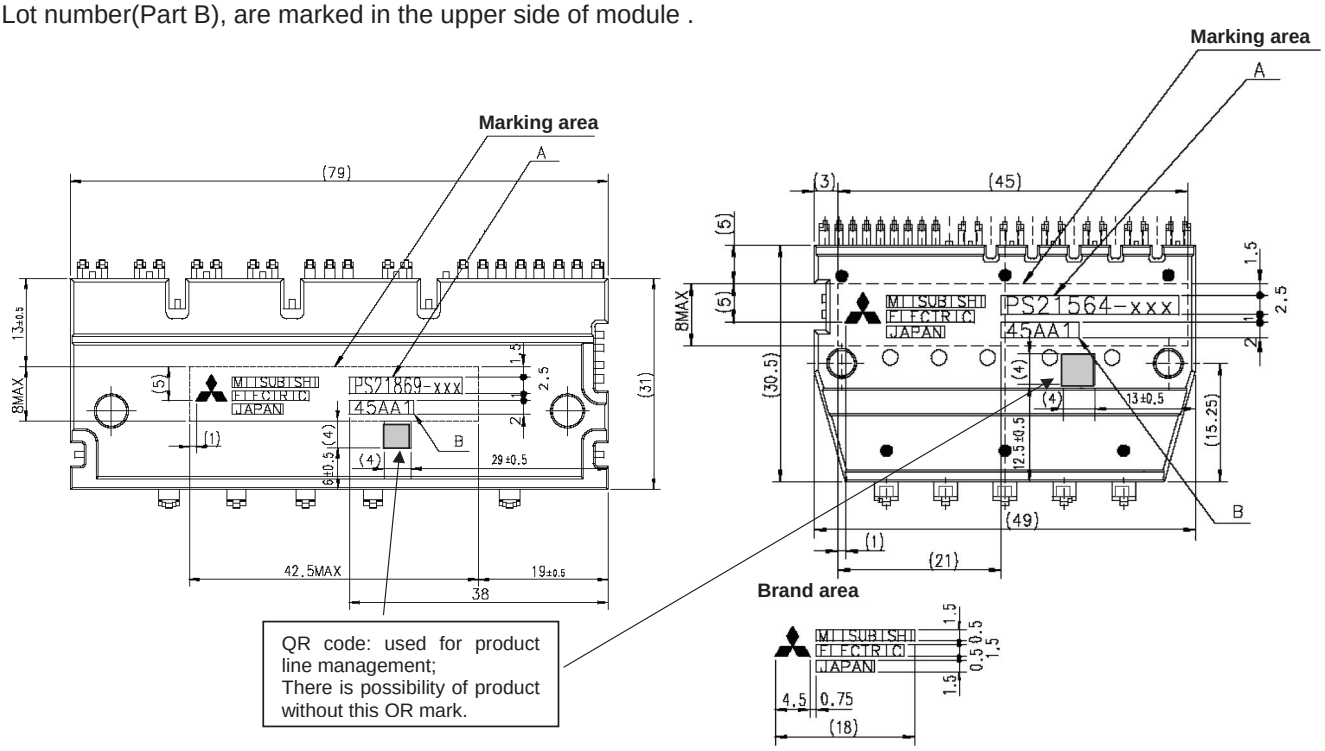


Figure 3-5 Creepage between dummy terminal and heat sink

For Large DIPIPM the creepage distance between dummy terminal and heat sink ensure min.4mm.

3.4 Laser Marking

The laser marking range of DIPIPM is described in Figure 3-6. Mitsubishi Corporation mark, Type name (Part A), and Lot number(Part B), are marked in the upper side of module .



QR code is registered trademark of DENSO WAVE INCORPORATED in JAPAN and other countries.

Figure 3-6 Laser Marking

3.5 Input / Output Terminals Description

3.5.1 Terminal Arrangement

Table 9. (a) DIPIPM terminal Arrangement

DIPIPM		
Terminal No.	Terminal Name	Description
1	U_P	U-phase P-side control input terminal
2	V_{P1}	U-phase P-side control supply positive terminal
3	V_{UFB}	U-phase P-side drive supply positive terminal
4	V_{UFS}	U-phase P-side drive supply GND terminal
5	V_P	V-phase P-side control input terminal
6	V_{P1}	V-phase P-side control supply positive terminal
7	V_{VFB}	V-phase P-side drive supply positive terminal
8	V_{VFS}	V-phase P-side drive supply GND terminal
9	W_P	W-phase P-side control input terminal
10	V_{P1}	W-phase P-side control supply positive terminal
11	V_{PC}	P-side control supply GND terminal
12	V_{WFB}	W-phase P-side drive supply positive terminal
13	V_{WFS}	W-phase P-side drive supply GND terminal
14	V_{N1}	N-side control supply positive terminal
15	V_{NC}	N-side control supply GND terminal
16	CIN	SC current trip voltage detecting terminal
17	CFO	Fault pulse output width setting terminal
18	F_O	Fault signal output terminal
19	U_N	U-phase N-side control input terminal
20	V_N	V-phase N-side control input terminal
21	W_N	W-phase N-side control input terminal
22	P	Inverter DC-link positive terminal
23	U	U-phase output terminal
24	V	V-phase output terminal
25	W	W-phase output terminal
26	N	Inverter DC-link negative terminal
27	VPC	Dummy-pin (Note 1)
28	UPG	Dummy-pin
29	P	Dummy-pin
30	VPC	Dummy-pin
31	VPG	Dummy-pin
32	U	Dummy-pin
33	WPG	Dummy-pin
34	V	Dummy-pin
35	UNG	Dummy-pin
36	VNC	Dummy-pin
37	VNO	Dummy-pin
38	WNG	Dummy-pin
39	VNG	Dummy-pin
40	W	Dummy-pin
41	P	Dummy-pin

Table 9. (b) Mini DIPIPM terminal Arrangement

Mini DIPIPM		
Terminal No.	Terminal Name	Description
1	V_{UFS}	U-phase P-side drive supply GND terminal
2	UPG	Dummy-pin
3	V_{UFB}	U-phase P-side drive supply positive terminal
4	V_{P1}	U-phase P-side control supply positive terminal
5	COM	Dummy-pin
6	U_P	U-phase P-side control input terminal
7	V_{VFS}	V-phase P-side drive supply GND terminal
8	VPG	Dummy-pin
9	V_{VFB}	V-phase P-side drive supply positive terminal
10	V_{P1}	V-phase P-side control supply positive terminal
11	COM	Dummy-pin
12	V_P	V-phase P-side control input terminal
13	V_{WFS}	W-phase P-side drive supply GND terminal
14	WPG	Dummy-pin
15	V_{WFB}	W-phase P-side drive supply positive terminal
16	V_{P1}	W-phase P-side control supply positive terminal
17	COM	Dummy-pin
18	W_P	W-phase P-side control input terminal
19	UNG	Dummy-pin
20	VNO	(Note 2)
21	U_N	U-phase N-side control input terminal
22	V_N	V-phase N-side control input terminal
23	W_N	W-phase N-side control input terminal
24	F_O	Fault signal output terminal
25	CFO	Fault pulse output width setting terminal
26	CIN	SC current trip voltage detecting terminal
27	V_{NC}	N-side control supply GND terminal
28	V_{N1}	N-side control supply positive terminal
29	VNG	Dummy-pin
30	WNG	Dummy-pin
31	P	Inverter DC-link positive terminal
32	U	U-phase output terminal
33	V	V-phase output terminal
34	W	W-phase output terminal
35	N	Inverter DC-link negative terminal

Note:

1) Don’t connect all dummy-pins to any other terminals or PCB pattern.
2) VNO terminal treatment way:
   Connect it with N terminal for PS21562-P(5A/600V) or PS21563-P(10A/600V);
   Leave it open for PS21564-P(15A/600V).

3.5.2 Detailed Description of Input / Output Terminals

Table 10. Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	$U(V_{UFB})$–V_{UFS} $V(V_{VFB})$–V_{VFS} $W(V_{WFB})$–V_{WFS}	• Drive supply terminals for the P-side IGBTs. • By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIPIPM P-side IGBT drives. Each bootstrap capacitor is charged by the N-side VD supply during ON-state of the corresponding N-side IGBT in the loop. • Abnormal operation might happen if the VD supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a smoothing capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a smoothing capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals. • Voltage input type. These terminals are internally connected to Schmitt trigger circuit composed by 5V-class CMOS. • The wiring of each input should be as short as possible (less than 2 cm) to protect the DIPIPM from noise interference. • To prevent signal oscillations, an RC coupling is reccomended.
Short-circuit trip voltage detecting terminal	CIN	• Current sensing resistor should be connected between this terminal and V_{NC} to detect short-circuit accidents (short-circuit voltage trip level). Input impedance for CIN terminal is approximately 600kΩ. • RC filter should be connected for noise immunity.
Fault signal output terminal	F_O	• Fault signal output terminal. • This output is open drain type. F_O signal line should be pulled up to a 5V logic supply with approximately 10kΩ resistor.
Fault pulse output width setting terminal	CFO	• The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and VNC to set the fault pulse width. • The capacitor of 22nF is recommended (corresponding to 1.8ms typical value of fault pulse output time).
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted verry closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	N	• DC-link negative power supply terminal (power ground) of the inverter. • This terminal is connected internally to the emitters of all N-side IGBTs.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.

3.5.3 Description of Protective Functions

Table 11. Description of protective functions

Function	Symbol	Description
Normal drive	-	• "high-active" drive logic. • A low-level input signal ($V_{CIN} < V_{th(off)}$) drives IGBT off, and a high-level input signal ($V_{CIN} > V_{th(on)}$) drives IGBT on.
Short circuit protection	SC	• The external shunt resistor detects bus current of the DC-link. A short circuit is regarded when the current exceeds the specified SC trip level, and the N-side IGBTs are turned off immediately. • A fault pulse signal is output from Fo terminal when an SC current flows through the external shunt resistor. The pulse duration is determined by the capacitance of the capacitor connected between CFO and VNC. The reset operation is performed at the first on-lever signal input soon after Fo pulse duration .
Control supply under voltage protection (UV)	UV_D	• An internal logic monitors the N-side control supply voltage. If the voltage falls below the UV_D trip level for a given period of time, input signals to the N-side IGBTs are locked. • The state of control circuit under-voltage protection continuous until the voltage exceeds the UV_{Dr} reset level. • The fault resetting takes place at the next input signal if control supply voltage rises over the reset level.
	UV_{DB}	• An internal logic monitors the P-side floating supply voltage. If the voltage level drops below the UV_{DB} trip level for a given period of time, input signal for the corresponding P-side IGBT will not be accepted. • The state of control circuit under-voltage protection continuous until the voltage exceeds the UV_{DBr} reset level. • Fault signal is not output for the P-side UV failure.

3.5.4 Operation Sequence

DIPIPM Ver.3 is designed with high-active input logic, which is different from that of Ver.2.

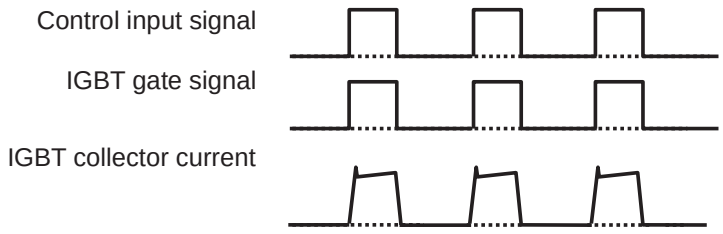


Figure 3-7 Operation sequence

3.5.5 Installation Guidelines (Flatness / Mounting Strength / Screw Type / Grease)

When installing a module to a heat sink, excessive uneven fastening way might apply stress to inside chips, which will lead to a broken or degradation of the device. An example of recommended fastening order is shown in Figure 3-8.

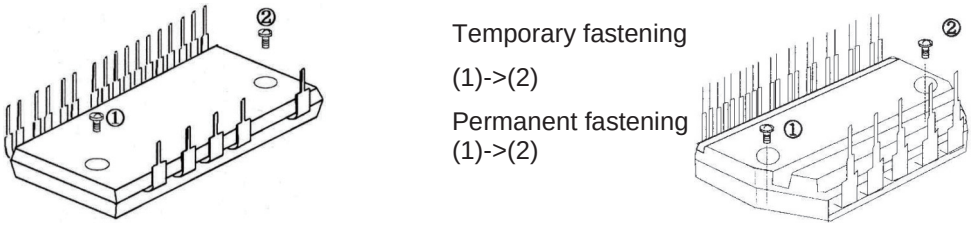


Figure 3-8. Recommended fastening order

Note: Generally, the temporary fastening torque is set to 20~30% of the maximum torque rating.

Table 12. Mounting torque and heat sink flatness specifications

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Large DIPIPM	Recommended 1.18N·m Mounting screw : M4	0.98	1.18	1.47	N·m
	mini DIPIPM	Recommended 0.78N·m Mounting screw : M3	0.59	0.78	0.98	N·m
Case surface flatness	See Fig. 3-9(a)		-50	-	+100	μm
Heat sink flatness	See Fig. 3-9(b)		-50	-	+100	μm

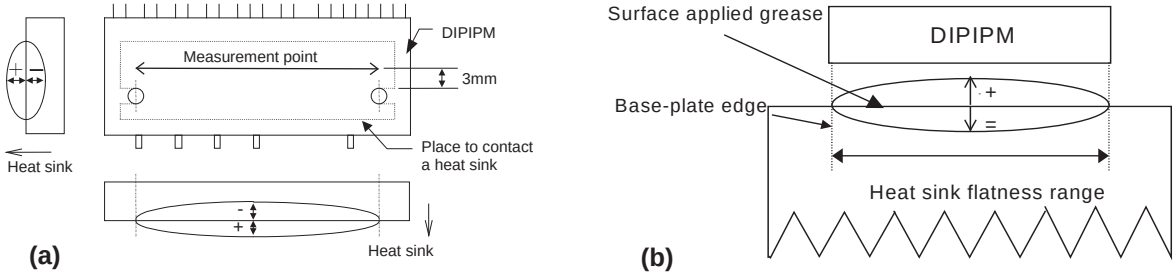


Figure 3-9. Measurement point of heat sink flatness

Note: The measurement point of mini DIPIPM is 3mm away from the screw, toward the power terminals.

In order to get most effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface (refer to Fig.3-9), the surface finishing-treatment should be within Rz12.

Evenly apply thermally-conductive grease with 100μm~200μm over the contact surface between a module and a heat sink, which is also useful for preventing the contact surface from corrosion. Furthermore, ensure the grease to be with stable quality and long endurance within wide operating temperature range. Use a torque wrench to fasten up to the specified torque rating. Exceeding the maximum torque limitation might cause a module to be damaged or degraded. Also, pay attention not to have any desert remaining on the contact surface between the module and the heat sink.

CHAPTER 4 APPLICATION SYSTEM

4.1 System Connection Diagram

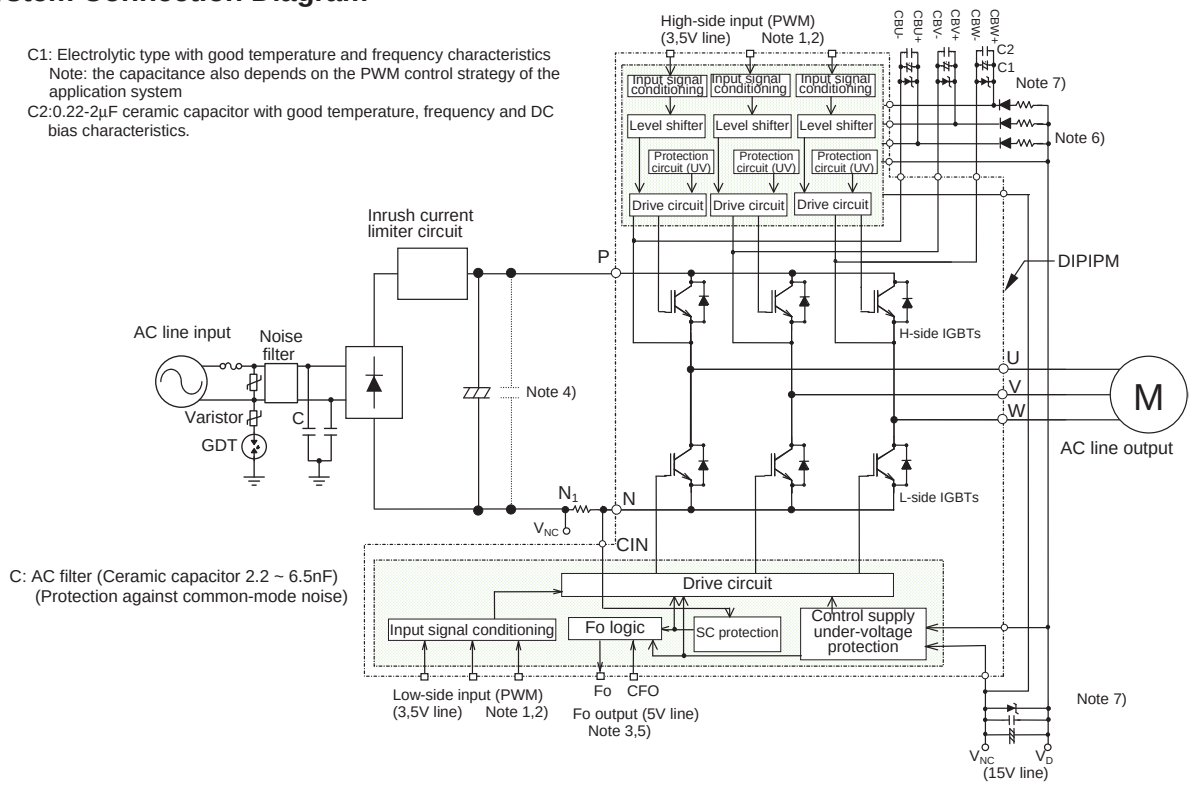


Figure 4-1. System block diagram of DIPIPM (e.g. Large DIPIPM)

Note 1) Input signal is high active logic. A 2.5kΩ(min.) resistor is built-in each input circuit. If external RC filter is used for noise immunity, pay attention to the variation of the input signal level.

Note 2) By virtue of integrating HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.

Note 3) Fo output is open drain type. This signal line should be pulled up to the positive side of a 5V supply with an approximate 10kΩ resistor.

Note 4) The wiring between the power DC-link capacitor and the P,N1 terminals should be as short as possible to protect DIPIPM against catastrophic high surge voltage. For extra precaution, a small film type snubber capacitor (0.1~0.22μF, high voltage type) is recommended to mount closely to the P and N1 terminals.

Note 5) Fo output pulse width (t_{FO}) should be determined by connecting external capacitor between CFO and VNC terminals. (Example :C_{FO} = 22nF -> t_{FO} = 1.8ms (typ.)).

Note 6) Use high voltage (over 600V) and high-speed recovery diode should be used for the bootstrap circuit.

Note 7) To prevent HVIC from surge destruction, it is recommended to insert a Zener diode (24V, 1W) between each control supply terminals.

4.2 Input circuit

4.2.1 Structure of Control Input Terminals and Application Examples

DIPIPM Ver.3 series employ High-Active input logic which released the sequence restriction between the control supply and the input signal in start-up or shut-down operation, therefore, makes the system fail-safe.

In addition, an about 2.5kΩ pull-down resistor is built-in each input circuit of the DIPIPM as shown in Fig. 4-2, hence, external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 13, a direct connection to 3V-class MCU or DSP becomes possible.

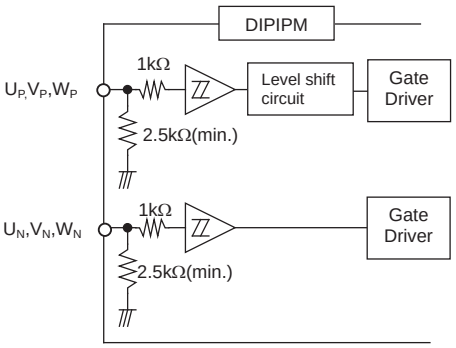


Figure 4-2. Internal structure of control input terminals

Table 13. Input threshold voltage ratings（VD=15V, Tj＝25°C）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1.Turn-on threshold voltage	Vth(on)	U_P, V_P, W_P-V_{NC} terminals	2.1	2.3	2.6	V
2.Turn-off threshold voltage	Vth(off)	U_N, V_N, W_N-V_{NC} terminals	0.8	1.4	2.1	V

4.2.2 Input Signal Voltage Rating

The input signal and the fault signal input/output is applicable not only for 3~5V class interface but also for 15V class interface. The maximum ratings for input signal and F_O output voltages are shown in Table 14. Since F_O is an open drain type terminal, it should be pulled up to the positive side of a 5V (or 15V) supply.

Table 14. Maximum ratings of input voltage and fault output voltage (Tj＝25°C)

Item	Symbol	Condition	Rating	Unit
Input voltage	V_{CIN}	Applied between U_P,V_P,W_P-V_{NC}, U_N,V_N,W_N-V_{NC}	-0.5~V_D+0.5	V
Fault output voltage	V_{FO}	Applied between Fo-V_{NC}	-0.5~V_D+0.5	V

4.2.3 Minimum Rating of Control Input Pulse Width

Table 15. Minimum rating of control input pulse width

Item		Condition		Part No.	min.	typ.	max.	Unit
Allowable minimum pulse width of control input	PWIN(on)	-	-	All	0.3	-	-	μsec
	PWIN(off)	200≤VCC≤350V, 13.5≤VD≤16.5V, 13.0≤VDB≤18.5V, -20≤Tf≤100°C, N-line inductance less than 10nH	Below rated current	PS21562-P	0.5	-	-	
				PS21563-P	0.5	-	-	
				PS21564-P	0.5	-	-	
				PS21865-P	1.4	-	-	
				PS21867-P	1.5	-	-	
				PS21869-P	3.0	-	-	
			Between rated current and 1.7 times of rated current	PS21562-P	0.5	-	-	
				PS21563-P	0.5	-	-	
				PS21564-P	2.0	-	-	
				PS21865-P	2.5	-	-	
				PS21867-P	3.0	-	-	
				PS21869-P	5.0	-	-	
			Between 1.7 times and 2.0 times of rated current	PS21562-P	0.5			
				PS21563-P	0.7			
				PS21564-P	2.6			
				PS21865-P	3.0			
				PS21867-P	3.6			
				PS21869-P	5.9			

Note: DIPIPM might make no response to an input on signal with pulse width less than PWIN(on);
DIPIPM might make no response or not work if the input off signal pulse width is less than PWIN(off).

4.3 Single Supply Drive Scheme

4.3.1 Initial Charging

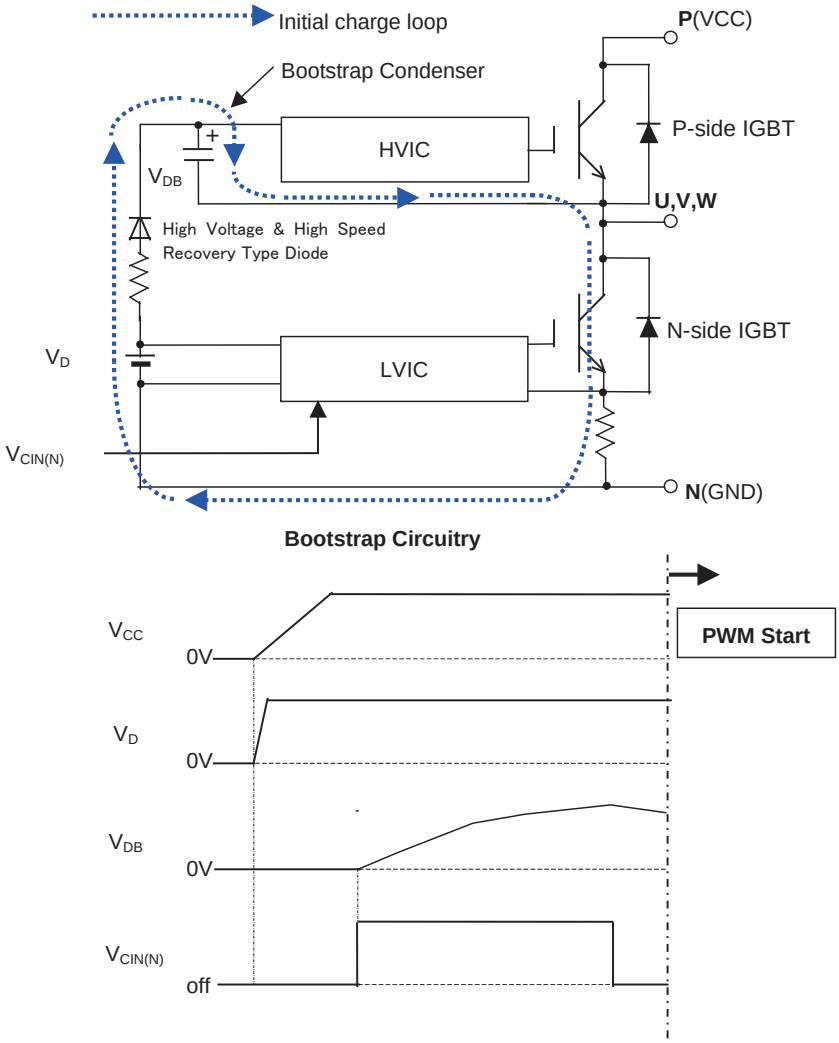


Figure 4-3. Charging current loop and timing chart of bootstrap circuit

Charging:

In order to start the DIPIPM, initial bootstrap charging is necessary. By turning on the N-side IGBT, as shown in Figure 4-3, the bootstrap capacitor will be charged. The pulse width or pulse number should be large enough for a full charge of the bootstrap capacitor.

4.3.2 Charging and Discharging of the Bootstrap Capacitor During Inverter Operation

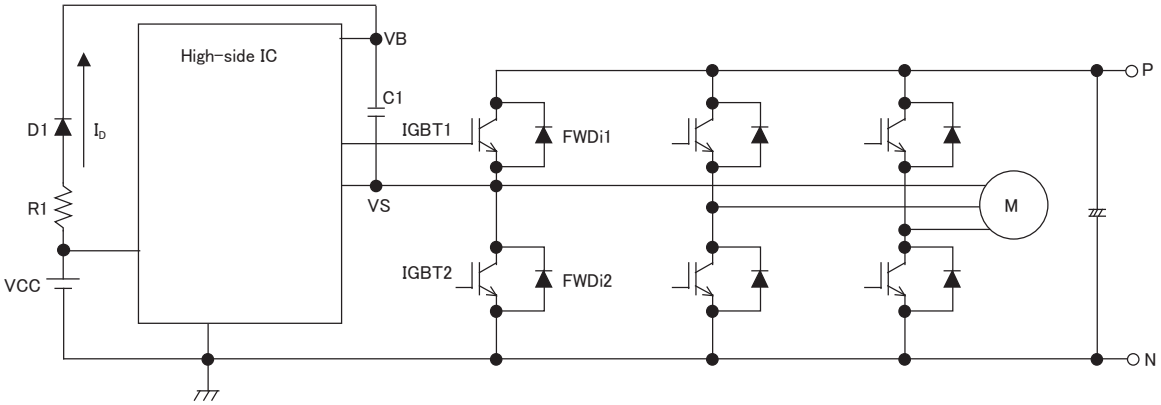


Figure 4-4. Inverter circuit diagram

(1) Charging operation Timing Chart of Bootstrap Capacitor (C1)

Sequence (1-1) : IGBT2 ON (Figure 4-5)

When IGBT2 is in the ON state, charging voltage on C1 ($V_{C(1)}$) is calculated by

$V_{C(1)} = V_{CC}-V_{F1}-V_{sat2}-I_D \cdot R1$ (Transient state)

$V_{C(1)} = V_{CC}$ (Steady state)

V_{CC} is the charging supply voltage, V_{F1} the forward voltage drop of diode D1, V_{sat2} the saturation voltage of IGBT2, I_D the charging current, and R1 the inrush current limitation resistance.

Then, IGBT2 is turned off. Motor current will flow through the free-wheel path of FWD1. Once the electric potential of VS rises near to that of P, the charging to C1 is stopped.

When IGBT1 is in ON state, the voltage of C1 gradually declines from the potential $V_{C(1)}$ due to the current consumed by the drive circuit.

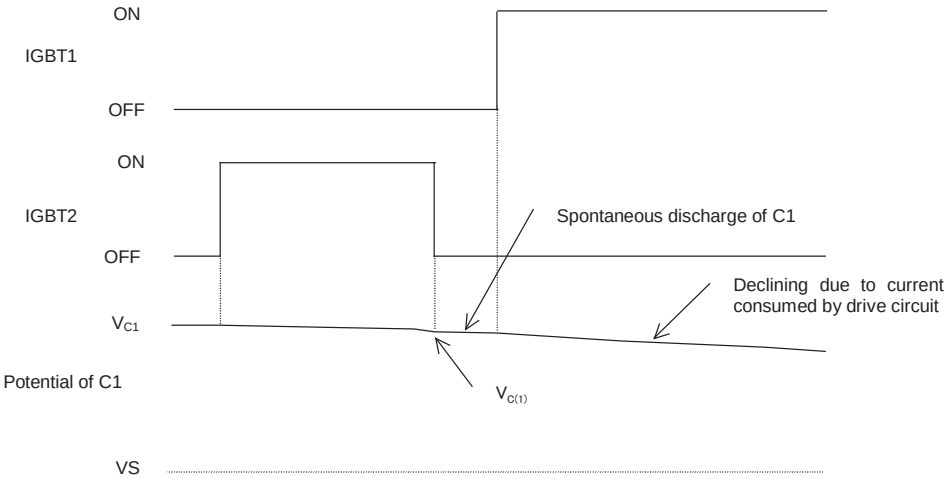


Figure 4-5. Timing chart of sequence (1-1)

Sequence (1-2): IGBT2 OFF and FWD2 ON (Figure 4-6)
When IGBT2 is OFF and FWD2 is ON, the voltage on C1 ($V_{C(2)}$) is calculated by:

$$V_{C(2)}=V_{CC}-V_{F1}+V_{EC2}$$

where V_{EC2} denotes the forward voltage drop of FWD2. When both IGBT2 and IGBT1 are OFF, the regenerative current flows continuously through the free-wheel path of FWD2. Therefore the potential of VS drops to $-V_{EC2}$, then C1 is recharged to restore the declined potential. When IGBT1 is turned ON, the potential of V_S rises to that of P, the charge to C1 stops and the voltage on C1 gradually declines from the potential $V_{C(2)}$ due to the current consumed by the drive circuit.

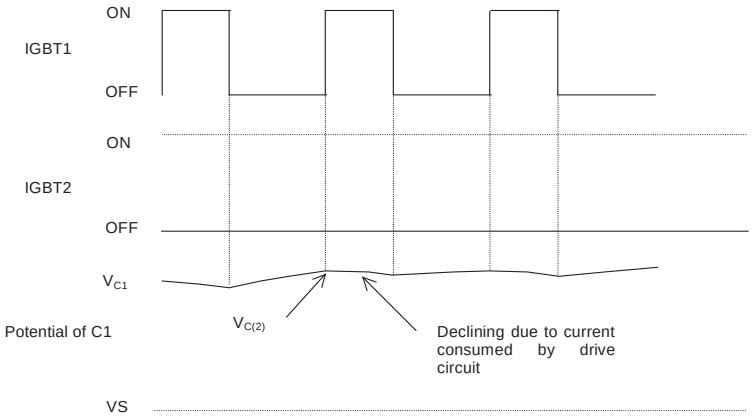


Figure 4-6. Timing chart of sequence (1-2)

（2）Guidelines of Selecting the Bootstrap Capacitor (C1) and Resistance (R1)
The capacitance of bootstrap capacitor can be calculated by:

$$C1=I_{BS}XT1/\Delta V$$

where T1 is the maximum ON pulse width of IGBT1 and I_{BS} is the drive current of the IC (depends on temperature and frequency characteristics), and ΔV is the allowable discharge voltage. A certain margin should be added to the calculated capacitance.
Resistance R1 should be basically selected such that the time constant C1·R1 will enable the discharged voltage (ΔV) to be fully charged again within the minimum ON pulse width (T2) of IGBT2.
However, if only IGBT1 has an ON-OFF-ON control mode (Figure 4-7), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.

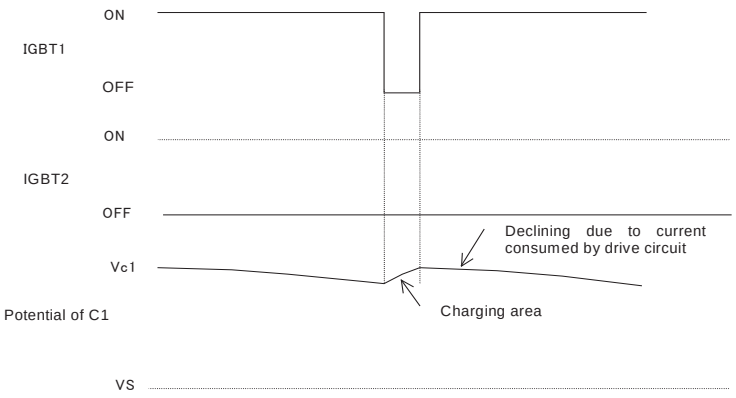


Figure 4-7. Timing Chart of ON-OFF-ON Control Mode

Designing example of Bootstrap circuit

■ Selecting bootstrap capacitor

Condition: ΔV_{DB}(discharged voltage)=1V, The maximum ON pulse width T1 of Upper-side IGBT is 5ms, I_{DB} is 0.4mA(Max. rating).

$$C=I_{DB}XT1/\Delta V_{DB}=2.0X10^{-6}$$

The calculated bootstrap capacitance is 2.0μF. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one.

■ Selecting bootstrap resistor

Condition: The value of bootstrap capacitor is 5μF, V_D=15V, V_{DB}=14V. If the minimum ON pulse width t_0 of lower-side IGBT or the minimum OFF pulse width t_0 of upper-side IGBT is 20μs, bootstrap capacitor needs to be charged ΔV_{DB}=1V during this period, therefore,

$$R=\{(V_D-V_{DB})Xt_0\}/(CX\Delta V_{DB})=4$$

The bootstrap resistor should be 4Ω.

In the case of the control for DCBLM or 2-phase modulation for IM (Induction Motor), there will be a long ON time period on the high-side IGBT, please pay attention to the bootstrap supply voltage drop.

Note:

The above result is only a calculation example. It is recommended that you design a system by taking consideration of the actual control pattern and lifetime of components.

■ Selecting bootstrap diode

The bootstrap diode with withstand-voltage more than 600V is recommended. In DIPIPM, the maximum rating of power supply is 450V. The actual voltage applied on the diode is 500V including a surge voltage of about 50V. Furthermore, if considering 100V for the margin, 600V class diode is necessary. The diode is also highly recommended to be with fast recovery characteristics (recovery time is less than 100ns).

Reference:

Recommended bootstrap diode: 10DF06 made by Inter Co., Japan.

■ Noise filter for control supply

It is recommended to insert a film type or ceramic type noise filter with 0.22~2μF to the control supply terminals(V_{P1}-V_{PC}, V_{N1}-V_{NC}, V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}). The smaller the supply parasitic impedance is , the smaller a feasible noise filter capacitance can be . The supply circuit should be such designed that the noise fluctuation is less than ±1V/μs, and the ripple voltage is less than ±2V.

Reference:

There are tow kinds of control supply in general use. The first one is DC-DC converter (3-terminal regulator), of which input DC supply comes from AC-transformer. The other is DC-DC converter (switching regulator), of which input DC supply comes from DC-link supply directly.

Note:

After bootstrap voltage have been fully charged, please input one pulse as the reset pulse of P-side input signal before starting PWM.

4.3.3 Current Characteristics

Figure 4-8~4-10 show the current characteristics of P-side bootstrap supply versus carrier frequency under different temperature, respectively. (Typical for PS21865-P)

Conditions: V_D=V_{DB}=15V, Tj=-20, 25, 125°C., Duty=10, 30, 50, 70, 90%

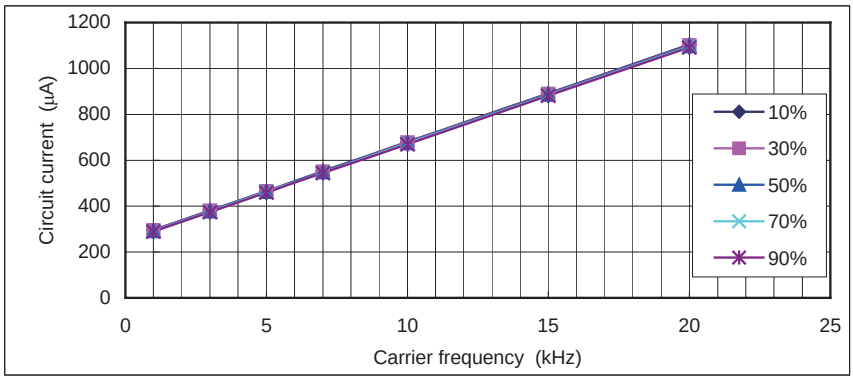


Figure 4-8 Current characteristics at Tj=-20°C

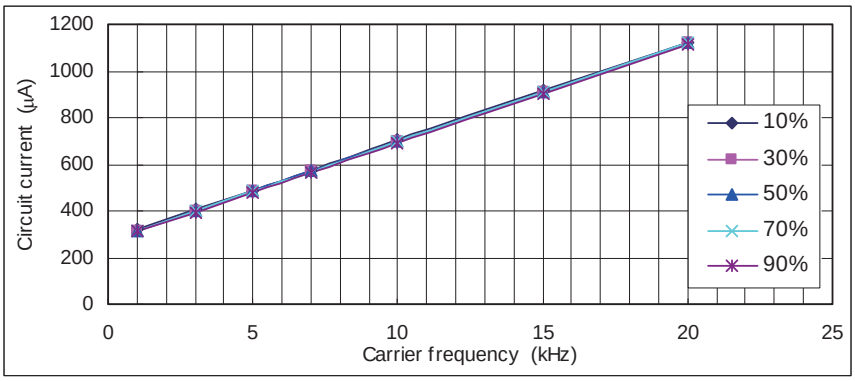


Figure 4-9 Current characteristics at Tj=25°C

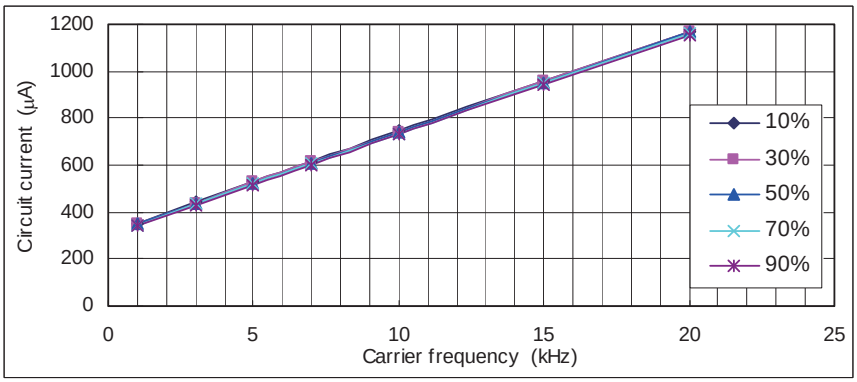


Figure 4-10 Current characteristics at Tj=125°C

Table 16. Typical value of circuit current for PS21865-P

(unit: μA)

Tj (°C)	Carrier Freqency fc(kHz)	Duty (%)				
		10	30	50	70	90
-20	1	296	294	292	291	289
	3	381	380	378	376	374
	5	466	464	463	461	459
	7	552	549	548	546	544
	10	680	677	675	673	670
	15	892	889	886	884	881
	20	1104	1101	1098	1095	1092
25	1	318	316	314	312	310
	3	404	402	400	398	395
	5	490	488	485	483	480
	7	575	573	571	568	565
	10	703	700	698	696	692
	15	914	912	910	907	903
	20	1125	1123	1121	1118	1114
125	1	353	351	348	346	343
	3	441	439	436	433	429
	5	528	526	523	520	516
	7	615	612	609	606	602
	10	745	742	738	734	730
	15	958	955	951	947	943
	20	1166	1167	1165	1161	1157

4.4 Interface Circuit Examples and Guidelines

4.4.1 Example of Direct Input Interface

Figure 4-11 shows a typical application circuit of interface schematic for PS21562-P and PS21563-P, where control signals are transfered directly from a microcomputer.

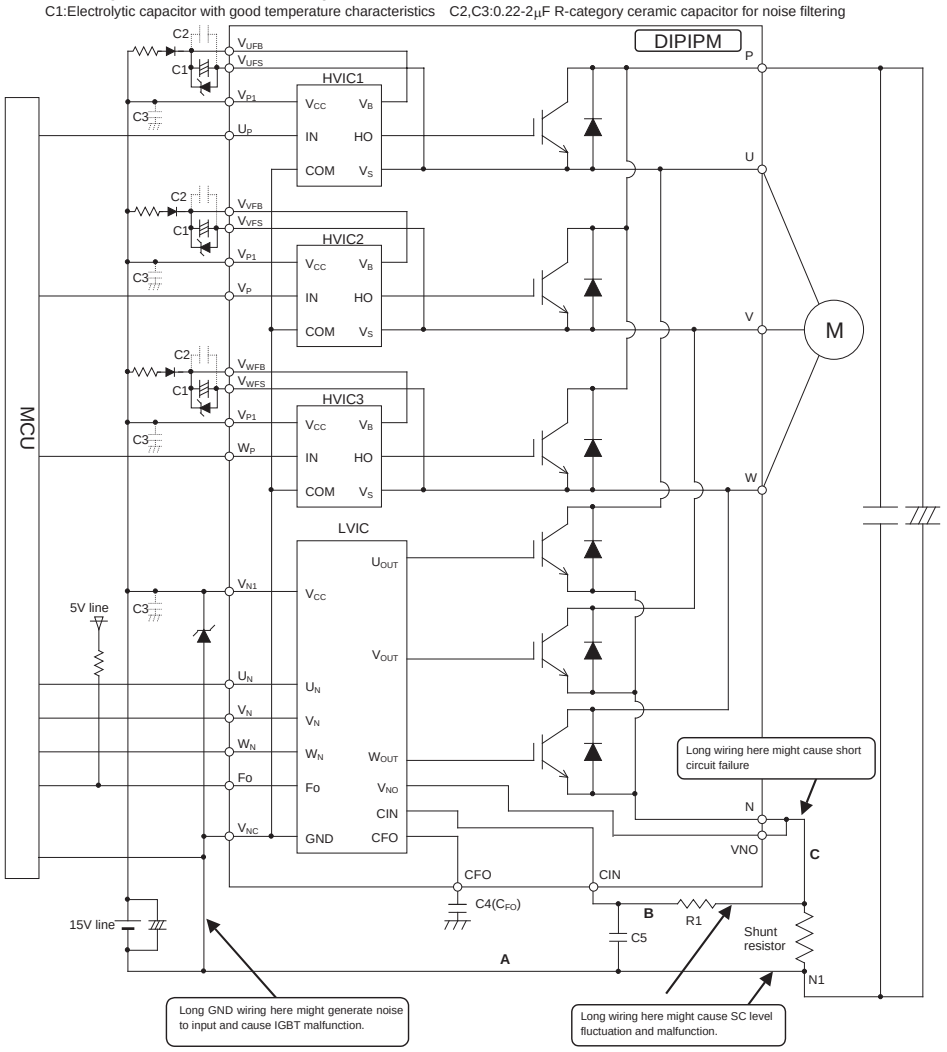


Figure 4-11. A example of interface circuit without opto-coupler

Note:

(1) Input drive is High-Active type. There is a 2.5kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(2) Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(3) Fo output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.

(4) Fo output pulse width can be determined by connecting an external capacitor between CFO and V_{NC} (C_{FO}). (e.g. C_{FO}=22nF->t_{FO}=1.8ms(typ.))

(5) To prevent erroneous protection, the wiring of A, B, C should be as short as possible.

(6) The time constant R1C5 of the protection circuit should be selected in the range of 1.5-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1,C5

(7) All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3 : good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(8) To prevent surge destruction, the wiring between the smoothing capacitor and the P,N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber between the P-N1 terminals is recommended.

(9) Connect V_{NO} terminal with N outside for PS21562-P and PS21563-P

(10) It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

(11) If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.

Figure 4-12 shows a typical application circuit of interface schematic for PS21564-P, where control signals are transfered directly from a microcomputer.

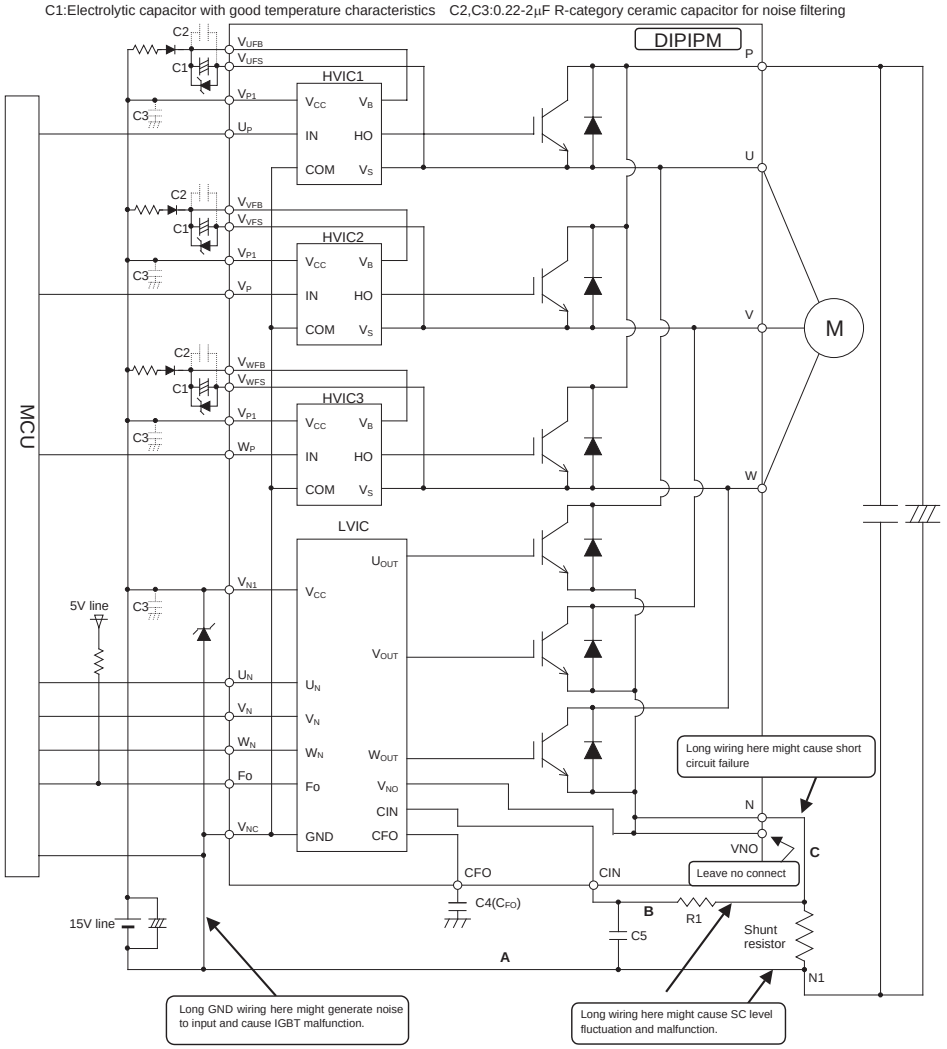


Figure 4-12. A example of interface circuit without opto-coupler

Note:

(1) Input drive is High-Active type. There is a 2.5kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(2) Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(3) Fo output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.

(4) Fo output pulse width can be determined by connecting an external capacitor between CFO and V_{NC} (C_{FO}). (e.g. C_{FO}=22nF->t_{FO}=1.8ms(typ.))

(5) To prevent erroneous protection, the wiring of A, B, C should be as short as possible.

(6) The time constant R1C5 of the protection circuit should be selected in the range of 1.5-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1,C5

(7) All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3 : good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(8) To prevent surge destruction, the wiring between the smoothing capacitor and the P,N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber between the P-N1 terminals is recommended.

(9) Leave V_{NO} terminal no connect because it is connected inside.

(10) It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

(11) If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.

Figure 4-13 shows a typical application circuit of interface schematic for PS2186X-P, where control signals are transfered directly from a microcomputer.

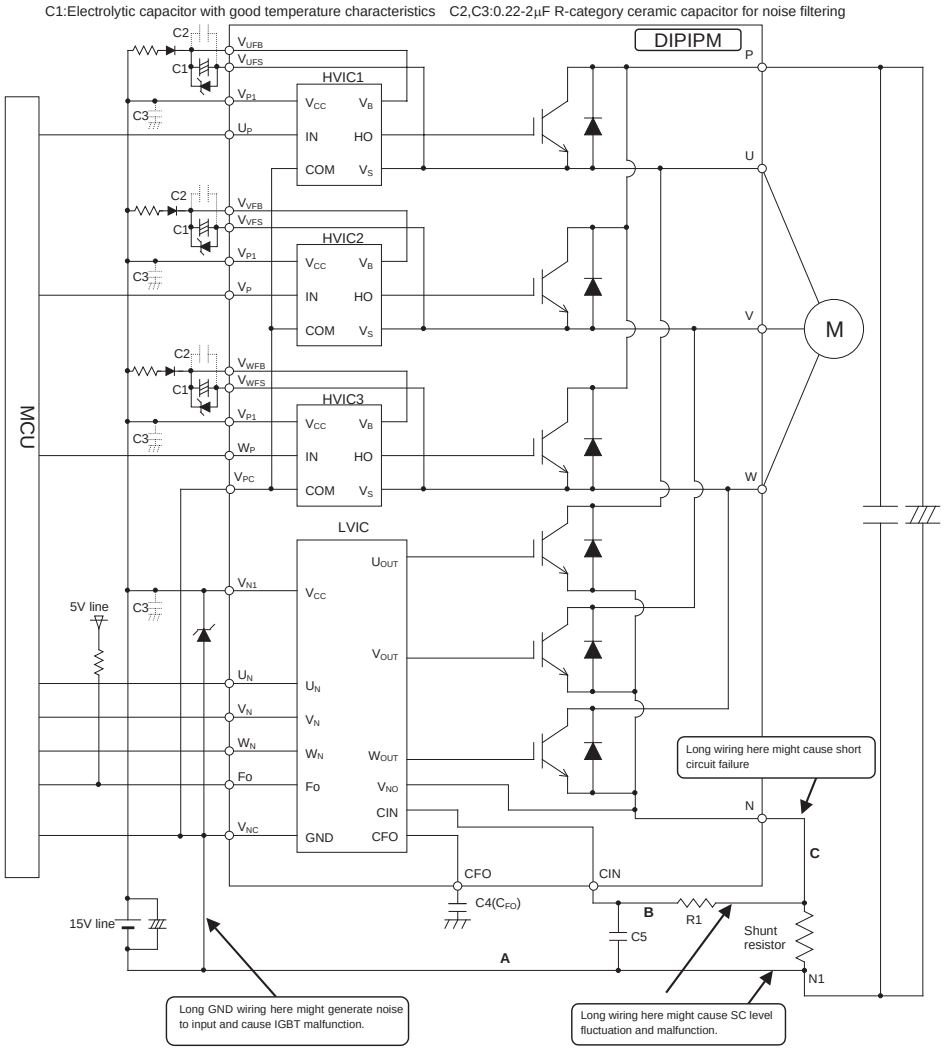


Figure 4-13. A example of interface circuit without opto-coupler

Note:

(1) Input drive is High-Active type. There is a 2.5kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(2) Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(3) Fo output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.

(4) Fo output pulse width can be determined by connecting an external capacitor between CFO and V_{NC} (C_{FO}). (e.g. C_{FO}=22nF->t_{FO}=1.8ms(typ.))

(5) To prevent erroneous protection, the wiring of A, B, C should be as short as possible.

(6) The time constant R1C5 of the protection circuit should be selected in the range of 1.5-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1,C5

(7) All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3 : good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(8) To prevent surge destruction, the wiring between the smoothing capacitor and the P,N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber between the P-N1 terminals is recommended.

(9) It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

(10) If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.

4.4.2 Example of Interface with Fast Opto-Coupler

Figure 4-14 shows a typical application circuit interface schematic for PS2186X-P by using fast Opto-Coupler (except Fo).

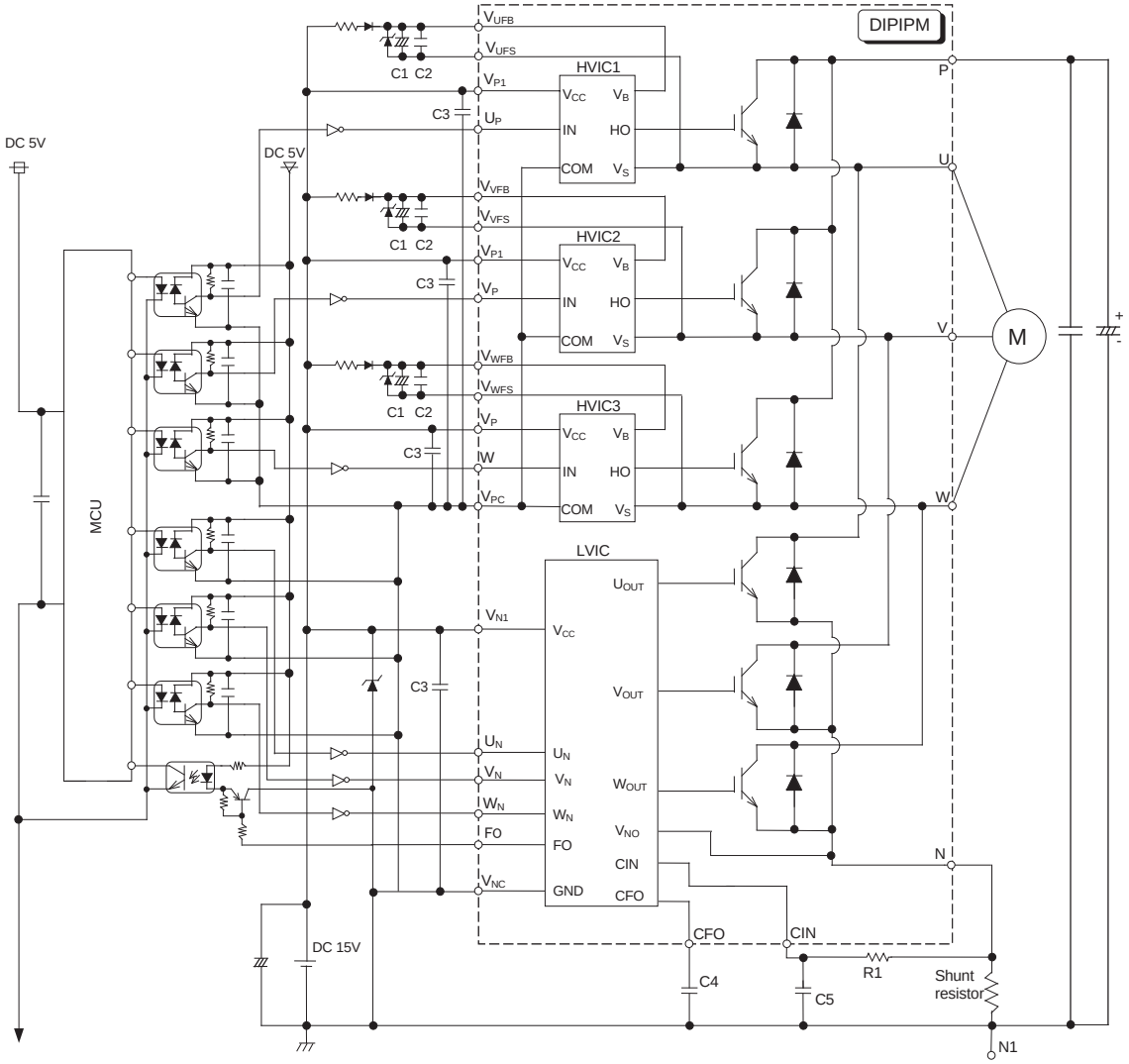


Figure 4-14. An example of interface circuit with fast opto-Coupler

Note:

(1) Fast type opto-coupler (High CMR) is recommended for electric isolation. Slow type opto-coupler leads to much longer time in signal rising and falling edge therefore is not recommended.

(2) Because Fo output current is 1mA(max) which cannot drive directly an opto-coupler, a buffer circuit should be added in the primary side of the opto-coupler.

4.4.3 Snubber Circuit

There are two positions ((1)or(2)) to mount a snubber capacitor to the DIPIPM as shown in Figure 4-15. Snubber capacitor should be installed in the position (2) so as to suppress surge voltage effectively. However, the charging and discharging currents generated by the wiring inductance and the snubber capacity will flow on the shunt resistor, which might cause an error protection if this current is large enough to reach the SC trip level on the shunt resistor.

In order to suppress the surge voltage maximally, the wiring at part-A should be as short as possible when mounting a snubber capacitor outside the shunt resistor as shown in position (1). An effective wiring example is shown in location (3).

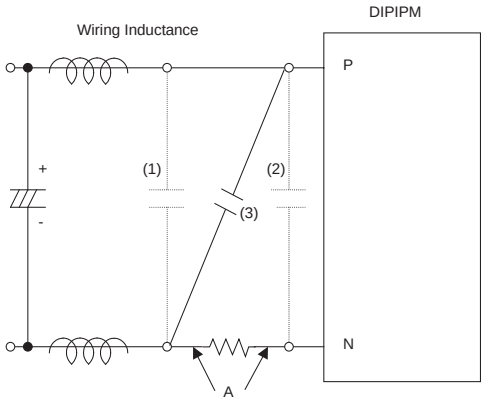


Figure 4-15 Instruction for snubber circuit location

4.4.4 Parallel Connection

Figure 4-16 shows the circuitry of parallel connection of two DIPIPMs.

Route (1) and (2) indicate the gate charging path of low-side IGBT in DIPIPM No.2. If the route is too long, gate voltage might drop due to large voltage drop on the wiring, which will result a bad effect to the second IPM operation. (Charging of bootstrap capacitor for high-side is similar, too.).

In addition, noise might easily impose to the wiring impedance. If there are many DIPIPM parallel connected, GND pattern becomes long and the influence to other circuit (power supply, protection circuit etc.) by the fluctuation of GND potential is conceivable, therefore parallel connection is not recommended.

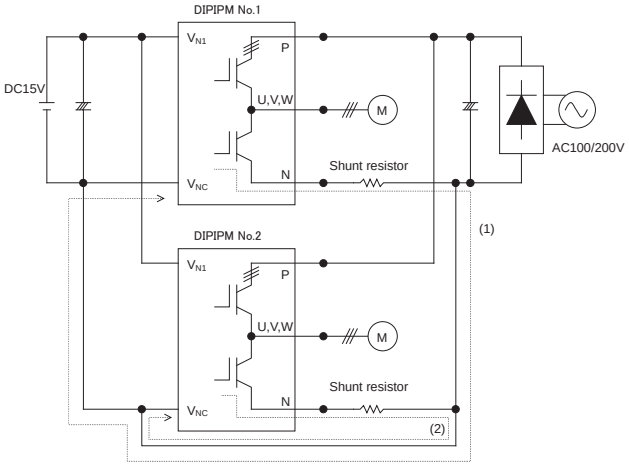


Figure 4-16 Parallel Connection

4.4.5 Input Signal Connection

Because input logic of DIPIPM Ver.3 is High-Active and there is pull-down resistor built-in each input circuit, external pull-up or pull-down resistor is no longer needed.

DIPIPM has limitation for the allowable minimum input pulse width, especially the off pulse width. DIPIPM might make no response or not work properly if the pulse width is less than the specified one. Please refer to Fig.4-17(b) for the countermeasure against possible small pulse width input.

Fo output is open drain type. This signal line should be pulled up to the positive side of the 5V power supply by a resistor of approximate 10kΩ.

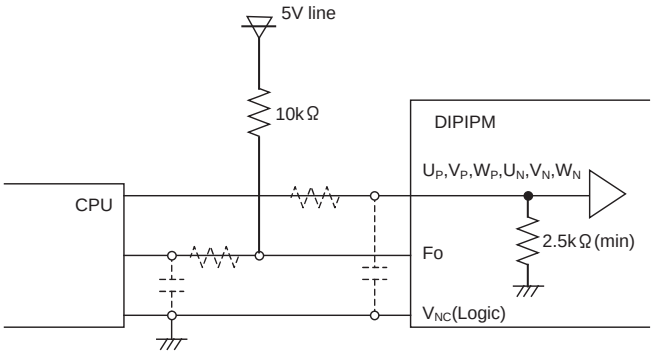


Figure 4-17(a). Input signal connection

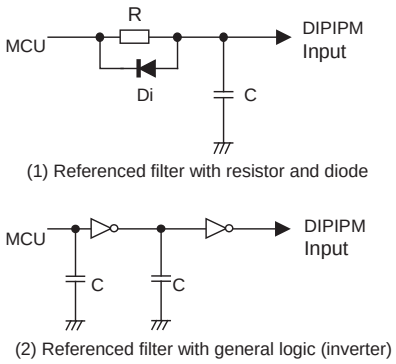


Figure 4-17(b). Example of Filter for narrow off pulse.

Note: RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board.
The DIPIPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

4.4.6 Recommended Wiring of Shunt Resistor

External current sensing resistor is applied to detect short-circuit accidents. A longer pattern between the shunt resistor and DIPIPM will cause so large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt and DIPIPM should be as short as possible.

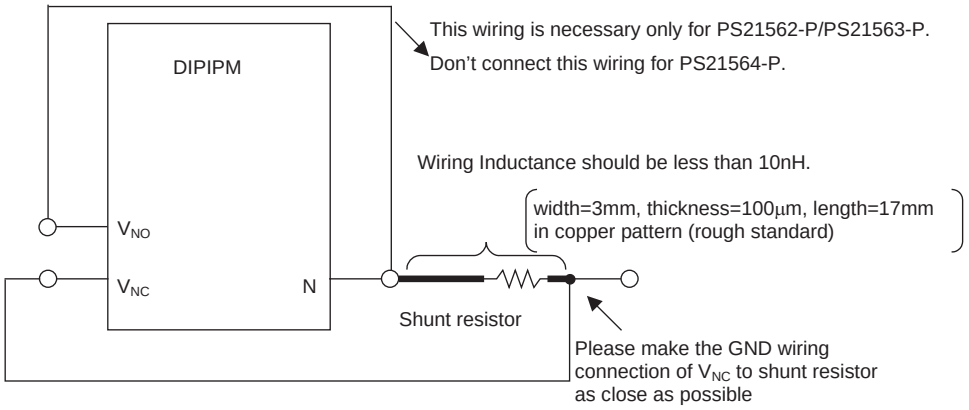


Figure 4-18 Recommendation for wiring of shunt resistor

4.4.7 Precaution for wiring on PCB

Warning points when designing PCB are described in Fig.4-19.
Please refer example of interface circuit as above too.

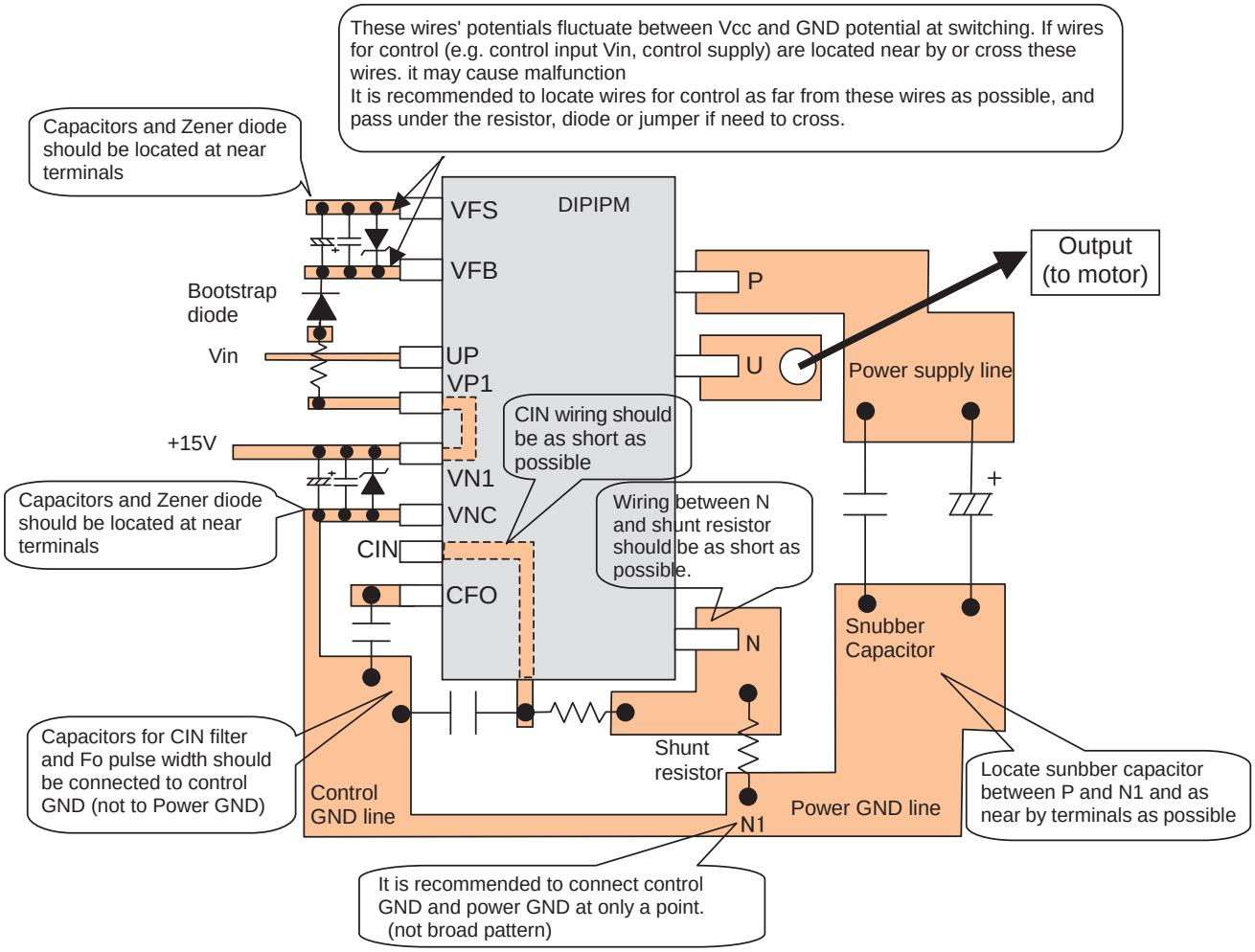


Figure 4-19 Precaution for wiring on PCB

4.5 Short Circuit Protective Function

4.5.1 Timing Chart of Short Circuit (SC) Protection

SC protection (Lower-side only with external shunt resistor and RC filter)

a1.Normal operation: IGBT ON and carrying current
a2.Short circuit detection (SC trigger).
a3.IGBT gate hard interruption
a4.IGBT turns OFF
a5.Fo outputs with a fixed pulse width determined by the external capacitor C_{FO}.
a6.Input “L” : IGBT OFF
a7.Input “H” : IGBT ON
a8.IGBT OFF in spite of input "H"

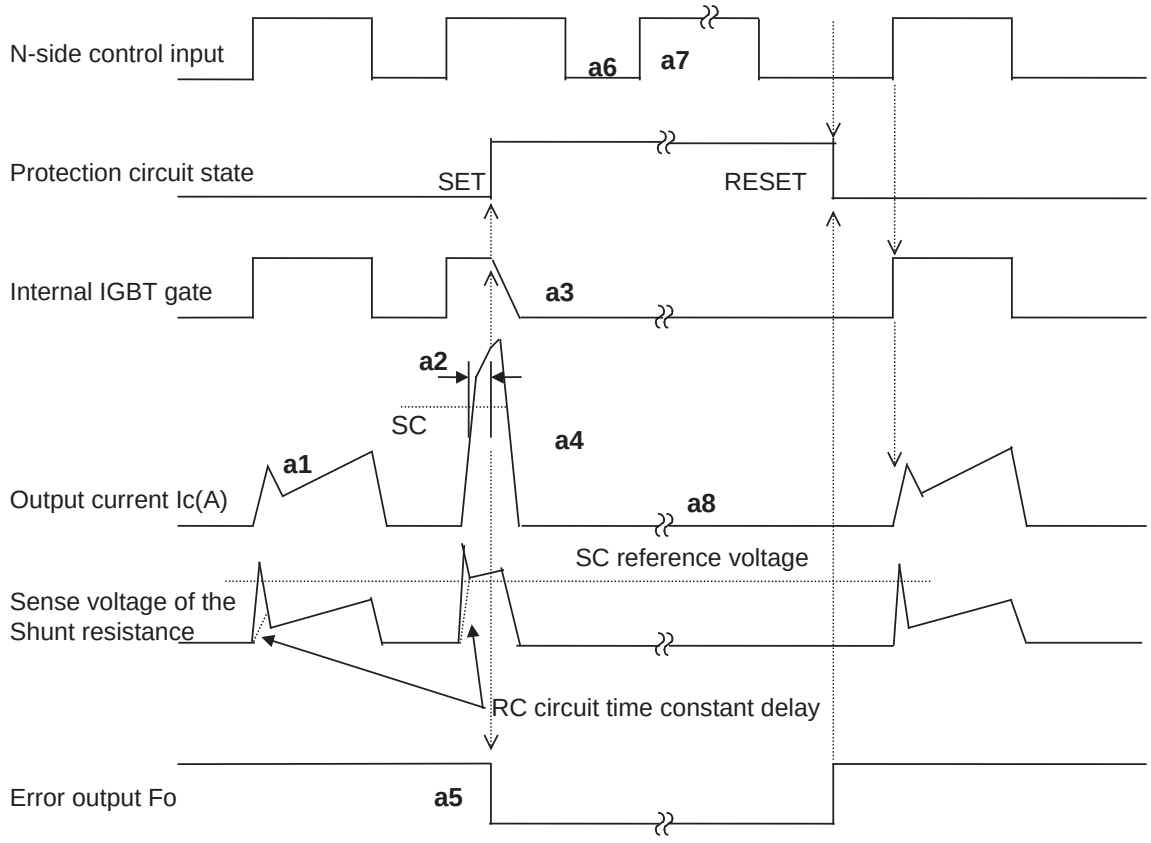


Figure 4-20 Timing chart of SC operation

Note:

The reset of SC protection will not activated unless the Fo level changes from low to high. IGBT will turn ON just at the next Low-to-High input signal.

4.5.2 Selecting Current Sensing Shunt Resistor

(1) Short-Circuit Protection

Figure 4-21 shows an example of external SC protection circuit. The line current on N-side DC-link is detected and the protective operation starts through the RC filter. If the current exceeds the SC reference level, all the gates of the N-side three-phase IGBTs are interrupted and the fault signal is asserted. As short–circuit protection is non-repetitive, IGBT operation should be stopped immediately as soon as the fault output.

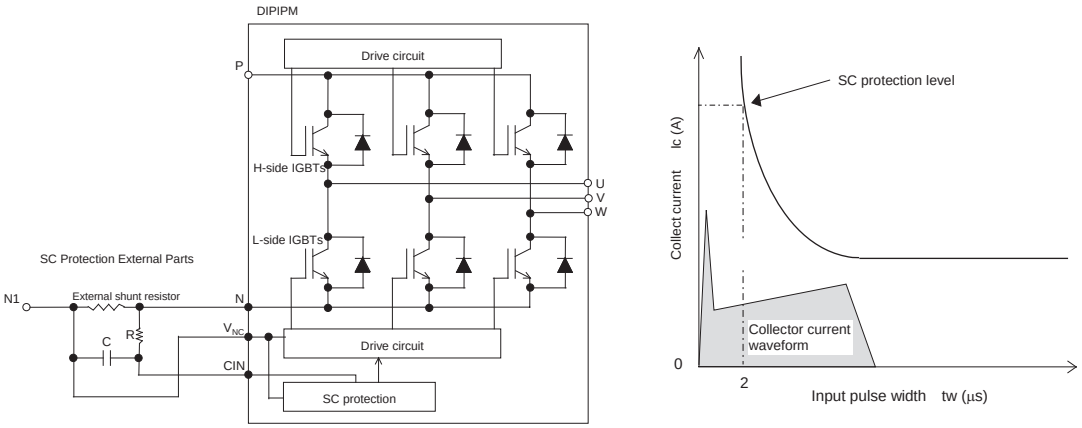


Figure 4-21 Example of external protection circuit

External protection circuit triggers off an SC protection by comparing the external shunt voltage to the reference SC trip voltage in LVIC. Then, LVIC interrupt IGBT gate to stop IGBT operation.

(2) Selecting Shunt Resistance

The value of current sensing resistance is calculated by the following expression :

$$R = V_{SC(ref)}/SC$$

where $V_{SC(ref)}$ is the SC reference voltage (trip level) of the control IC.

The maximum value of SC trip level should be set less than the minimum value of IGBT saturation current which is 2.0 times as large as the rating current. For example, the maximum value of SC trip level of PS21865-P is 2.0 x 20=40A.

Table 17. Specification for $V_{SC(ref)}$ (Unit: V)

	Min	Typ	Max
Specification at -20°C ≤Tj≤125°C	0.45	-	0.52

Similarly, by considering the dispersed property of shunt resistance, SC trip level is calculated as:

SC(max)= $V_{SC(ref)}$max./min. shunt resistance value

SC(min)= $V_{SC(ref)}$min./ max. shunt resistance value

If shunt resistance dispersion is ±5%, then the operative SC level has a variation as shown in Table 18.

Table 18. Operative SC level (unit: A) (Shunt resistance min.13.0mΩ, typ.13.7mΩ, max.14.3mΩ)

	min.	typ.	max.
Operative SC level at -20°C≤Tj≤125°C	31.4	-	40

It is possible that the actual SC protective level is less than a calculated one, due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. The final shunt resistance is recommended to determine by prototype experiment.

4.5.3 Filter Circuit Setting (RC Time Constant) for Short-circuit Protection Operation

(1) RC Time Constant Setting

It is necessary to set an RC filter in order to prevent malfunction of SC protection in case of noise interference. The RC time constant is determined depending on the applying time of noise interference and the withstand voltage capability of the IGBT.

When the voltage drop on external shunt resistor exceeds the SC protective level, the voltage is applied to CIN terminal via the RC filter. The time (t1) that the CIN terminal voltage rises to the referenced SC protective level can be calculated by the following expression:

$$V=R\cdot I\cdot(1-\varepsilon^{-t1/\tau})$$

$$t1=-\tau\cdot\ln(1-(V/R\cdot I)$$

V:SC reference voltage $V_{SC(ref)}$,
R:Shunt resistance,
I :Peak current,
τ :RC time constant,

The typical time delay of IC is shown in Table 19, ever since the IGBT gate starts to be interrupted by SC trip voltage detected at CIN terminal.

Table 19. Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	0.3	0.5	1.0	μs

Therefore, the total time from an SC trip current is detected to the IGBT gate is interrupted becomes:

$$t_{TOTAL}=t1+t2$$

Example)

In the case of PS21865-P, if the maximum value of SC trip level (peak current) is set to 2.0 times of the rated current (i.e.40A), and the shunt resistor is 13mΩ, RC time constant is 2μs, $V_{SC(ref)}$ is 0.53V, then, the characteristics of the maximum current versus interrupting time can be obtained as shown in Figure 4-22

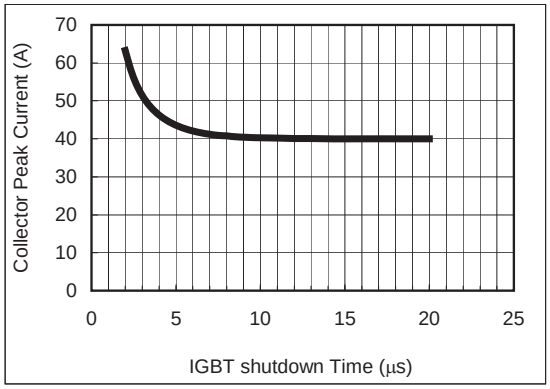


Figure 4-22 PS21865-P Shutdown time characteristics

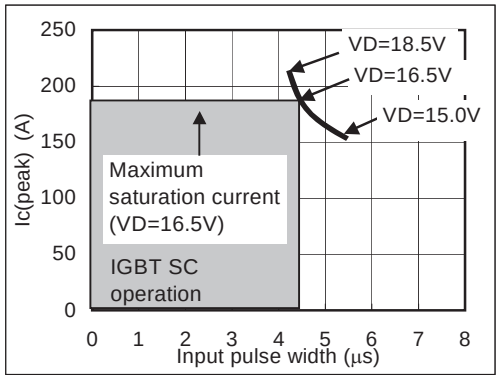


Figure 4-23 PS21865-P short circuit SOA

Figure 4-23 shows the typical safe operation area (SOA) of the 5th gen. IGBT used in PS21865-P under a short circuit failure status with the following condition. The graph illustrates that if the input ON pulse width is less than 4.5μs, IGBT has the ability to turn off safely. In this case IGBT can shutdown an SC current of about 190A under a recommended control supply voltage of 16.5V.

Vcc=400V, Tj=125°C, $V_{th(on)}$=min. non-repetitive, $V_{CES}\leq$600, $V_{cc(surge)}$=500V, 2m-long inductive load

(2) Guidelines of Wiring for Protection Circuit

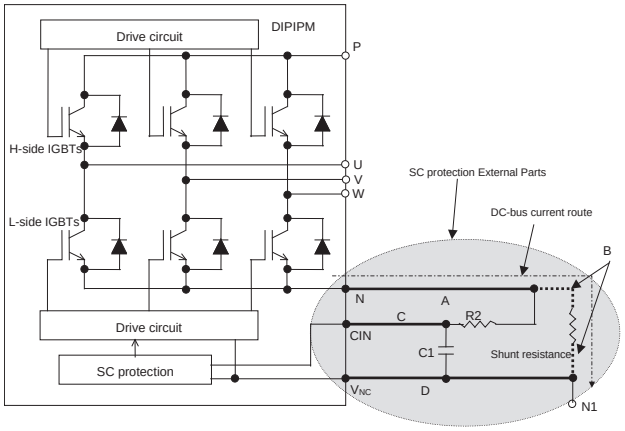


Figure 4-24. External protection circuit

A. Influence of the part-A wiring pattern

The ground of Low-side IGBT gate is V_{NC}. If part-A wiring pattern in Figure 4-24 is too long, voltage fluctuation occurs due to the wiring inductance, which results the potential of IGBT emitter variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

B. Influence of the part-B wiring pattern

The part-B wiring affects SC protection level. SC protection works by judging the voltage over the CIN-V_{NC}(typ.0.48V) terminals. If part-B wiring is too long, surge voltage occurs easily due to the wiring inductance, therefore leads to deterioration of SC protection level. It is necessary to connect CIN and VNC directly to the two ends of shunt resistor and avoid the part-B wiring area.

C. Influence of the part-C wiring pattern

R2C1 filter is added to remove noise influence occurring on shunt resistor. Filter effect will become small and noise is easy to impose on the wiring if part-C wiring is too long. Please install a R2C1 filter near CIN, VNC terminal as close as possible.

D. Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described in above item A~C, therefore, GND wiring should be as short as possible.

4.5.4 SOA of DIPIPM

The following describes the SOA (Safety Operating Area) of the DIPIPM.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: The add of V_{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(PROT)}$: DC-link voltage that DIPIPM can protect itself.

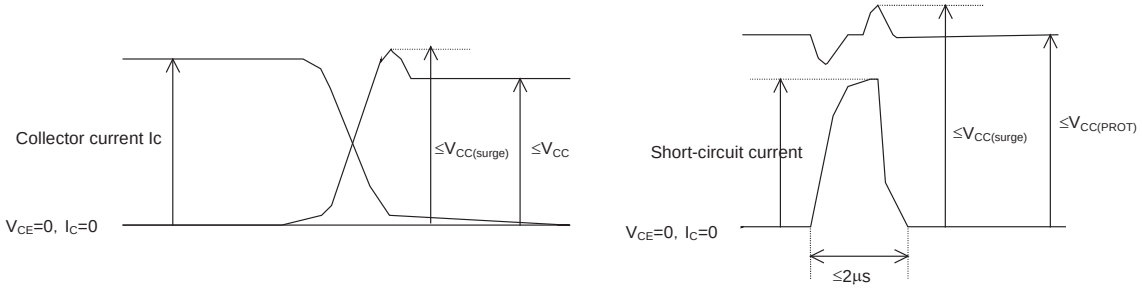


Figure 4-25 SOA for Switching and Short-circuit

In Case of switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT . By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting from $V_{CC(surge)}$ the surge voltage (50V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor is V_{CC}, that is 450V.

In Case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT . By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting from $V_{CC(surge)}$ the surge voltage (100V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor is V_{CC}, that is, 400V.

4.5.5 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happens on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.4-26 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj).

(The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

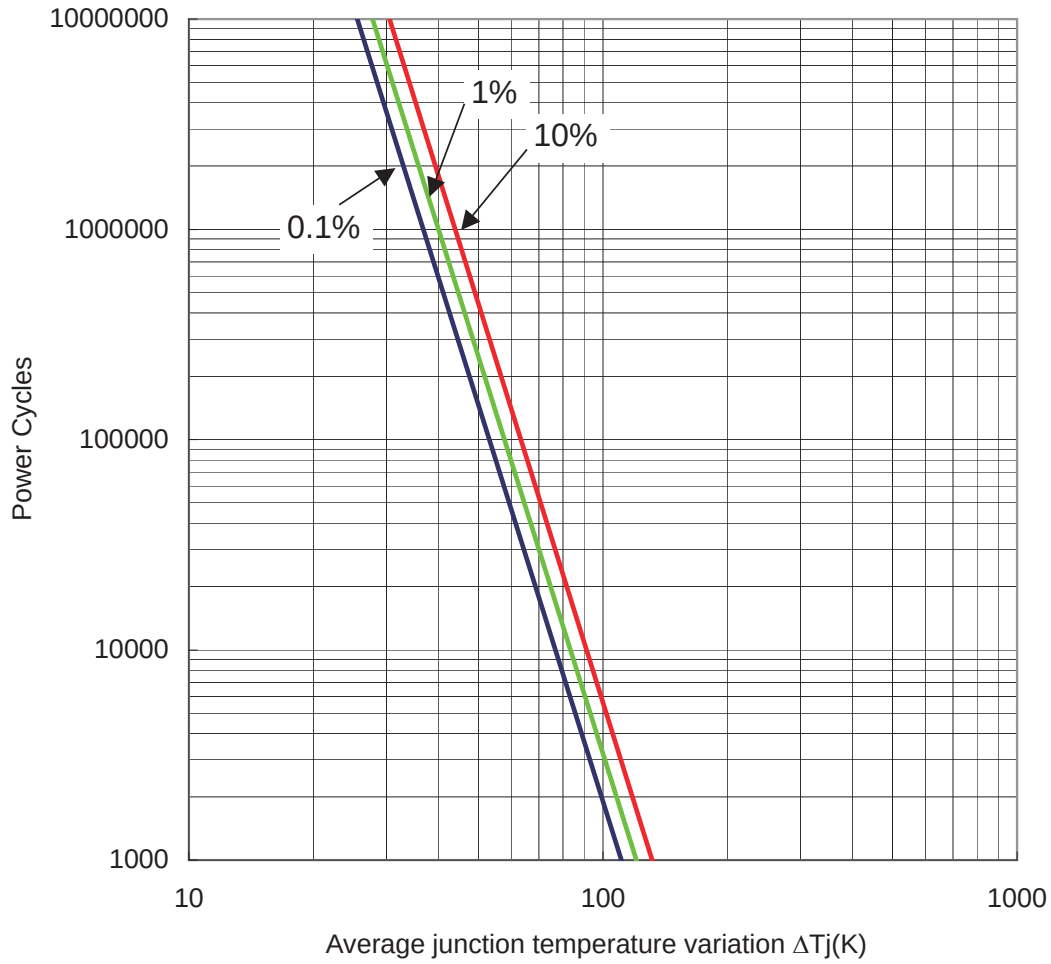


Figure 4-26. Power cycle curve

4.6 Fault Output Circuit

Table 20. Maximum Ratings

Item	Symbol	Condition	Ratings	Unit
Fault output supply voltage	V_{Fo}	Applied between Fo-V_{NC}	-0.5~V_D+0.5	V
Fault output current	I_{Fo}	Sink current of Fo terminal	1	mA

Table 21. Electric Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V, Fo=10kΩ,5V pulled-up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V, I_{Fo}=1mA	-	-	0.95	V

Because Fo terminal is an open drain type, it should be pulled up to 5V level via a pull-up resistor. The resistor has to satisfy the above specifications.

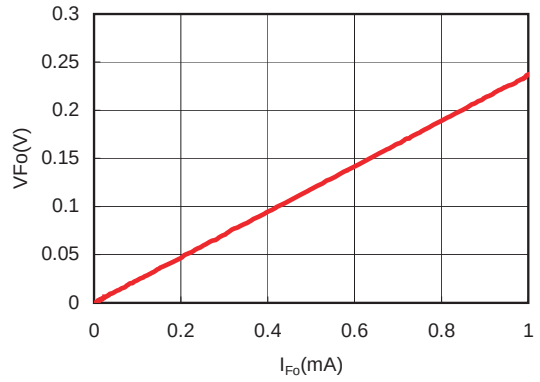


Figure 4-27 Voltage-current characteristics of Fo terminal (V_D=15V,Tj=25°C,typical data)

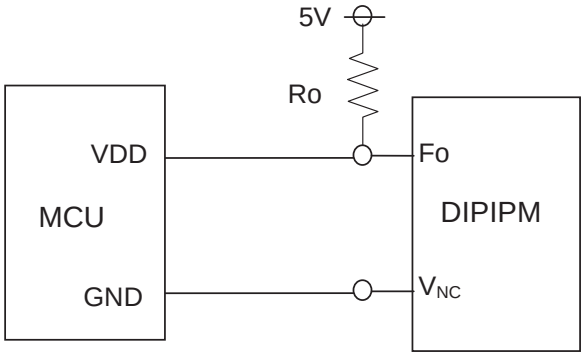


Figure 4-28 Fo terminal wiring

4.7 Guidelines for Control Supply

4.7.1 Timing Charts of Under-Voltage Protection

(1)Under-Voltage Protection (N-side, V_D)

a1. Control supply voltage rising . After the voltage level reaches UV_{Dr}, the circuits start to operate when next input applied.
a2. Normal operation : IGBT ON and carrying current
a3. Under voltage trip (UV_{Dt})
a4. IGBT turns OFF inspite of control input condition.
a5. Fo keeps output during the UV period, however, Fo pulse is not less than the fixed width for very short UV interval.
a6. Under voltage reset (UV_{Dr})
a7. Normal operation : IGBT ON and carrying current

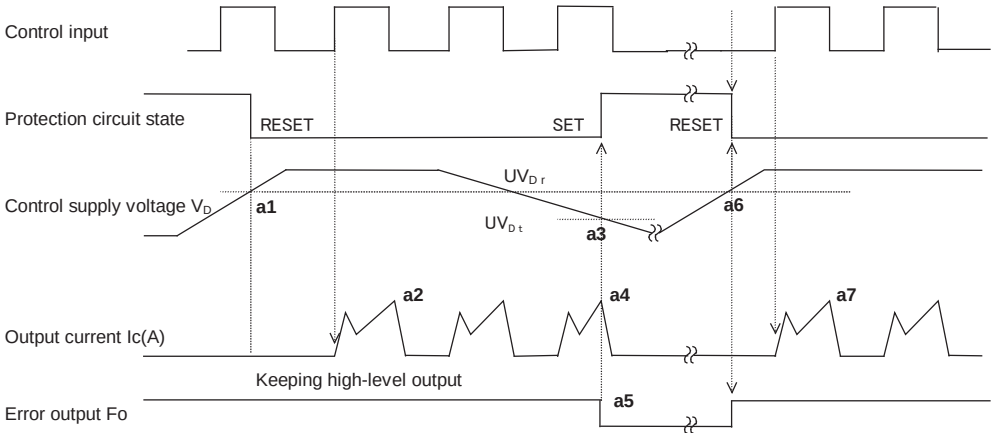


Figure 4-29 Timing Chart for N-side UV Operation

Note: All three-phase N-side IGBTs will be interrupted concurrently if N-side UV happened.

(2)Under-Voltage Protection (P-side, V_{DB})

(a) The case of Large DIPIPM (PS2186X-P)

a1. Control supply voltage rising. After the voltage reaches UV_{DBr}, the circuits start to operate soon.
a2. Normal operation : IGBT ON and carrying current
a3. Under voltage trip (UV_{DBt})
a4. IGBT OFF inspite of control input signal level, but there is no Fo signal output.
a5. Under voltage reset (UV_{DBr})
a6. Normal operation : IGBT ON and carrying current

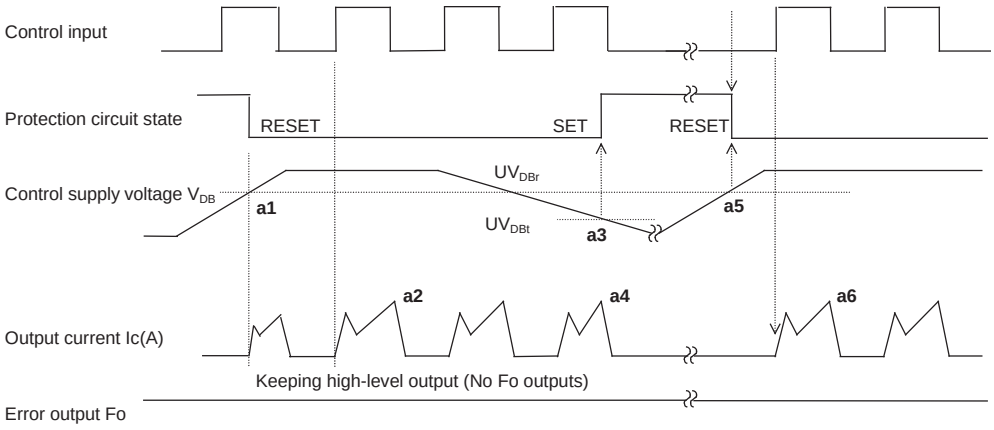


Figure 4-30 Timing Chart for P-side UV Operation(PS2186X-P)

Note: Only the IGBT of the phase with P-side UV failure will be interrupted; other IGBTs will not be stopped.

(b) The case of Mini DIPIPM (PS2156X-P)

a1. Control supply voltage rising. After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied.
a2. Normal operation : IGBT ON and carrying current
a3. Under voltage trip (UV_{DBt})
a4. IGBT OFF inspite of control input signal level, but there is no Fo signal output.
a5. Under voltage reset (UV_{DBr})
a6. Normal operation : IGBT ON and carrying current

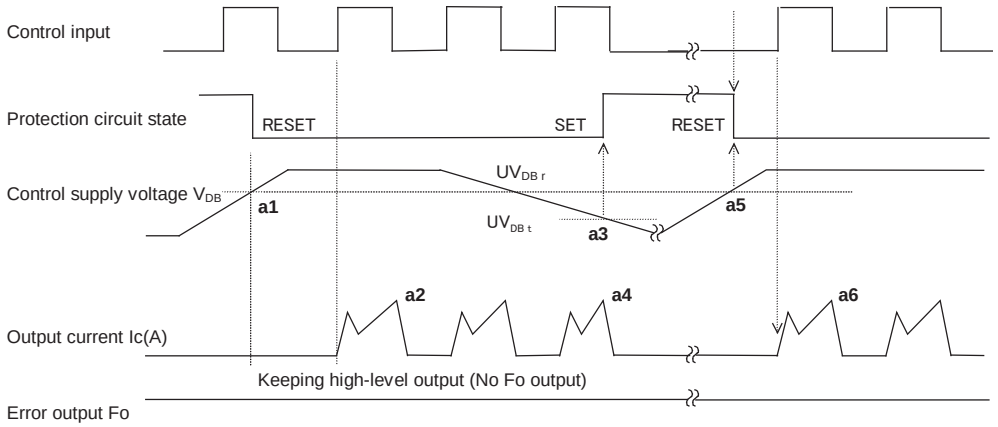


Figure 4-31 Timing Chart for P-side UV Operation(PS2156X-P)

Note: Only the IGBT of the phase with P-side UV failure will be interrupted; other IGBTs will not be stopped.

4.7.2 Other Guidelines

Table 22 describes DIPIPM state corresponding to various control supply. The ripple included control voltage should meet the specification.

Table 22. DIPIPM state corresponding to control supply voltage

Range of control supply voltage (V_D, V_{DB})	State
0~4.0	It is almost the same as no power supply. Control supply under-voltage protection will not operate and no Fo signal will be asserted. Basically IGBT doesn't turn on because supply voltage is under threshold voltage (Vth). But external noise may cause DIPIPM malfunction (turns ON). Please start up DC-link voltage after control power supply start up.
4.0~12.5	Even if control input signals are applied, IGBT does not work. Supply under-voltage protection starts operation and outputs Fo signals.
12.5~13.5	Switching operation works. However, this value is below the recommended one, $V_{CE(sat)}$ and switching time will be out of the specified values, it may increase collector dissipation and junction temperature.
13.5~16.5(13.5~18.5for V_{DB})	Recommended values.
16.5~20(18.5~20for V_{DB})	Switching operation works. This range, however, is over the recommended value, thus, too fast switching speed might cause the chips to be damaged.
20.0~	The control circuit will be destroyed.

Note: UV fault signals are asserted only for V_D supply.

(1) Specifications for Ripple Noise

If high frequency noise is imposed on the control IC supply line, it may cause IC a malfunction and assert an error fault signal. To avoid such malfunction, the supply circuit should be designed such that the noise fluctuation is limited within ±1V/μs, and the ripple voltage is less than 2V.

Specification: dV/dt≤±1V/μs, Vripple≤2Vp-p

(2) UV filter

When control supply voltage falls down, IGBT will turn OFF ignoring the input signal. It will take about 10μsec to keep on interrupting the gate after receiving an set signal because there is a built-in 10μsec filter (typ.).

4.8 Power Loss and Thermal Dissipation Design

4.8.1 Power Loss Calculation

Simple expressions for calculating average power loss

◆ Scope

In preparation for applying the DIPIPM in VVVF inverter, it is possible to calculate overall loss in normal operation in order to select (or compare) power modules. This calculation, however, cannot be applied to thermal design under extreme conditions.

◆ Assumptions

(1) Sine waveform current output PWM control VVVF inverter
(2) PWM signals generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies within the range: $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100)
(4) Output current is given by Icp·sinx and it does not have ripple.
(5) Load power factor for output current is cos θ, while ideal inductive load is assumed for switching.
(6) IGBT saturation voltage $V_{CE(sat)}$ is in proportion to the collector current Ic.
(7) Forward voltage drop of free-wheeling diode V_{EC} is in proportion to the forward current I_{EC}.
(8) Switching losses $P_{SW(on)}$ and $P_{SW(off)}$ are in proportion to the collector current.
(9) Reverse current of free-wheeling diode is constant regardless of the forward current I_{EC}.

◆ Expressions

(1) Static loss of IGBT

$$Icp \times Vce(sat)(@\ Icp) \times (\frac{1}{8} + \frac{D}{3\pi}\cos\theta)$$

(2) Dynamic loss of IGBT

$$(Psw(on) + Psw(off)) \times\ fc \times \frac{1}{\pi}$$

(3) Static loss of free-wheeling diode

$$Iecp \times Vec(@\ Ifp = Icp) \times (\frac{1}{8} - \frac{D}{3\pi}\cos\theta)$$

(4) Dynamic loss of free-wheeling diode

$$\frac{1}{8} \times (Irr \times Vcc \times trr \times\ fc)$$

◆ Expressions Derivation

For the time t, duty ratio of PWM signals is represented by $\frac{1 + D \times \sin t}{2}$ This corresponds to the change of output voltage. Thus, with the power factor cosθ indicating the relationship between output current and voltage, the expressions to calculate output current and PWM duty will be derived as follows:

$$Output\ \ current = Icp \times \sin x$$

$$PWM\ \text{Duty} = \frac{1 + D \times \sin(t + \theta)}{2}$$

Thus, $V_{CE(sat)}$ and V_{EC} at the phase x for linear approximation is calculated by:

$$Vce(sat) = Vce(sat)(@\ Icp) \times \sin x$$

$$Vec = Vec(@\ Iecp = Icp)(-1) \times \sin x$$

Thus, the static loss of transistor is calculated by:

$$\frac{1}{2\pi}\int_0^{\pi}(Icp\times\sin x)\times Vce(sat)(@\,Icp)\times\frac{1+D\sin(x+\theta)}{2}\cdot dx$$

$$= Icp\times Vce(sat)(@\,Icp)\times\frac{1}{2\pi}\int_0^{\pi}(Icp\times\sin^2 x)\times\frac{1+D\sin(x+\theta)}{2}\cdot dx$$

$$= Icp\times Vce(sat)(@\,Icp)\times\frac{1}{8}+\frac{D}{3\pi}\cos\theta$$

Similarly, the static loss of free-wheeling diode is calculated by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi}((-1)\times Icp\times\sin x)\times((-1)\times Vec(@\,Icp)\times\sin x)\times\frac{1+D\sin(x+\theta)}{2}\cdot dx$$

$$= Icp\times Vec(@\,Icp)\times(\frac{1}{8}-\frac{D}{3\pi}\cos\theta)$$

On the other hand, the dynamic loss of transistor, which does not depend on PWM duty, is calculated by:

$$\frac{1}{2\pi}\int_0^{\pi}(Psw(on)(@\,Icp)+Psw(off)(@\,Icp))\times\sin x\times fc\cdot dx$$

$$= (Psw(on)(@\,Icp)+Psw(off)(@\,Icp))\times fc\times\frac{1}{\pi}$$

If dynamic loss of free-wheeling diode is idealized as shown in Figure 4-32, it is calculated by:

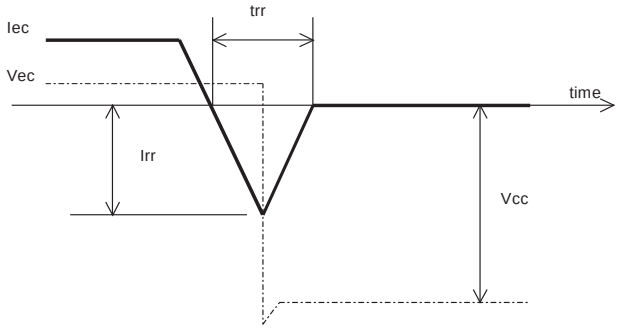


Figure 4-32. FWDi Dynamic Loss

$$Psw = \frac{Irr\times Vcc\times trr}{4}(const.)$$

Recovery occurs in the middle of output current period. Thus, the dynamic loss is calculated by:

$$\frac{Irr\times Vcc\times trr}{4}\times fc\times\frac{1}{2}$$

$$\frac{1}{8}\times(Irr\times Vcc\times trr\times fc)$$

◆ Guidelines for applying the power loss expressions in inverter designs

- Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of : PWM duty; output current; the values of $V_{CE(sat)}$, V_{EC}, Psw corresponding to the output current.
- PWM duty depends on the way of generating signals.
- The relationship between output current waveform or output current and PWM duty changes depending on the way of generating signals, load, and other various factors. Thus, calculation should be performed based on actual waveforms.
- $V_{CE(sat)}$ and Psw(on, off) should be the value at Tj=125°C.

4.8.2 Temperature Rise Considerations and Calculation Example

The result of loss calculation using the typical characteristics is shown in Figure 4-33 as “Effective current versus carrier frequency characteristics”.

Conditions: V_{CC}=300V, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., Switching loss=Typ., Tj=125°C, Tf=100°C,Rth(j-f)=Max., P.F=0.8, 3-phase PWM modulation, 60Hz sine waveform output

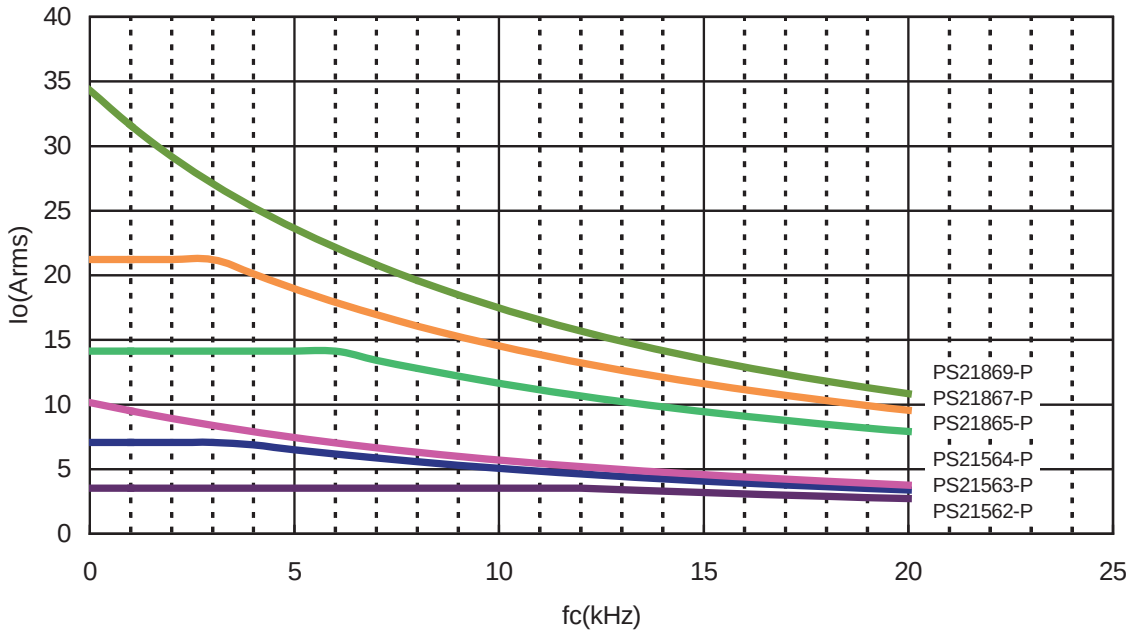


Figure 4-33 Allowable effective current-carrier frequency characteristics

Fig.4-33 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tf=100°C. Tj=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The allowable motor current can also be obtained from the free power loss simulation software provided by Mitsubishi electric on its web site (URL: http://www.mitsubishichips.com/).

4.9 Noise Withstand Capability

4.9.1 Evaluation Circuit

In noise test of DIPIPM, ±2.0kV or much high withstand capability has been confirmed under the conditions given in Figure 4-34 However, noise withstand capability greatly depends on the test conditions, the wiring patterns of control substrate, parts layout, and other factors; therefore a confirmation on prototype is necessary.

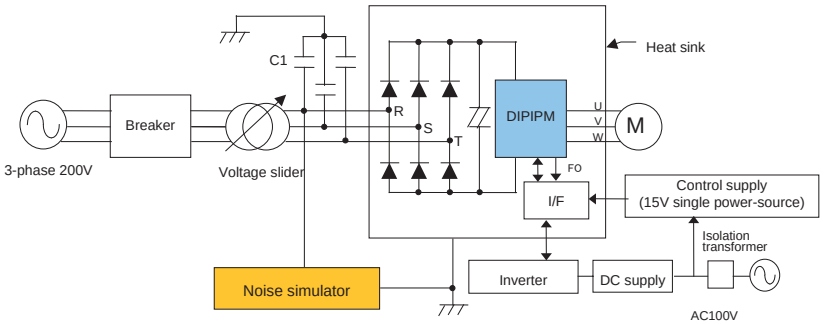


Figure 4-34 Noise test circuit

Note:

C1: AC line common-mode filter 4700pF
PWM signals are inputted from microcomputer both directly and through opto-coupler
15V single power-source drive
Test is performed for both IM and DCBLM motors

Test conditions

V_{CC}=300V, V_D=15V, Ta=25°C, no load
Scheme to apply noise : From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05~1μs, input in random.

4.9.2 Countermeasures and Precautions

DIPIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current.

For malfunction caused by external noise, please consider the following countermeasures:

(1) Improving power supply filtering (close to DIPIPM terminals)
(2) Lowering impedance of input parts (reducing pull-up resistance)
(3) Connecting filter between input parts and GND (bypassing noise)

4.9.3.Surge Withstand Capability

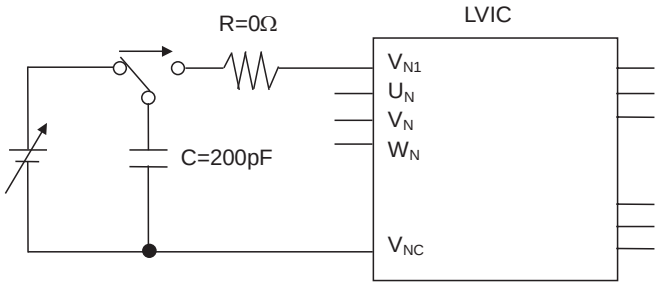


Figure 4-35 Surge Test circuit(V_{N1}terminal)

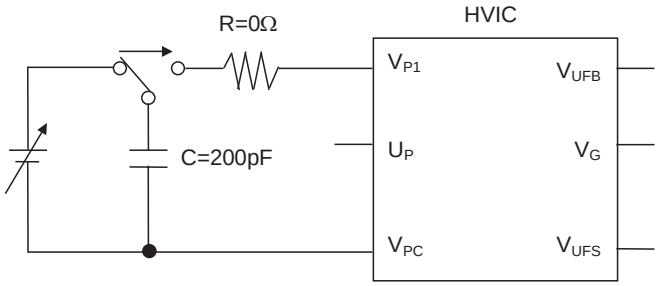
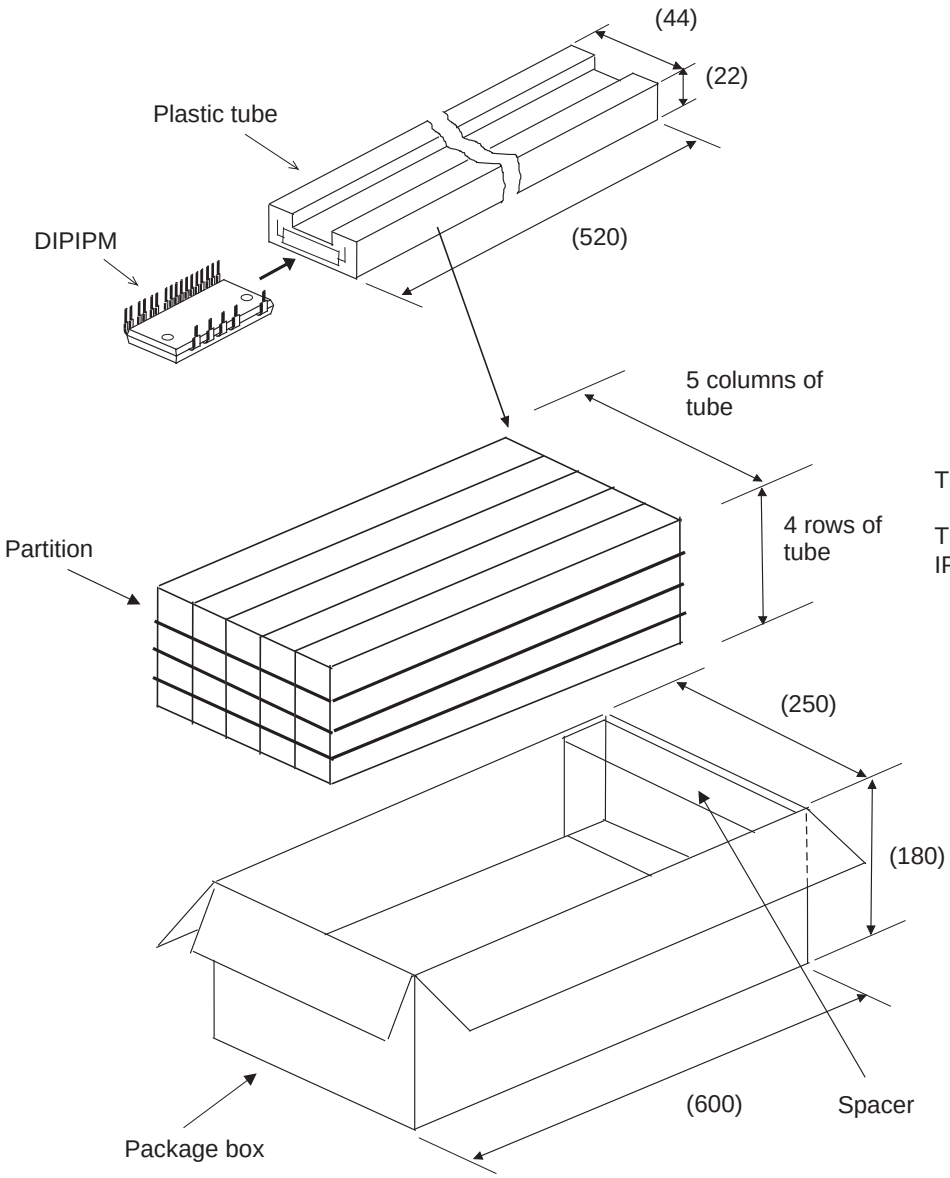


Figure 4-36 Surge Test circuit(V_{P1}terminal)

For surge test of DIPIPM, ±200V or more withstand capability has been confirmed under the conditions given in Figure 4-35,36.

CHAPTER 5 ADDITIONAL GUIDELINES

5.1 Packaging Specification



Quantity:

6 pcs per 1 tube

Total amount in one box (max):

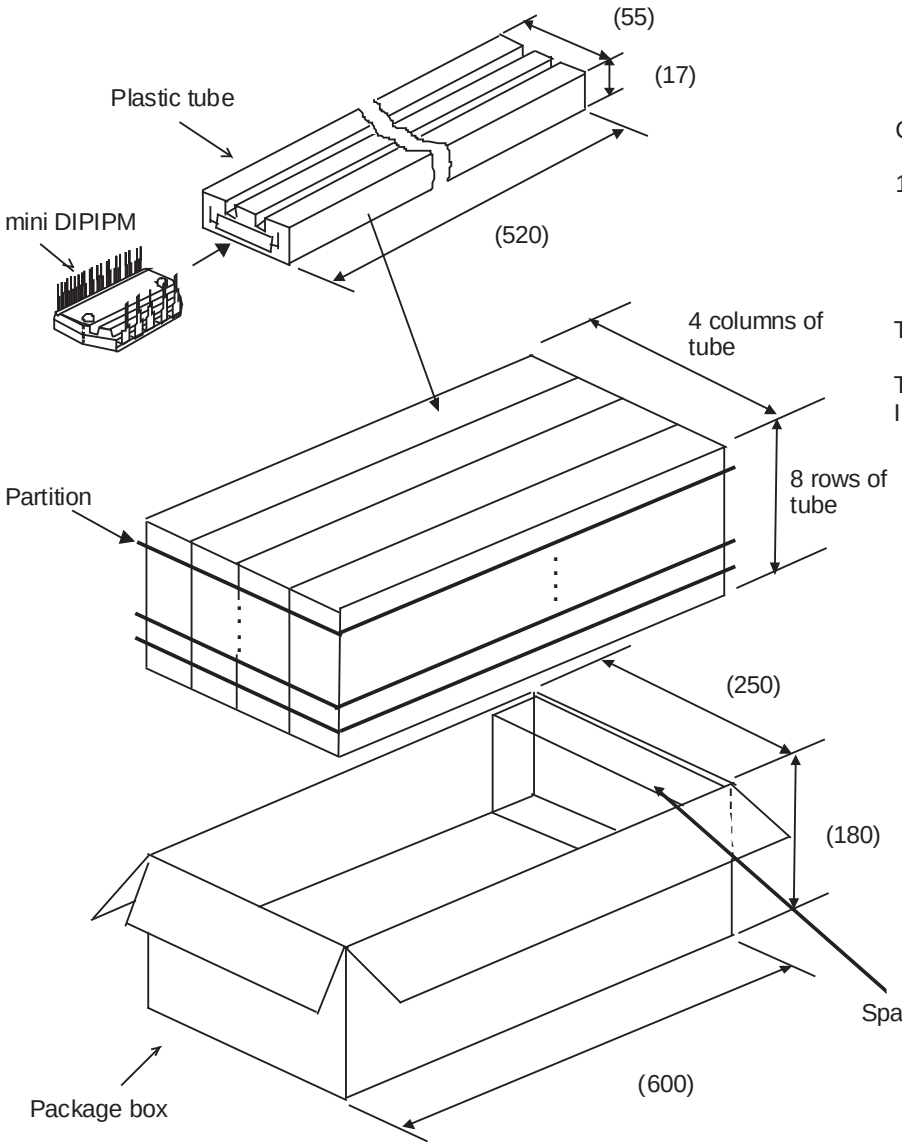
Tube Quantity: 5 × 4=20
IPM Quantity: 20 × 6=120

Weight (max):

≤65g per 1pcs of DIPIPM
≤490g per 1 tube
≤11kg per 1 box

Figure 5-1 DIPIPM Packaging Specification for Large DIP(PS2186X-P)

CHAPTER 5 ADDITIONAL GUIDELINES



Quantity:

10 pcs per 1 tube

Total amount in one box (max):

Tube Quantity: 4 × 8=32
IPM Quantity: 32 × 10=320

Weight (max):

≤20g per 1pcs of DIPIPM
≤310g per 1 tube
≤12kg per 1 box

Figure 5-2 DIPIPM Packaging Specification for Mini DIP(PS2156X-P)

5.2 Attention for Handling

Transportation	·Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ·Throwing or dropping the packaging boxes might cause the devices to be damaged. ·Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	·We recommend room temperature and humidity in the ranges 5~35°C and 45~75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	·When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	·Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Disposal	·The epoxy resin and the case materials are made of approved products in the UL standard 94-V0, still they are incombustible.
Static electricity	·Exclusive ICs of MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1) Notice of breakdown by static electricity Excessively high voltage (over the Max. rated input terminal voltage) resulting from the static electricity of human bodies and packaging materials, might cause the modules to be damaged if applied on the control terminals. For countermeasures against static breakdown, it is important to control the static electricity as much as possible and when it exists, discharge it as soon as possible. * Do not use containers which are easy to be electro-statically charged during transportation. * Be sure to short the control terminals with carbon cloth, etc. just before using the module. Also, do not touch between the terminals with bare hands. * During assembly (after removing the carbon cloth, etc.), earth machines used and human bodies. We suggest putting a conductive mat on the surface of the operating table and the surrounding floor. * When the terminals on the printed circuit board with mounted modules are open, the modules might be damaged by static electricity on the printed circuit board. * When using a soldering iron, earth its tip. (2) Notice when the control terminals are open * When the control terminals are open, do not apply voltage between the collector and emitter. * Short the terminals before taking a module off.

Keep safety first in your circuit designs!

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