# HVIGBT Module Application Note

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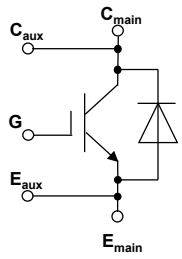
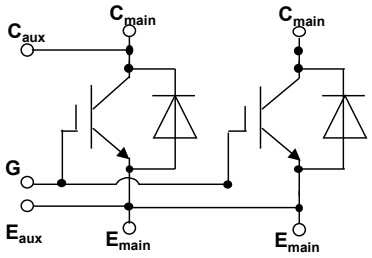
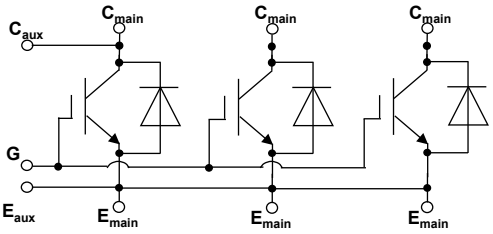
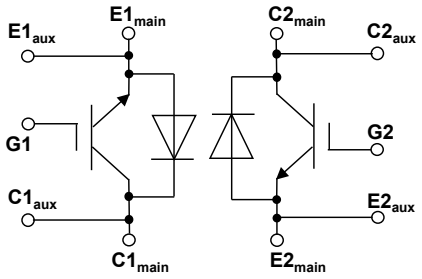
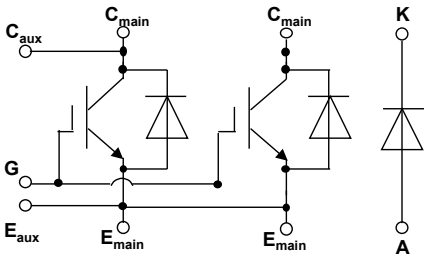
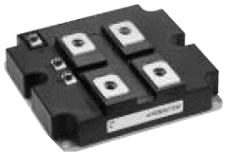
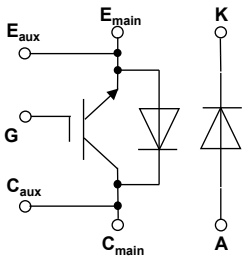
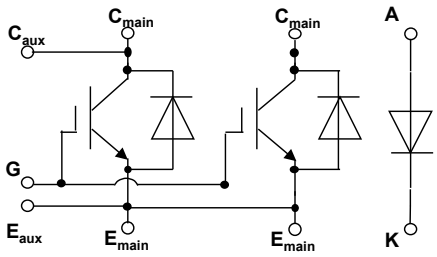
# 1. Circuit Topologies

Mitsubishi HVIGBT modules circuit topologies are grouped into three types: Single type (H), Dual type (D), Chopper type (E2 or E4). The following table shows the used topologies in detail for each package outline.

| Type | Outline | Circuit topology | Features |
|---|---|---|---|
| Single (H) |  |  | Each module contains one IGBT and an anti-parallel free-wheel diode.<br>The package size and number of main terminals depends on the module`s current rating.<br>For higher current ratings, modules usually have two or three segments in parallel. In this case, the main collector terminals are not internally connected with each other. However, the emitter terminals are internally connected via the auxiliary emitter pattern. |
| |  |  | |
| |  |  | |
| Dual (D) |  |  | Each module contains two IGBTs with respective anti-parallel free-wheel diodes.<br>The two IGBTs are not connected electrically inside the module.<br>By connecting the main terminals outside the module, a half-bridge configuration is possible. This external connection can be done between E2 and C1 or between E1 and C2. |

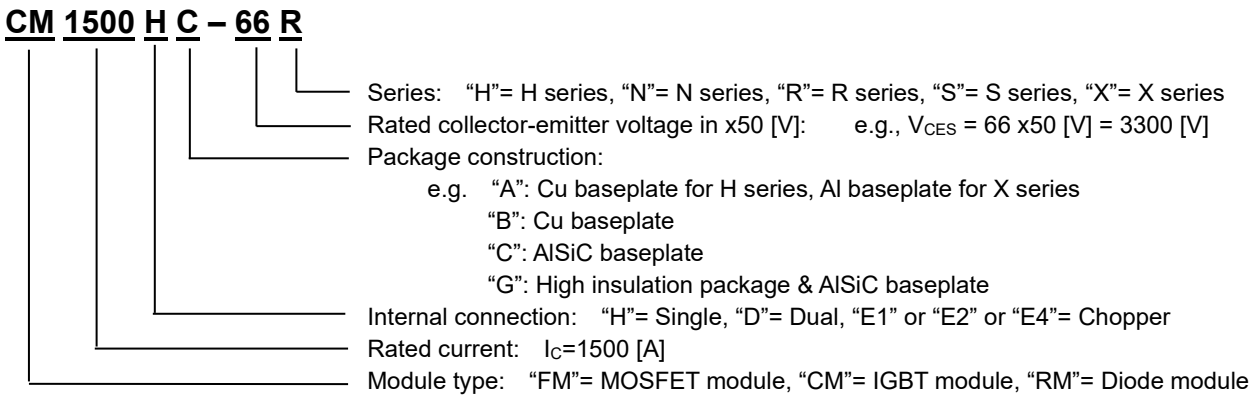
# - Circuit Topologies -

| Type | Outline | Circuit topology | Features |
|---|---|---|---|
| Chopper (E2) |  |   | Each module contains one IGBT and an anti-parallel free-wheel diode, as well as a chopper diode.<br>The IGBT and chopper diode are not connected electrically inside the module.<br>Two chopper types are available:<br>In the E2 type, the chopper diode has the same terminal-layout direction as the IGBT`s anti-parallel free-wheel diode.<br>In the E4 type the chopper diode has the opposite terminal-layout direction as the IGBT`s anti-parallel free-wheel diode. |
| Chopper (E4) |  |   | |
| |  |   | |

## 2. Numbering System

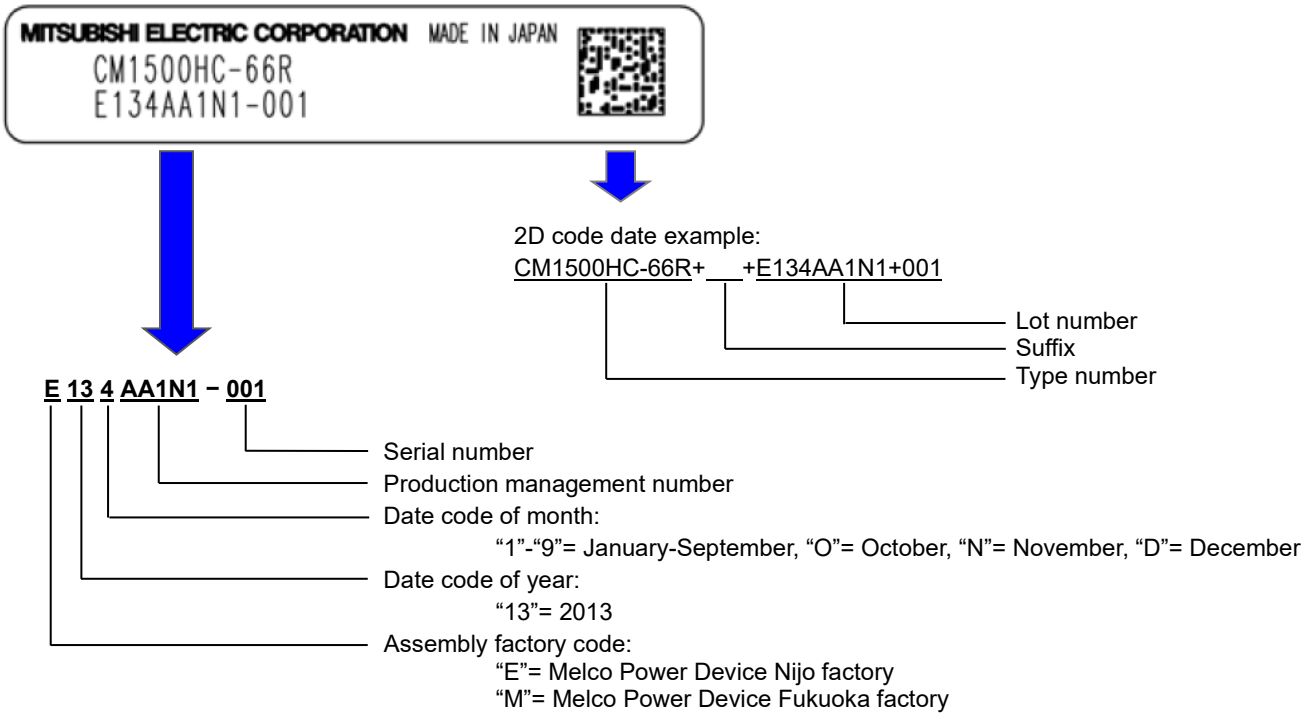
Each module has a type number. An example of type number is shown below.

Example of type number:




Each module has a label. The label contains the following information (See below example).

Type number: CM1500HC-66R
2D code: Data Matrix (ECC200)
Lot number : E134AA1N1-001
Manufacturer: MITSUBISHI ELECTRIC CORPORATION
Country of origin: JAPAN



# 3. HVIGBT Datasheet Ratings

## 3.1 Maximum Ratings

The ratings shown below are the most important for IGBT lifetime consideration. A maximum rating establishes either a limiting capability or limiting condition (maximum or minimum) for the power module.
They set the boundaries for the power module, outside of which the lifetime will be severely reduced.

Table 3-1. Maximum ratings on the datasheet for CM1500HC-66R

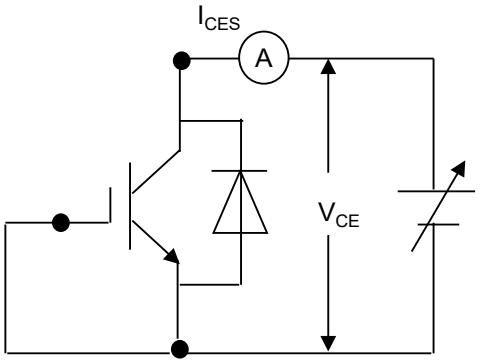
**MAXIMUM RATINGS**

| Symbol | Item | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage | $V_{GE}$ = 0V, $T_j$ = -40…+150°C | 3300 | V |
| | | $V_{GE}$ = 0V, $T_j$ = −50°C | 3200 | |
| $V_{GES}$ | Gate-emitter voltage | $V_{CE}$ = 0V, $T_j$ = 25°C | ± 20 | V |
| $I_C$ | Collector current | DC, $T_c$ = 95°C | 1500 | A |
| $I_{CRM}$ | | Pulse (Note 1) | 3000 | A |
| $I_E$ | Emitter current (Note 2) | DC | 1500 | A |
| $I_{ERM}$ | | Pulse (Note 1) | 3000 | A |
| $P_{tot}$ | Maximum power dissipation (Note 3) | $T_c$ = 25°C, IGBT part | 15600 | W |
| $V_{iso}$ | Isolation voltage | RMS, sinusoidal, f = 60Hz, t = 1 min. | 6000 | V |
| $V_e$ | Partial discharge extinction voltage | RMS, sinusoidal, f = 60Hz, $Q_{PD}$ ≤ 10 pC | 2600 | V |
| $T_j$ | Junction temperature | | −50 ~ +150 | °C |
| $T_{jop}$ | Operating junction temperature | | −50 ~ +150 | °C |
| $T_{stg}$ | Storage temperature | | −55 ~ +150 | °C |
| $t_{psc}$ | Short circuit pulse width | $V_{CC}$ = 2500V, $V_{CE}$ ≤ $V_{CES}$, $V_{GE}$ =15V, $T_j$ =150°C | 10 | μs |

### ■ $V_{CES}$ : collector-emitter voltage

Definition: Maximum collector-emitter voltage with gate-emitter shorted ($V_{GE}$ = 0)
Parameters: $V_{GE}$ and $T_j$
Confirmation test conditions: see Fig. 1 The gate-emitter voltage is set to short circuit ($V_{GE}$=0 V).

The collector-emitter voltage is set to the specified maximum value.
The collector cutoff current, $I_{CES}$, shall not exceed the specified maximum value.




Shorted between gate and emitter

Fig. 3-1 $V_{CES}$ test circuit

■ **$V_{GES}$ : Gate-emitter voltage**

Definition: Maximum gate-emitter voltage with collector-emitter shorted ($V_{CE}$=0V)
Parameters: $V_{CE}$ and $T_j$
Confirmation test conditions: see Fig .3-2. The gate-emitter voltage $V_{GE}$ is set to the specified maximum value.

The gate leakage current, $I_{GES}$, shall not exceed the specified maximum value.

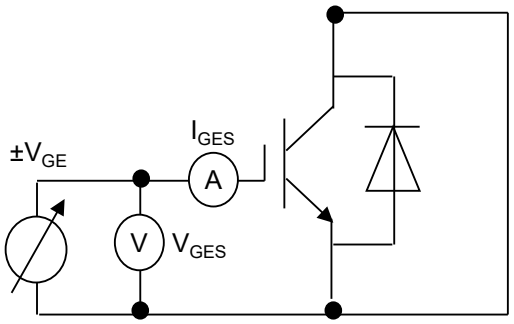



Fig. 3-2 $V_{GES}$ test circuit

■ **$I_C$ : Collector current (Continuous collector direct current)**

Definition: Maximum allowable value of DC collector current.
Parameter: $T_c$

■ **$I_{CRM}$ : Collector current (Repetitive peak current)**

Definition: Maximum allowable value of pulse collector current.
Parameters: $T_j$
Notice: Pulse width and repetition rate should be such that junction temperature $T_j$ does not exceed $T_{jop}$ rating.

■ **$I_E$ : Emitter current (Free-wheel diode forward current)**

Definition: Maximum allowable value of free-wheel diode DC current.
Parameters: $T_c$

■ **$I_{ERM}$ : Emitter current (Repetitive peak free-wheel diode current)**

Definition: Maximum allowable value of free-wheel diode pulse current.
Parameters: $T_j$
Notice: Pulse width and repetition rate should be such that junction temperature $T_j$ does not exceed $T_{jop}$ rating.

■ **$P_{tot}$ : Maximum power dissipation of IGBT part**

Definition: Maximum allowable value of power dissipation in IGBT part at $T_C$=25°C.
$P_{tot} = (T_{jmax} - T_C) / R_{th(j-c)Q}$
Parameters: $T_{jmax}$, $T_c$, $R_{th(j-c)Q}$

## ■ $V_{iso}$ : Isolation voltage

Definition: Maximum allowable AC voltage that can be applied between electrical module terminals (all power and signal terminals shorted together) and module baseplate for 1minute.
Parameters: $T_j$ , f, Time

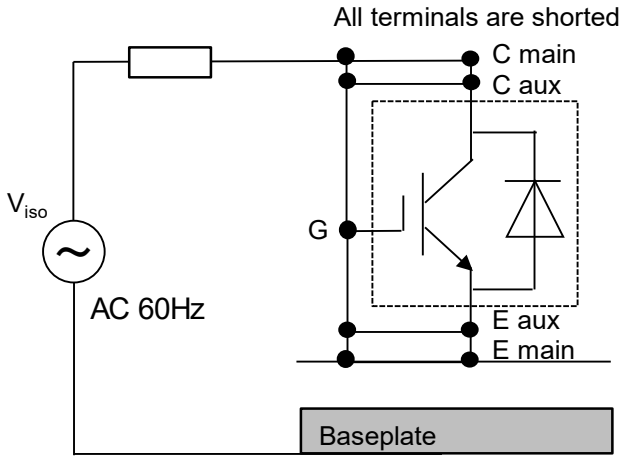



Fig. 3-3 Isolation voltage test circuit

## ■ $V_e$ : Partial discharge extinction voltage

Definition: Value of isolation voltage when $Q_{PD}$ of partial discharge is below specified limit of 10pC (see Fig.3-5). Test timing and test conditions are specified in IEC60270(Edtion3.1).

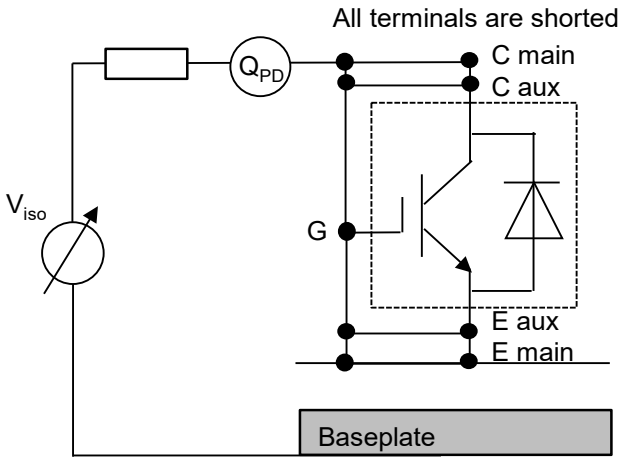



Fig. 3-4 Partial discharge test circuit

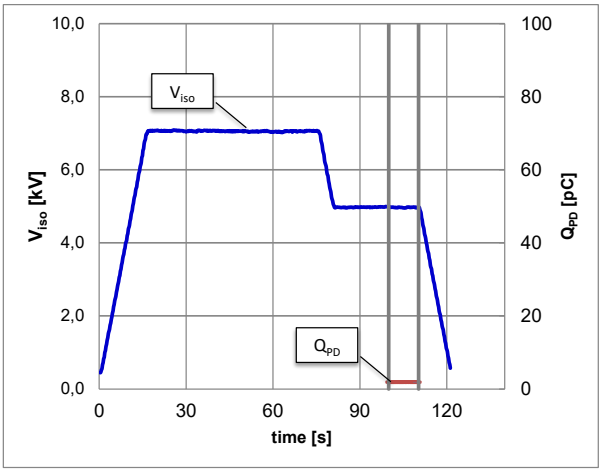



Fig. 3-5 Partial discharge test timing chart

### ■ $T_j$ : Junction temperature

Definition: IGBT and diode chip temperature in the junction region that can be calculated by using the thermal resistance between junction and case ($R_{th(j-c)}$). That is, the virtual junction temperature, because we cannot observe the exact junction temperature.

$T_j = T_C + R_{th(j-c)} \times P_C$

Also the junction temperature means all IGBT or diode chips temperatures' average. The junction temperature
$T_j$ should not exceed the $T_{jmax}$ rated value in on-state.

### ■ $T_{jop}$ : Operating junction temperature

Definition: Range of allowable operating junction temperature. Operating temperature means junction temperature during IGBT module operation. Junction temperature $T_j$ must not exceed the $T_{jop(max)}$.

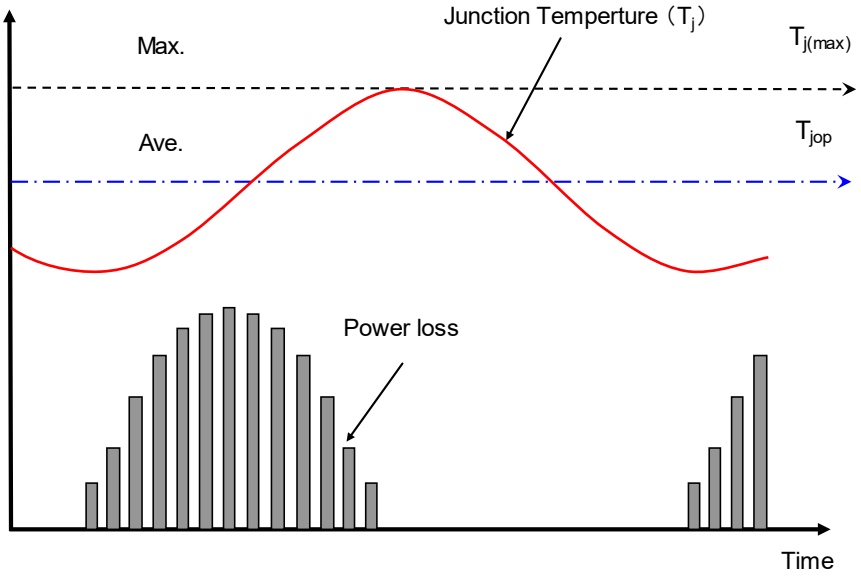



Fig. 3-6 Definitions of $T_j$ and $T_{jop}$

### ■ $T_{stg}$ : Storage temperature

Definition: Range of allowable ambient temperature without applied voltage or current.

## ■ $t_{psc}$ : Short circuit pulse width

Definition: Maximum allowable value of short circuit pulse width.
This width is defined between rising (50% $V_{GE}$) and falling edge (50% of $V_{GE}$) under specified conditions, shown in Fig.3-8.

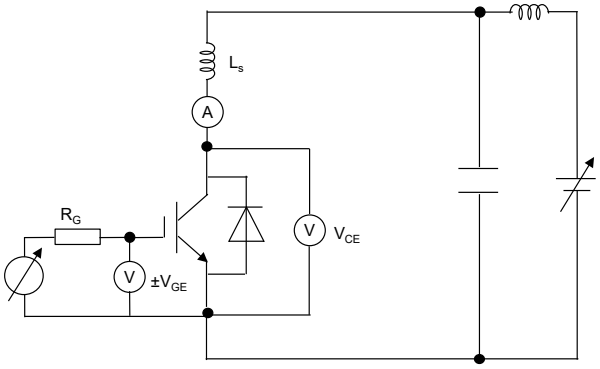



Fig. 3-7 Short circuit test diagram

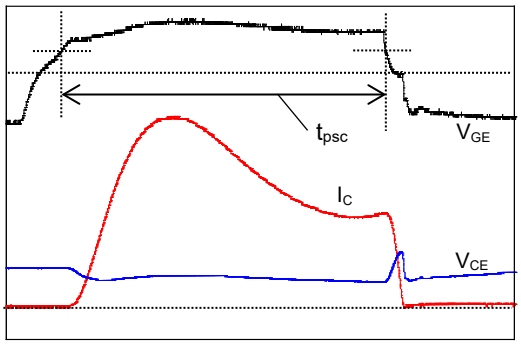



Fig. 3-8 Short circuit test waveform

## 3.2 Electrical Characteristics

Table 3-2. Electrical characteristics on the datasheet for the CM1500HC-66R

**ELECTRICAL CHARACTERISTICS**

| Symbol | Item | Conditions | | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current | $V_{CE}$ = $V_{CES}$, $V_{GE}$ = 0V | $T_j$ = 25°C | — | — | 6.0 | mA |
| | | | $T_j$ = 125°C | — | 6.0 | — | |
| | | | $T_j$ = 150°C | — | 36.0 | — | |
| $V_{GE(th)}$ | Gate-emitter threshold voltage | $V_{CE}$ = 10 V, $I_C$ = 150 mA, $T_j$ = 25°C | | 5.7 | 6.2 | 6.7 | V |
| $I_{GES}$ | Gate leakage current | $V_{GE}$ = $V_{GES}$, $V_{CE}$ = 0V, $T_j$ = 25°C | | −0.5 | — | 0.5 | µA |
| $C_{ies}$ | Input capacitance | $V_{CE}$ = 10 V, $V_{GE}$ = 0 V, f = 100 kHz, $T_j$ = 25°C | | — | 210.0 | — | nF |
| $C_{oes}$ | Output capacitance | | | — | 13.0 | — | nF |
| $C_{res}$ | Reverse transfer capacitance | | | — | 6.0 | — | nF |
| $Q_G$ | Total gate charge | $V_{CC}$ = 1800V, $I_C$ = 1500A, $V_{GE}$ = ±15V | | — | 16.0 | — | µC |
| $V_{CEsat}$ | Collector-emitter saturation voltage | $I_C$ = 1500 A (Note 4), $V_{GE}$ = 15 V | $T_j$ = 25°C | — | 2.45 | — | V |
| | | | $T_j$ = 125°C | — | 3.10 | 3.70 | |
| | | | $T_j$ = 150°C | — | 3.25 | — | |
| $t_{d(on)}$ | Turn-on delay time | $V_{CC}$ = 1800 V, $I_C$ = 1500 A, $V_{GE}$ = ±15 V, $R_{G(on)}$ = 1.6 Ω, $L_s$ = 100 nH, Inductive load | $T_j$ = 25°C | — | 1.00 | — | µs |
| | | | $T_j$ = 125°C | — | 0.95 | 1.25 | |
| | | | $T_j$ = 150°C | — | 0.95 | 1.25 | |
| $t_r$ | Turn-on rise time | | $T_j$ = 25°C | — | 0.28 | — | µs |
| | | | $T_j$ = 125°C | — | 0.30 | 0.50 | |
| | | | $T_j$ = 150°C | — | 0.30 | 0.50 | |
| $E_{on(10\%)}$ | Turn-on switching energy (Note 5) | | $T_j$ = 25°C | — | 2.10 | — | J |
| | | | $T_j$ = 125°C | — | 2.75 | — | |
| | | | $T_j$ = 150°C | — | 3.00 | — | |
| $E_{on}$ | Turn-on switching energy (Note 6) | | $T_j$ = 25°C | — | 2.20 | — | J |
| | | | $T_j$ = 125°C | — | 2.90 | — | |
| | | | $T_j$ = 150°C | — | 3.20 | — | |
| $t_{d(off)}$ | Turn-off delay time | $V_{CC}$ = 1800 V, $I_C$ = 1500 A, $V_{GE}$ = ±15 V, $R_{G(off)}$ = 5.6 Ω, $L_s$ = 100 nH, Inductive load | $T_j$ = 25°C | — | 2.70 | — | µs |
| | | | $T_j$ = 125°C | — | 2.80 | 3.30 | |
| | | | $T_j$ = 150°C | | 2.85 | 3.30 | |
| $t_f$ | Turn-off fall time | | $T_j$ = 25°C | — | 0.30 | — | µs |
| | | | $T_j$ = 125°C | — | 0.35 | 1.00 | |
| | | | $T_j$ = 150°C | — | 0.40 | 1.00 | |
| $E_{off(10\%)}$ | Turn-off switching energy (Note 5) | | $T_j$ = 25°C | — | 2.00 | — | J |
| | | | $T_j$ = 125°C | — | 2.45 | — | |
| | | | $T_j$ = 150°C | | 2.50 | — | |
| $E_{off}$ | Turn-off switching energy (Note 6) | | $T_j$ = 25°C | — | 2.20 | — | J |
| | | | $T_j$ = 125°C | — | 2.70 | — | |
| | | | $T_j$ = 150°C | — | 2.80 | — | |

| Symbol | Item | Conditions | | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{EC}$ | Emitter-collector voltage (Note 2) | $I_E$ = 1500 A (Note 4), $V_{GE}$ = 0 V | $T_j$ = 25°C | — | 2.15 | — | V |
| | | | $T_j$ = 125°C | — | 2.30 | 2.80 | |
| | | | $T_j$ = 150°C | — | 2.25 | — | |
| $t_{rr}$ | Reverse recovery time (Note 2) | $V_{CC}$ = 1800 V, $I_C$ = 1500 A, $V_{GE}$ = ±15 V, $R_{G(on)}$ = 1.6 Ω, $L_s$ = 100 nH, Inductive load | $T_j$ = 25°C | — | 0.50 | — | µs |
| | | | $T_j$ = 125°C | — | 0.70 | | |
| | | | $T_j$ = 150°C | — | 0.80 | — | |
| $I_{rr}$ | Reverse recovery current (Note 2) | | $T_j$ = 25°C | — | 1250 | — | A |
| | | | $T_j$ = 125°C | — | 1500 | — | |
| | | | $T_j$ = 150°C | — | 1550 | — | |
| $Q_{rr}$ | Reverse recovery charge (Note 2) | | $T_j$ = 25°C | — | 1050 | — | µC |
| | | | $T_j$ = 125°C | — | 1700 | | |
| | | | $T_j$ = 150°C | — | 2000 | — | |
| $E_{rec(10\%)}$ | Reverse recovery energy (Note 2) (Note 5) | | $T_j$ = 25°C | | 1.05 | — | J |
| | | | $T_j$ = 125°C | — | 1.75 | | |
| | | | $T_j$ = 150°C | — | 2.00 | — | |
| $E_{rec}$ | Reverse recovery energy (Note 2) (Note 6) | | $T_j$ = 25°C | | 1.20 | — | J |
| | | | $T_j$ = 125°C | — | 2.00 | | |
| | | | $T_j$ = 150°C | — | 2.30 | — | |

■ **$I_{CES}$ : Collector cutoff current**

Definition: Collector current in IGBT off-state when collector-emitter voltage is set to the specified maximum value $V_{CES}$ and the gate-emitter is shorted ($V_{GE}$=0V).
Confirmation test conditions: The gate-emitter voltage is set to short circuit ($V_{GE}$=0 V).
The collector-emitter voltage is set to the specified maximum value.

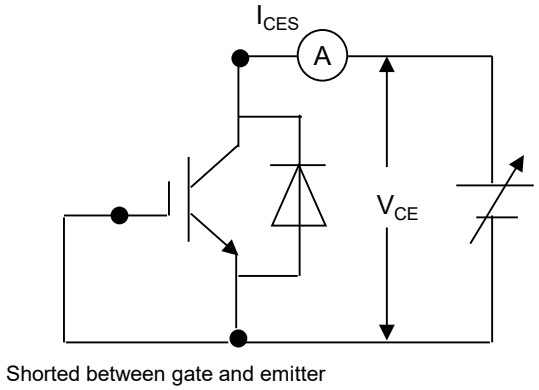



Fig. 3-9 $I_{CES}$ test circuit

■ **$V_{GE(th)}$ : Gate-emitter threshold voltage**

Definition: Gate-emitter voltage at $I_C$ = $10^{-4}$ × rated collector current and $V_{CE}$ = 10V.
Confirmation test conditions: $T_j$ = 25°C, $V_{CE}$ = 10V and $I_C$ = $10^{-4}$ × rating current

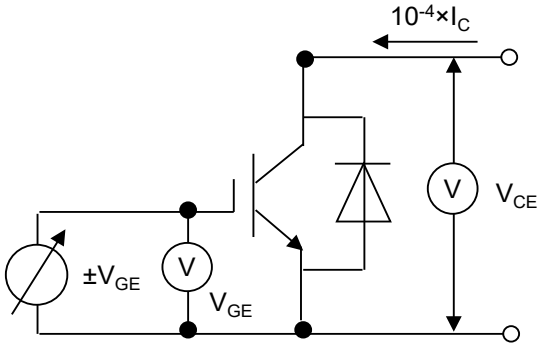



Fig. 3-10 $V_{GE(th)}$ test circuit

■ **$I_{GES}$ : Gate leakage current**

Definition: Gate leakage current when $V_{GE}$ is set to the specified maximum value $V_{GES}$ and the collector-emitter is shorted.
Confirmation test conditions: $V_{GE} = V_{GES}$, $V_{CE} = 0V$ and $T_j = 25°C$

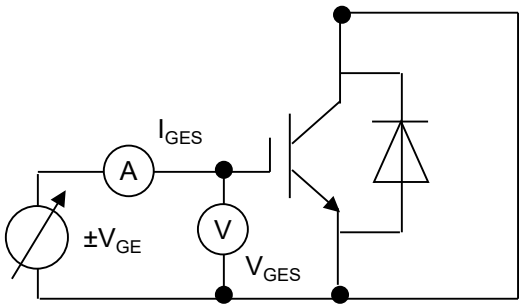



Fig. 3-11 $I_{GES}$ test circuit

■ **$C_{ies}$ : Input capacitance**

Definition: AC capacitance between gate and emitter with collector-emitter shorted.
Confirmation test conditions: $T_j$=25°C, $V_{CE}$=0V, $V_{GE}$=10V and AC 100 kHz (Tested at chip-level)

This is the input capacitance measured between the gate and emitter terminals with the collector shorted to the emitter for AC signals. $C_{ies}$ is made up of the gate to-collector capacitance ($C_{CG}$) in parallel with the gate to emitter capacitance ($C_{GE}$). The input capacitance must be charged to the threshold voltage before the device begins to turn on, and must be discharged to the plateau voltage before the device begins to turn off.

■ **$C_{oes}$ : output capacitance**

Definition: AC capacitance between collector and emitter with gate-emitter shorted.
Confirmation test conditions: $T_j$=25°C, $V_{CE}$=10V, $V_{GE}$=0V and AC 100 kHz (Tested at chip-level)

This is the output capacitance measured between the collector and emitter terminals with the gate shorted to the emitter for AC voltages. $C_{oes}$ is made up of the collector to emitter capacitance ($C_{CE}$) in parallel with the gate to collector capacitance ($C_{CG}$). For soft switching applications, $C_{oes}$ is important because it can affect the resonance of the circuit.

### ■ $C_{res}$ : Reverse transfer capacitance

Definition: AC Capacitance between collector and gate with gate-emitter shorted.
Confirmation test conditions: $T_j$=25°C, $V_{CE}$=10V, $V_{GE}$=0V, AC 100 kHz (Test on chip-level)

This is the reverse transfer capacitance measured between the collector and gate terminals with the emitter connected to ground. The reverse transfer capacitance is equal to the gate to collector capacitance ($C_{CG}$). The reverse transfer capacitance, often referred to as the Miller capacitance, is one of the major parameters affecting voltage rise and fall times during switching.

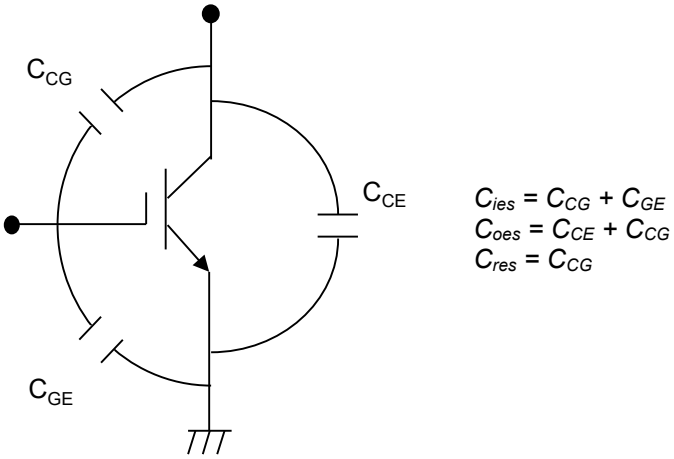



Fig. 3-12 IGBT Capacitances

### ■ $Q_G$ : Total gate charge

Definition: Charge required to raise the gate-emitter voltage from -15V to +15V at IGBT turn-on.

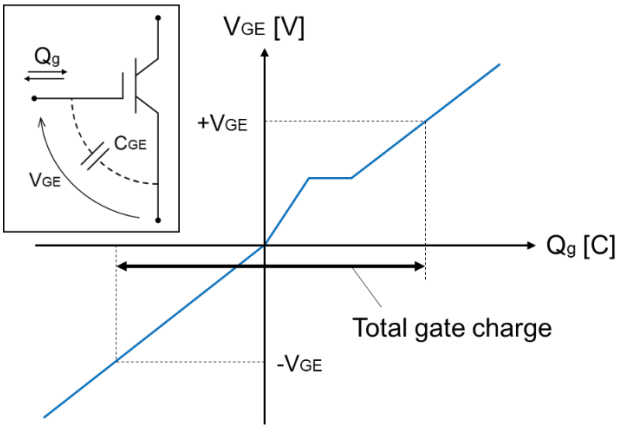



Fig. 3-13 IGBT gate charge

■ **$V_{CEsat}$ : Collector-emitter saturation voltage**

Definition: Collector-emitter voltage at the collector current under specified conditions.
Note 1: $V_{CEsat}$ is measured between auxiliary collector and auxiliary emitter terminals.
Note 2: Pulse width and repetition rate should be selected to cause negligible rise of $T_j$ during the $V_{CEsat}$ testing.

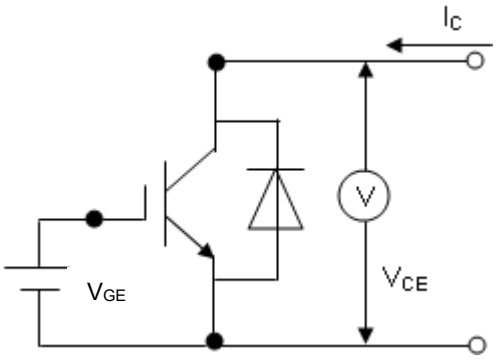



Fig. 3-14 $V_{CEsat}$ test circuit

■ **$t_{d(on)}$ : Turn-on delay time**

Definition: Turn-on delay time is defined as the time between the input gate-emitter voltage reaching 10% of $V_{GE}$ (=1.5V) and the collector current reaching 10% of $I_C$ under specified conditions. (Detail is shown in Fig. 3-16)

■ **$t_r$ : Turn-on rise time**

Definition: Turn-on rise time is the time needed to increase the collector current from 10% $I_C$ to 90% $I_C$ under specified conditions. (Detail is shown in Fig.3-16)

### ■ $E_{on}$, $E_{on(10\%)}$ : Turn-on switching energy

Definition: Switching energy dissipated during turn-on under specified conditions.
(Time definitions are shown in Fig. 3-16)
Two values may be given in Mitsubishi datasheets: $E_{on}$ and $E_{on(10\%)}$.
$E_{on}$ is defined according to IEC60747-9: the integration range is defined between t1 (10% $I_C$) and t3 (2% $V_{CE}$).

$$E_{on} = \int_{t1}^{t3} V_{CE}(t) \times I_C(t)\, dt$$

$E_{on(10\%)}$ is defined for the integration range between t1 (10% $I_C$) and t2 (10% $V_{CE}$).

$$E_{on(10\%)} = \int_{t1}^{t3} V_{CE}(t) \times I_C(t)\, dt$$

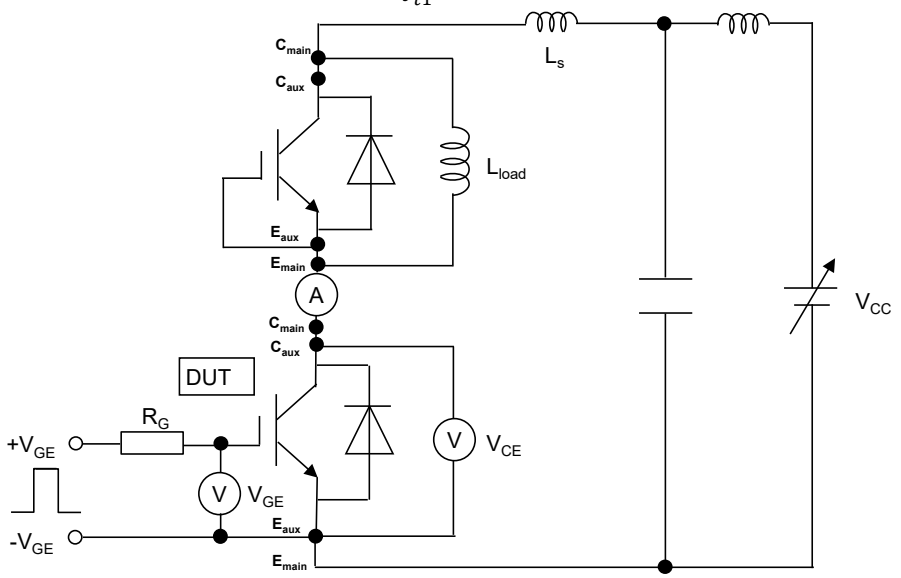



Fig. 3-15 Switching test circuit

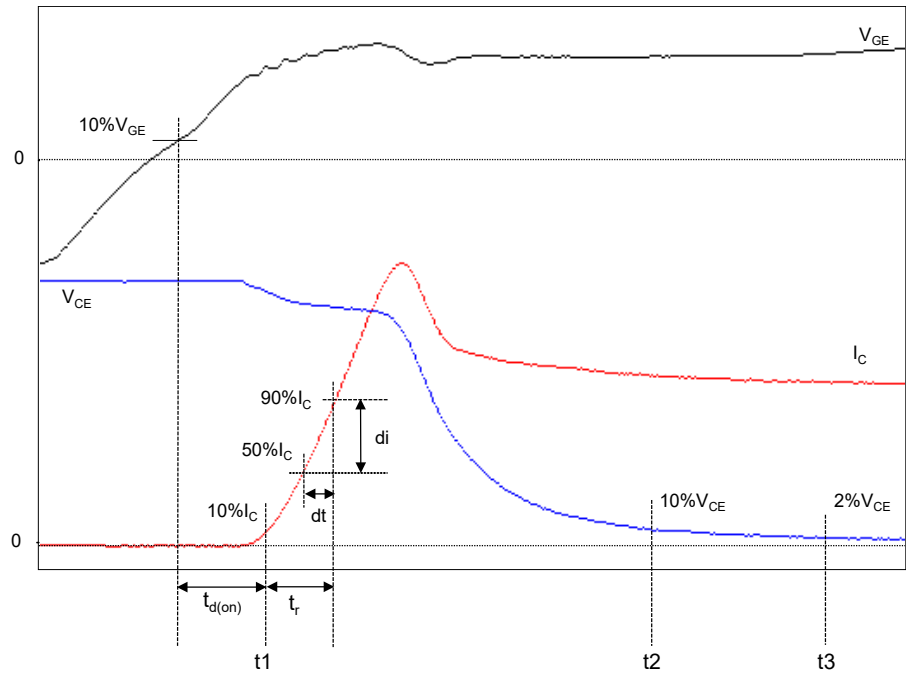



Fig. 3-16 Turn on switching waveform

■ $t_{d(off)}$ : Turn-off delay time

Definition: Turn-off delay time is defined as the time between the input gate-emitter voltage reaching 90% of $V_{GE}$ (=13.5V) and the collector current reaching 90% of $I_C$ under specified condition. (Detail is shown in Fig. 3-17)

■ $t_f$ : Turn-off fall time

Definition: Turn-off fall time is the time needed for the collector current to decrease from 90% $I_C$ to 10% $I_C$ under specified conditions. (Detail is shown in Fig. 3-17)

■ $E_{off}$, $E_{off(10\%)}$ : Turn-off switching energy

Definition: Switching energy dissipated during turn-off under specified conditions.
(Time definitions are shown in Fig.3-17)
Two values may be given in Mitsubishi datasheets: $E_{off}$ and $E_{off(10\%)}$.
$E_{off}$ is defined according to IEC60747-9: the integration range is defined between t1 (10% $V_{CE}$) and t3 (2% $I_C$).

$$E_{off} = \int_{t1}^{t3} V_{CE}(t) \times I_C(t)\, dt$$

$E_{off(10\%)}$ is defined for the integration range between t1 (10% $V_{CE}$) and t2 (10% $I_C$).

$$E_{off(10\%)} = \int_{t1}^{t2} V_{CE}(t) \times I_C(t)\, dt$$

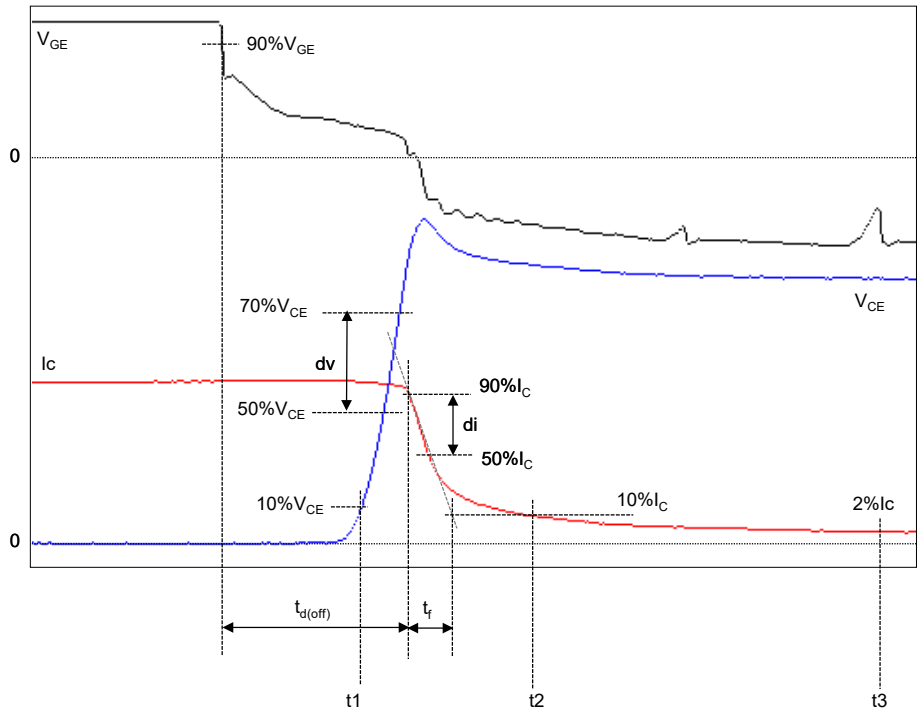



Fig. 3-17 Turn-off switching waveform

■ **$V_{EC}$ : Emitter-collector voltage**

Definition: Emitter-collector voltage at specified free-wheel diode forward current.
Note 1: All parameters marked by suffix “EC” are related to anti-parallel free-wheel diode.
Note 2: $V_{EC}$ is measured between auxiliary collector and auxiliary emitter terminals.
Note 3: Pulse width and repetition rate should be selected to cause negligible rise of $T_j$ during $V_{EC}$ testing.

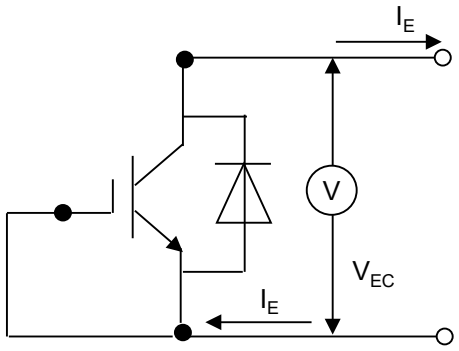



Fig. 3-18 $I_E$ test circuit

■ **$t_{rr}$ : Reverse recovery time**

Definition: Reverse recovery time is defined as the time between the zero crossing of emitter current (t1) and the zero crossing of an approximate line through 90% $I_{rr}$ and 50% $I_{rr}$ under specified conditions.
(Detail is shown in Fig.3-20)

■ **$I_{rr}$ : Reverse recovery current**

Definition: Maximum value of reverse recovery current under specified conditions.
(Detail is shown Fig.3-20)

■ **$Q_{rr}$ : Reverse recovery charge**

Definition: Charge extracted from the free-wheel diode during reverse recovery (between t1 and t4) under specified conditions.
(Details see Fig.3-20)

$$Q_{rr} = \int_{t1}^{t4} I_E(t)\, dt$$

### ■ $E_{rec}$, $E_{rec,(10\%)}$ : Reverse recovery energy

Definition: Reverse recovery energy is the energy dissipated in the free-wheel diode during reverse recovery under specified conditions. (Time definitions are shown in Fig.3-20)
Two values may be given in Mitsubishi datasheets: $E_{rec}$ and $E_{rec(10\%)}$.$E_{rec}$ is defined for integration range between t2 (10% $V_{EC}$) and t4 (2% $I_E$).

$$E_{rec} = \int_{t2}^{t4} V_{EC}(t) \times I_E(t)\, dt$$

$E_{rec}$ should be used for $T_j$ calculation.
$E_{rec(10\%)}$ is defined for integration range between t2 (10% $V_{EC}$) and t3 (10% $I_E$).

$$E_{rec(10\%)} = \int_{t2}^{t3} V_{EC}(t) \times I_E(t)\, dt$$

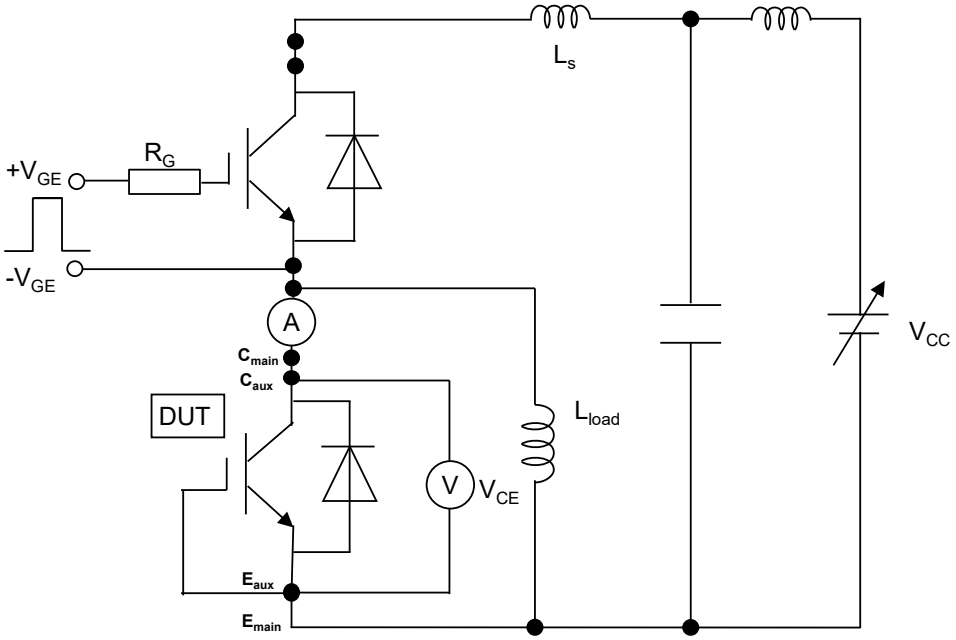



Fig. 3-19 Reverse recovery test circuit

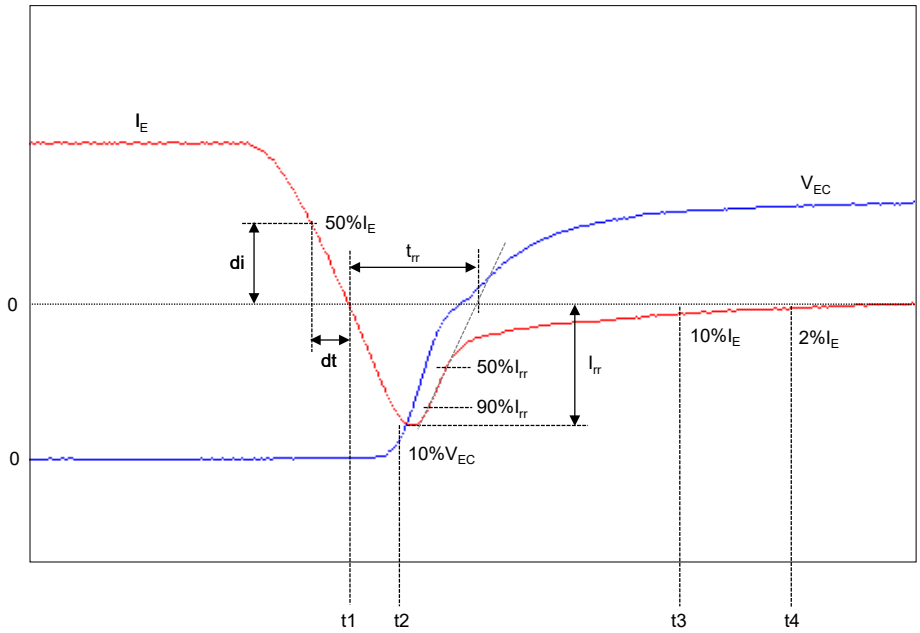



Fig. 3-20 Reverse recovery waveform

## 3.3 Thermal Characteristics

Table 3-3 Thermal characteristics on datasheet for the CM1500HC-66R

**THERMAL CHARACTERISTICS**

| Symbol | Item | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $R_{th(j-c)Q}$ | Thermal resistance | Junction to Case, IGBT part | — | — | 8.0 | K/kW |
| $R_{th(j-c)D}$ | | Junction to Case, FWDi part | — | — | 15.0 | K/kW |
| $R_{th(c-s)}$ | Contact thermal resistance | Case to heat sink, $\lambda_{grease}$ = 1W/m·k, $D_{(c-s)}$ = 100μm | — | 6.0 | — | K/kW |

The thermal resistances given in the Mitsubishi datasheet are based on the thermal equivalent circuit according to Fig.3-21 The Y-model allows calculating $T_j$ for IGBT and free-wheel diode by assuming a homogeneous power flow through the contact resistance from a the module baseplate to a heat sink.

■ **$R_{th(j-c)Q}$ : Thermal resistance (IGBT part)**

Definition: Thermal resistance between IGBT chip (junction) and the case (baseplate).

The thermal resistance $R_{th(j-c)Q}$ is specified as maximum value and defining the temperature difference between IGBT chip and module baseplate ($\Delta T_{(j-c)} = T_j - T_c$). The temperature reference points are located in the center of IGBT chip for Tj and at the surface of baseplate directly below the center of the chip for $T_c$.

■ **$R_{th(j-c)D}$ : Thermal resistance (diode part)**

Definition: Thermal resistance between free-wheel diode chip (junction) and the case (baseplate).

The thermal resistance $R_{th(j-c)D}$ is specified as maximum value and defining the temperature difference between diode chip and module baseplate ($\Delta T_{(j-c)} = T_j - T_c$). The temperature reference points are located in the center of diode chip for $T_j$ and at the surface of baseplate directly below the center of the chip for $T_c$.

■ **$R_{th(c-s)}$ : Contact thermal resistance**

Definition: Thermal resistance between the case and heat-sink under specified conditions.

The thermal resistance $R_{th(c-s)}$ is given in the datasheet as the typical value for a grease having a thermal conductivity λ = 1 W/m and a thickness of d =100μm. This value is given for reference only, and should be confirmed for the actual grease condition used.

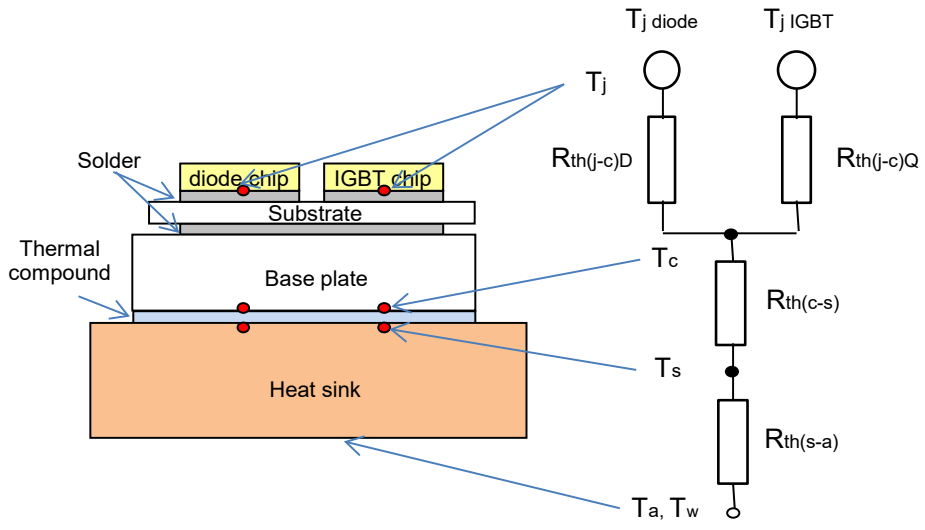



Fig. 3-21 Thermal resistance model

**Confirmation test conditions for the thermal characteristics:**

1. Measurement of calibration curve ($V_{CE}$ – $T_j$)

   The module's dependency between temperature and collector-emitter voltage can be measured in the temperature range of 25°C to 125°C.The calibration curve can then be made from the measurement results for the sake of junction temperature estimation. Fig.3-22 shows the temperature coefficient of the collector-emitter voltage at the low measuring current.

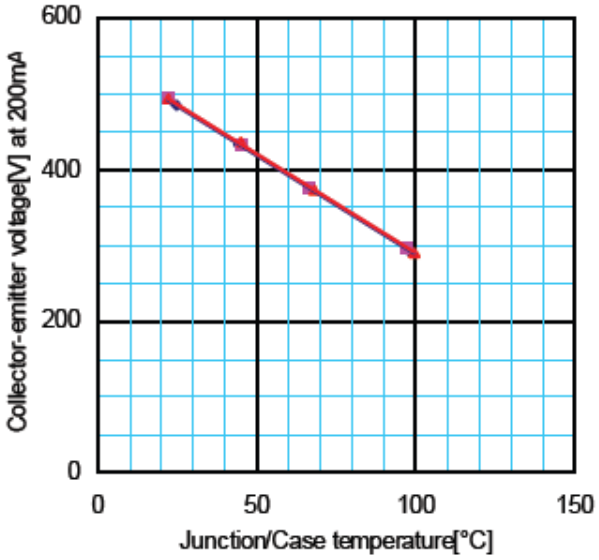



Fig. 3-22 An example of calibration curve ($V_{CE}$ – $T_j$)

2. Attachment method for thermocouples

   Thermocouples should be attached to the heat-sink for temperature measurement of the thermal interface, case to the heat-sink. (see Fig.3-23) These should be attached directly under the IGBT and/or diode chips with rubber boosters and aluminum foil to provide stability and facilitate accurate measurement. The rubber boosters are used to press the thermocouples tips to the baseplate with suitable pressure. The aluminum foil is used between the thermocouple and heat-sink to provide stability with a thermally conductive material. As indicated in Fig. 3-21, the thermocouples in the base-plate and heatsink must be installed in pairs and should be separated by no more than 3-5mm.

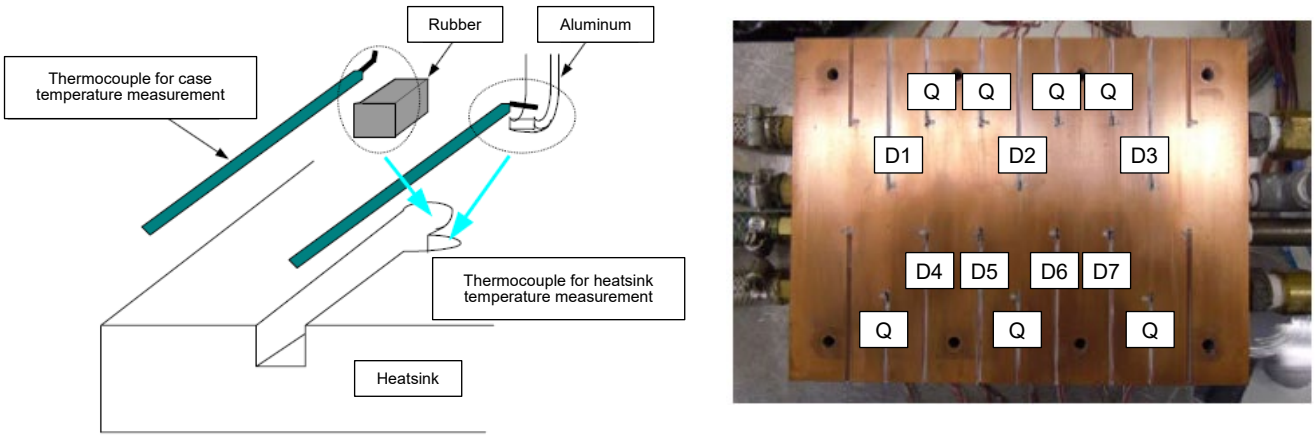



Fig. 3-23 attachment method Thermocouple

3. Measuring thermal resistance

Thermal grease with a thickness of 100μm is applied between the heat-sink surface and the module base-plate. The thickness is estimated from the weight of the thermal grease.

$$Thickness = \frac{Weight\ of\ thermal\ grease}{Density\ of\ thermal\ grease\ \times baseplate\ area}$$

Moreover, the module is mounted on the heat-sink with the rated torque.
The test circuit is shown in Fig.3-24.

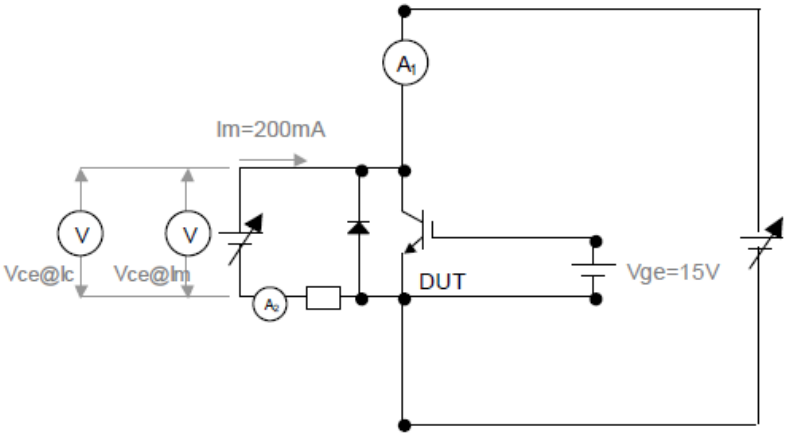



Fig. 3-24 Test circuit for IGBT part

The main collector current should be maintained until the junction temperature, $T_j$, is stable at less than 125°C. The thermal resistance is calculated from the average value of several measurements.

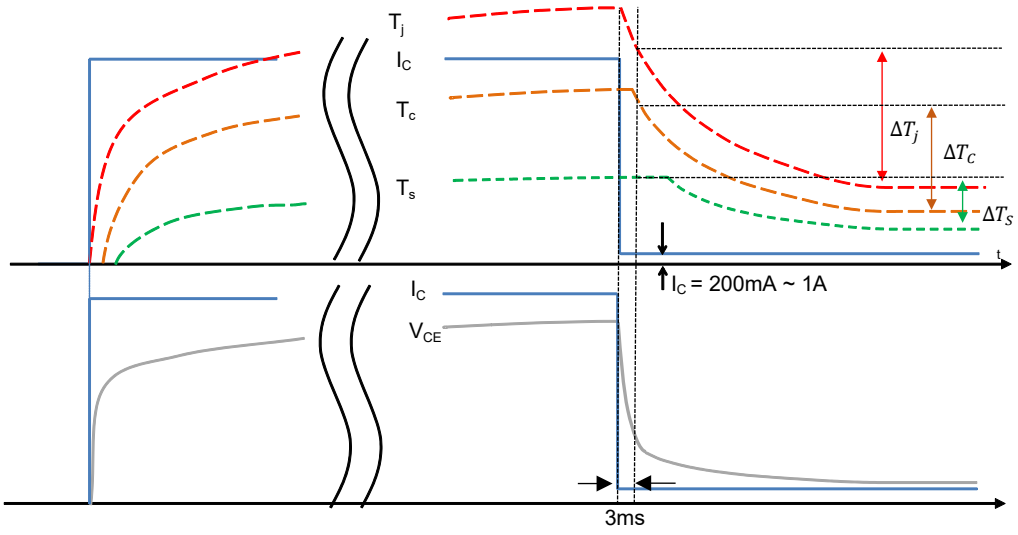



Fig. 3-25 Measurement profile

4. Calculation of the thermal resistance
After junction temperature ($T_j$), case temperature ($T_c$) and heatsink temperature ($T_S$) are stabilized, the transient thermal measurement is finished. Thermal resistances can be calculated using the following equations:

$$R_{th(j-c)Q} = (\Delta T_j - \Delta T_c)/P \ , \ R_{th(c-f)} = (\Delta T_c - \Delta T_S)/P \ , \ P = I_C \times V_{CE}$$

Where $\Delta T_j$, $\Delta T_C$ and $\Delta T_S$ mean temperature differential between the temperature at the time after 3ms from turning off and the saturated temperature.

## 3.4 Mechanical characteristics

Table 3-4 Mechanical characteristics on the datasheet for the CM1500HC-66R

**MECHANICAL CHARACTERISTICS**

| Symbol | Item | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $M_t$ | Mounting torque | M8 : Main terminals screw | 7.0 | — | 22.0 | N·m |
| $M_s$ | | M6 : Mounting screw | 3.0 | — | 6.0 | N·m |
| $M_t$ | | M4 : Auxiliary terminals screw | 1.0 | — | 3.0 | N·m |
| m | Mass | | — | 1.2 | — | kg |
| CTI | Comparative tracking index | | 600 | — | — | — |
| $d_a$ | Clearance | | 19.5 | — | — | mm |
| $d_s$ | Creepage distance | | 32.0 | — | — | mm |
| $L_{P\ CE}$ | Parasitic stray inductance | | — | 11.0 | — | nH |
| $R_{CC'+EE'}$ | Internal lead resistance | $T_C$ = 25°C | — | 0.12 | — | mΩ |
| $r_g$ | Internal gate resistance | $T_C$ = 25°C | — | 1.5 | — | Ω |

■ $M_t$: Mounting torque at terminal screw

Definition: Allowable range for the torque on the terminal screws.

■ $M_s$: Mounting torque at mounting screw

Definition: Allowable range for the torque on the mounting screws.

■ m: Mass

Definition: Mass of the IGBT module.

■ CTI: Comparative Tracking Index

Definition: A value indicating the performance of tracking resistance for an insulator.

The CTI value characterizes the plastic material used for the module's package. With the help of CTI the minimum creepage distance can be defined for a given pollution degree according to IEC standard 60112.

■ $d_a$: Clearance

Definition: The shortest distance in air between two conductive parts.

■ $d_s$: Creepage distance

Definition: The shortest distance along the surface of the insulating material between two conductive parts. Measurement of creepage distances and clearances are according to IEC standard 60664-1(Edtion5.0).

■ $L_{P\ CE}$: Parasitic stray inductance

Definition: Total parasitic stray inductance inside the module between the main collector terminal and the main emitter terminal. (See Fig.3-26)

■ $R_{CC'+EE'}$: Internal lead resistance

Definition: The resistances between the main collector terminal and the auxiliary collector terminal ($R_{CC'}$) and between the main emitter and the auxiliary emitter terminal ($R_{EE'}$). (See Fig.3-26)

■ $r_g$: Internal gate resistance

Definition: Internal series gate resistance inside the module. (See Fig. 3-26)

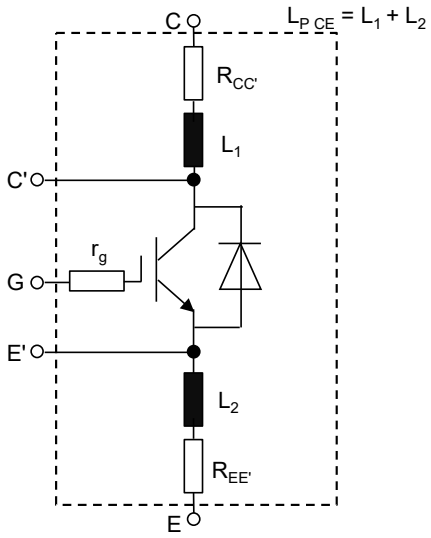



Fig. 3-26 Parasitic stray inductances, internal lead resistances, and internal gate resistance

## 3.5 Performance Curves

The performance curves show the typical electrical characteristics and the maximum transient thermal impedance characteristics of the IGBT and FWDi. These characteristics can be used to calculate power losses and junction temperature rise for operating conditions.

■ **Output characteristics**

The output characteristics define the value of $V_{CE}$ that the IGBT will have when conducting a given $I_C$ for a given value of $V_{GE}$. The IGBT is intended for switching operation only and the range for practical use is limited to the range of $V_{CE}$ within the saturation area.

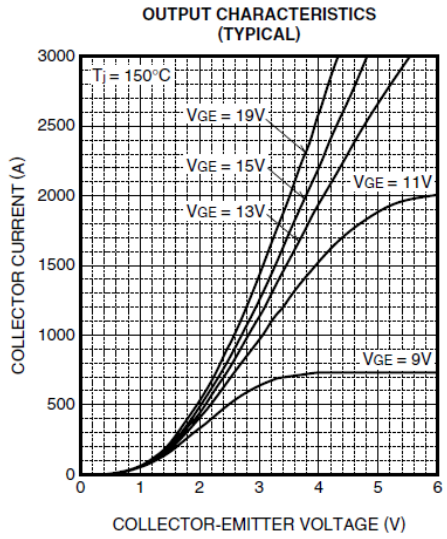
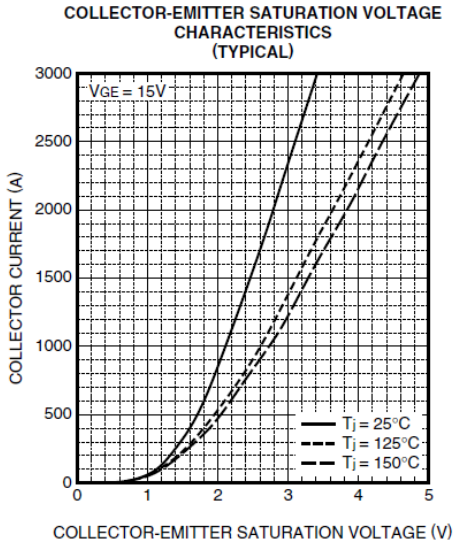
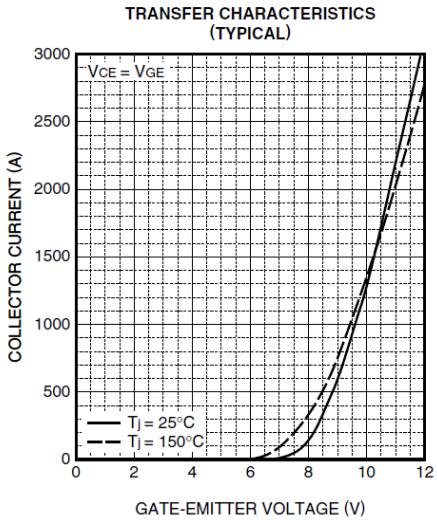



Fig. 3-27 Output characteristics (Typical)

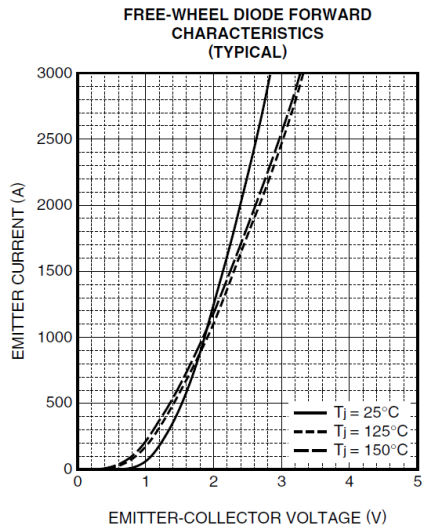
## ■ Collector-emitter saturation voltage characteristics

| | |
|---|---|
| $V_{CEsat}$ is given as a function of the collector current at the junction temperatures of 25°C, and 125°C, and 150°C. |  <br>Fig. 3-28 Collector-emitter saturation voltage characteristics (Typical) |

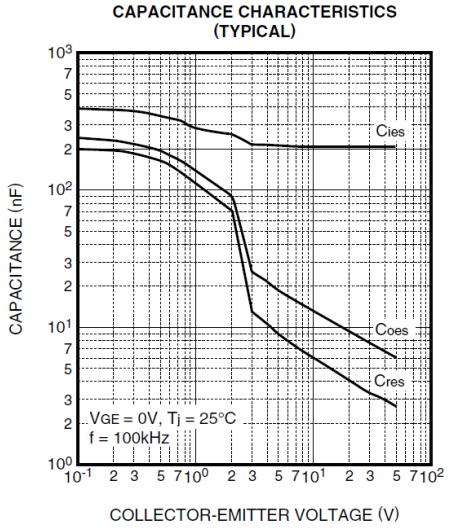
## ■ Transfer characteristics

| | |
|---|---|
| Transfer characteristics show that the maximum allowable collector current for corresponding gate-emitter voltage and junction temperatures. The turn-on threshold voltage decreases with increasing with increasing junction temperature. |  <br>Fig. 3-29 Transfer characteristics (Typical) |

## ■ Free-wheel diode forward characteristics

| | |
|---|---|
| $V_{EC}$ is given as a function of the diode forward current at the junction temperatures of 25°C, 125°C and 150°C. |  <br>Fig. 3-30 Free-wheel diode forward characteristics (Typical) |

## ■ Capacitances characteristics

| | |
|---|---|
| The capacitance characteristics curves show the input, output, and transfer capacitances as a function of the collector-emitter voltage.<br>The definitions of these characteristic are described in the chapter 3.2. (see page 14) |  <br>Fig. 3-31 Free-wheel diode forward characteristics (Typical) |

## ■ Gate charge characteristics

The curve shows the gate-emitter voltage as a function of the gate charge at the typical collector-emitter voltage, rated collector current, and junction temperature of 25°C.
The definition of the gate charge characteristics is described in chapter 3.2.(see page 14)

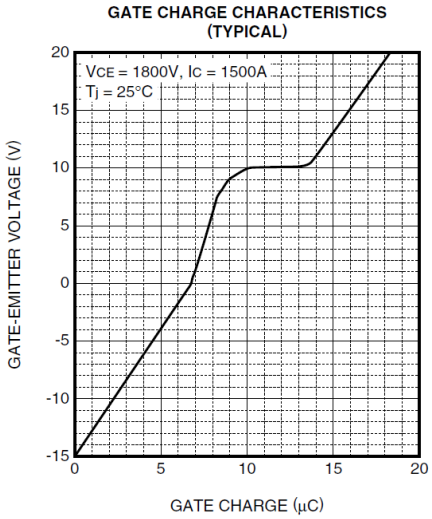



Fig. 3-32 Free-wheel diode forward characteristics (Typical)

## ■ Switching energy characteristics (Current dependency)

The switching energy characteristics show the typical switching energies for the IGBT and diode as a function of the collector current at the specified conditions.
These definitions of these characteristic are described in chapter 3.2.

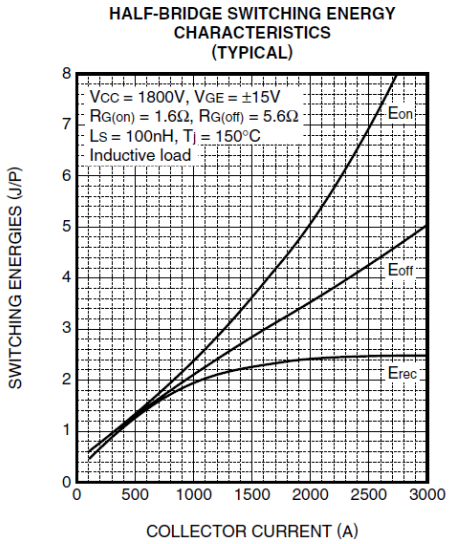



Fig. 3-33 Switching energy characteristics (Typical)

■ **Switching energy characteristics (Gate resistance dependency)**

The switching energy characteristics show the typical switching energies for the IGBT and diode as a function of the external series gate resistance at the specified conditions.
The definitions of these characteristics are described in chapter 3.2.

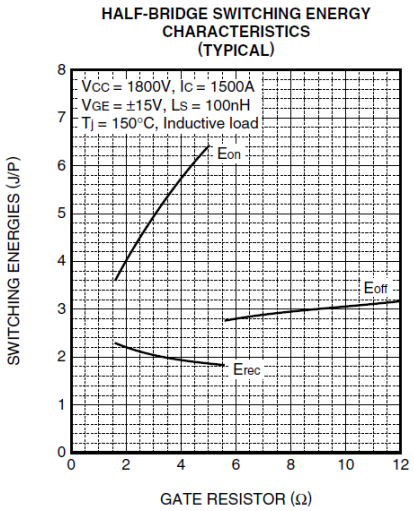



Fig. 3-34 Switching energy characteristics (Typical)

■ **Switching time characteristics (Current dependency)**

The switching time characteristics show the typical switching times for the IGBT as a function of the collector current at the specified conditions.
The definitions of these characteristics are described in chapter 3.2.

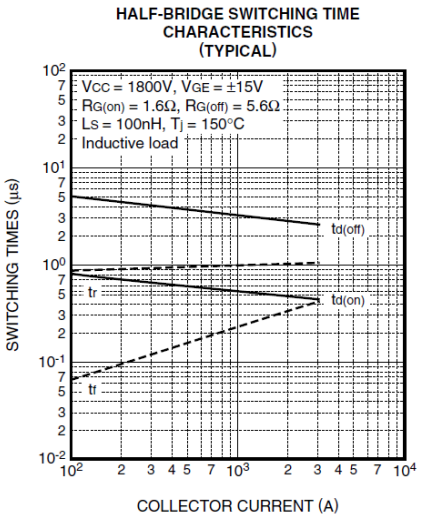



Fig. 3-35 Switching time characteristics (Typical)

■ **Diode reverse recovery characteristics**

The reverse recovery characteristics show the typical $I_{rr}$ and $t_{rr}$ characteristics for the free-wheel diode as a function of the emitter current at the specified conditions.

The definitions of these characteristics are described in chapter 3.2.

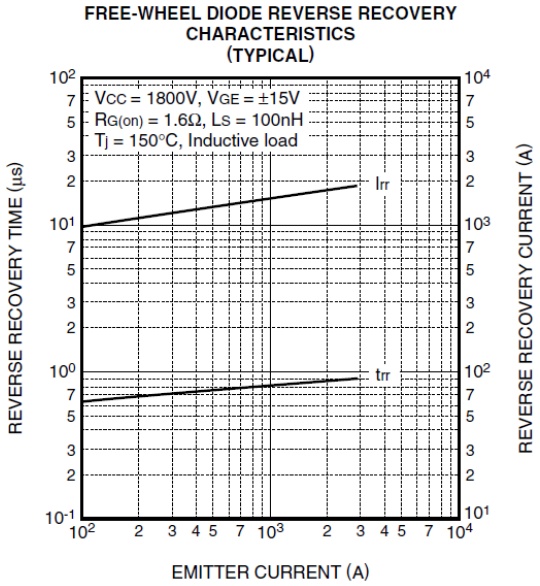



Fig. 3-36 Diode reverse recovery characteristics (Typical)

■ **Transient thermal impedance characteristics**

The transient thermal impedance characteristic can be used to calculate the rise of junction temperature over case temperature per unit of power applied for a given time period.
The value of $Z_{th(j-c)}$ is obtained by multiplying the value of $R_{th(j-c)}$ by the normalized factor taken from the curve at the time of interest.

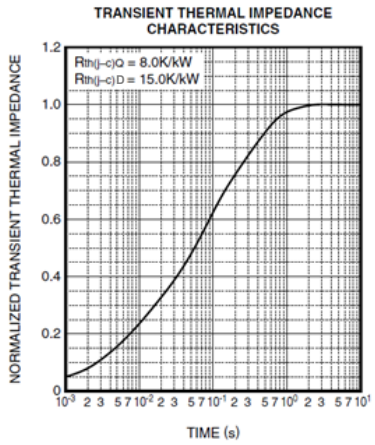
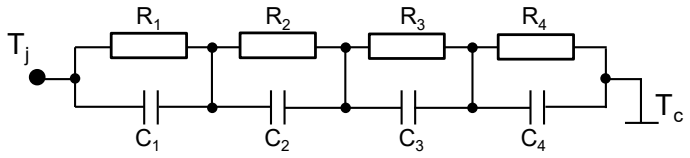



Fig. 3-37 Transient thermal impedance characteristics

The transient thermal impedance $Z_{th(j-c)}$ characteristic is fitted to numeric characteristics $R_i$ and $C_i$. They have no physical meaning.

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i \left\{ 1 - exp\left( -\frac{t}{\tau_i} \right) \right\}$$

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| $R_i$ [K/kW] : | 0.0096 | 0.1893 | 0.4044 | 0.3967 |
| $\tau_i$ [sec] : | 0.0001 | 0.0058 | 0.0602 | 0.3512 |



## 3.6 Safe Operating Areas

The Safe Operating Areas (SOA) given in the datasheets specify the absolute maximum limits that must not be exceeded in any operation mode of the device. To ensure that this rule is not violated, the user must carefully check each SOA under all application conditions and design in a proper margin for the identified worst case conditions. This margin should cover all possible application tolerances and overload conditions. Three different SOA must be considered:

- Reverse Bias SOA (RBSOA)
- Short Circuit SOA (SCSOA)
- Reverse Recovery SOA (RRSOA)

## 3.7 Reverse Bias Safe Operating Area (RBSOA)

The RBSOA specifies the limits of IGBT turn-off capability. The RBSOA curve is the locus of points defining the maximum allowable simultaneous occurrence of collector current, $I_C$, and collector- to- emitter voltage, $V_{CE}$ , during a turn-off of the IGBT from its saturated conduction state.
Three different limits can be distinguished within the RBSOA:

a) The maximum collector current $I_{C(max)}$ allowed to be turned-off
b) The maximum collector-to-emitter voltage magnitude $V_{CE(max)}$ during turn-off
c) At high $I_C$- and $V_{CE\text{-}values}$, a de-rating area may be present in the RBSOA

An example RBSOA (for CM1500HC-66R) is shown in Fig. 3-38

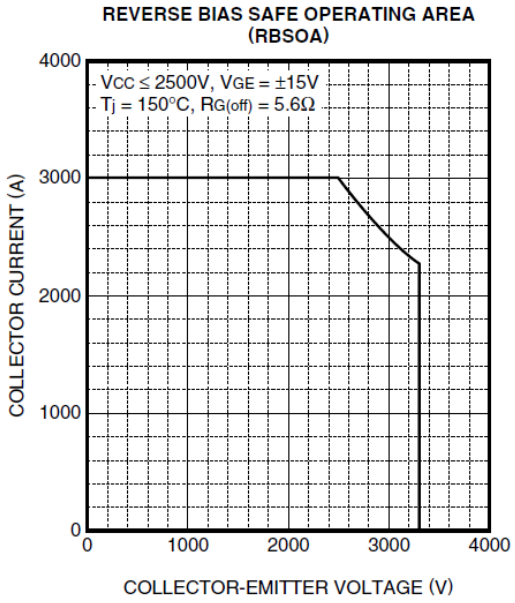



Fig. 3-38 RBSOA curve (for CM1500HC-66R)

The conditions under which the RBSOA is specified are:

- The DC-link voltage $V_{CC}$ should not exceed the given maximum value ($V_{CC}$ ≤ 2500V).
- The gate driver voltage $V_{GE}$ should be switched from +15V to -15V during turn-off
- The junction temperature $T_j$ should not exceed the given maximum value ($T_j$=150°C)
- The gate resistance at turn-off should not be smaller than the indicated minimum value ($R_{G(off)}$=5.6Ω)
- The DC-link inductance $L_s$ should not exceed the value given in the datasheet as condition for $E_{off}$ ($L_s$=100nH for CM1500HC-66R)

The RBSOA must be confirmed during device qualification for each new converter design under real application conditions. For this purpose, the HVIGBT modules should be mounted into the real application circuit using the intended DC-bus and gate driver.

The test should be done by single pulse testing individually **each HVIGBT-module's** mounting position in the converter using a half bridge switching test circuit with an inductive load (see Fig.3-39). This individual confirmation testing will help ensure that all possible worst case conditions, even with parasitic effects due to the individual mounting position, will be covered.

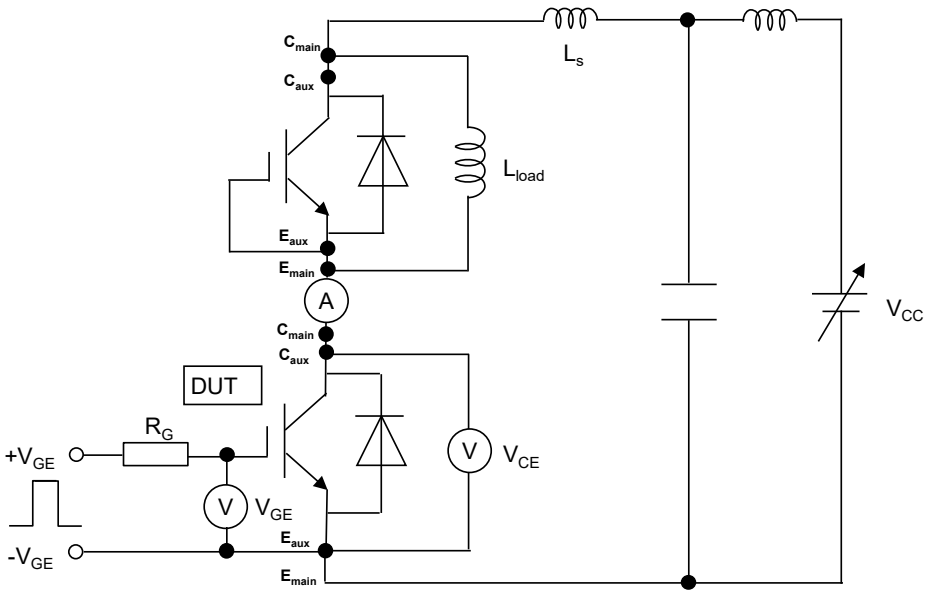



Fig. 3-39 RBSOA test circuit

Typical $I_C$ and $V_{CE}$-waveforms obtained by oscilloscopes and their transformation into the RBSOA-curve are shown in Fig. 3-40.

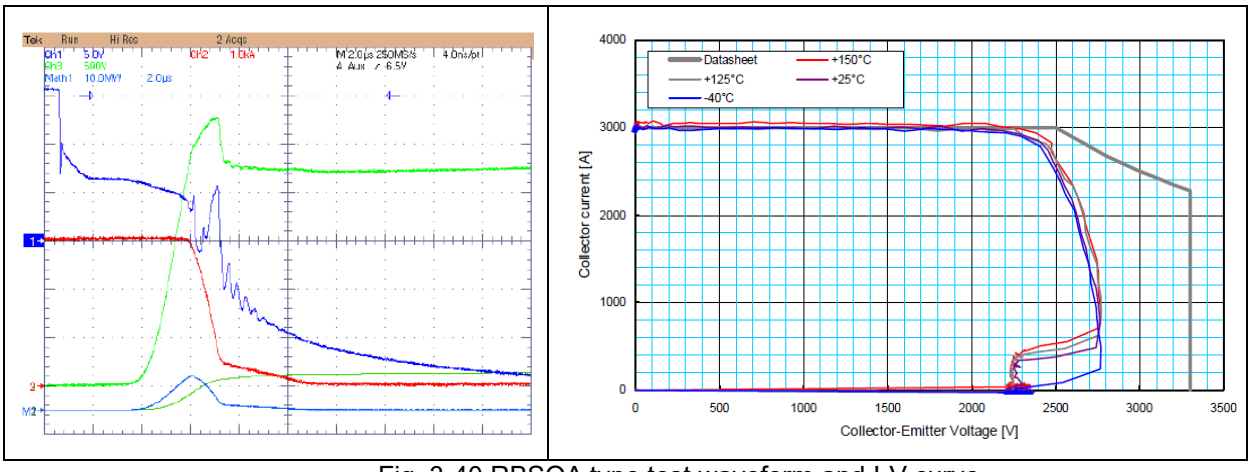



Fig. 3-40 RBSOA type test waveform and I-V curve

To correctly perform the RBSOA confirmation testing, the following considerations should be taken into account:

- The instantaneous value of collector to emitter voltage, $V_{CE}$, must be sensed between the auxiliary collector and emitter terminals of the DUT during turn-off (see Fig. 3-39).
- The $I_C$ current sensor should not significantly increase the total DC-link inductance, $L_s$.
- If the real value of DC-link inductance, Ls, exceed the value given as a condition for $E_{off}$ in the datasheet ($L_s$=100nH for the given example CM1500HC-66R), the RBSOA-limits should be reconfirmed with Mitsubishi application engineering.
- When converting the $I_C(t)$- and $V_{CE}(t)$-waveforms obtained by oscilloscope into an $I_C$-$V_{CE}$, special care should be taken for correctly compensating any delay of the $I_C$ current sensor. Non-compensated $I_C$-waveforms may result in wrong RBSOA confirmation test results.
- The non-violation of RBSOA should be confirmed for the complete range of operation conditions $I_C$, $V_{CC}$ and $T_j$. For all application conditions, the tested $I_C$-$V_{CE}$-curves should stay safely within the RBSOA-limit.

## 3.8 Short Circuit Safe Operating Area (SCSOA)

The SCSOA is specifies the limits of IGBT turn-off capability under short circuit conditions.
The main differences compared to RBSOA are:

- The SCSOA is valid for the single turn-off events only (in emergency cases), not for periodical switching. It is recommended not to exceed 1000 short circuit events over the lifetime of a module.
- The SCSOA describes the limits for IGBT turn-off from its de-saturated conduction state, meanings before SC, turn-off, the IGBT is limiting the collector current magnitude by being de-saturated.

When considering the short-circuit withstand capability of the HVIGBT modules, two different cases are generally reviewed:

**SC type 1**: When the IGBT is turned-on into an already existing external short circuit
**SC type 2**: When an external load or ground-fault short circuit is applied to an IGBT that is already in on-state

Fig. 3-41 and Fig. 3-42 show the circuitry and waveforms for SC type1 and SC type 2 testing.

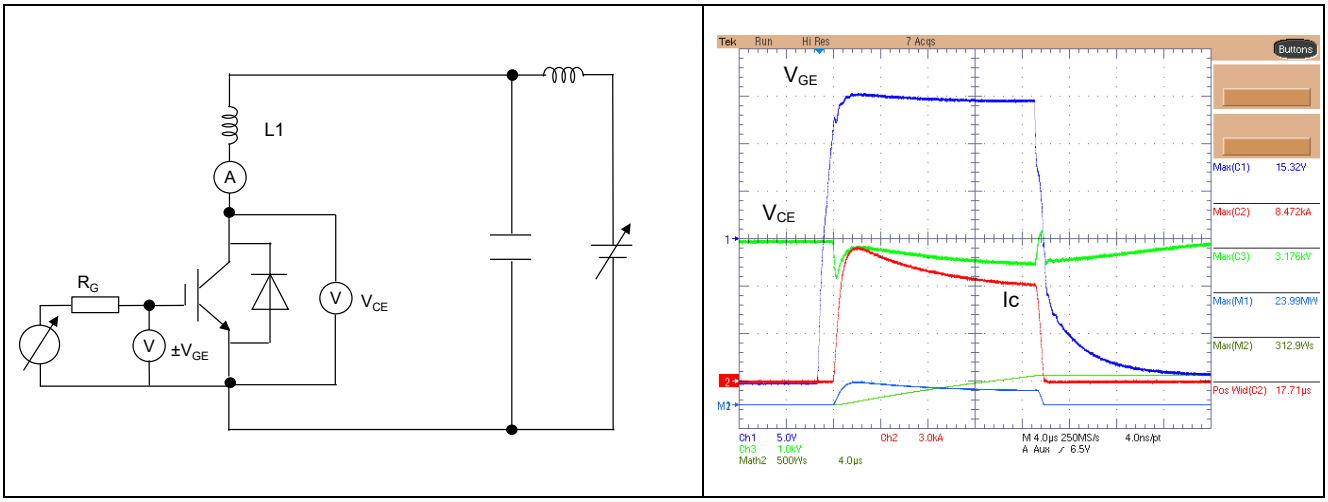



Fig. 3-41 SC type1 test circuit and waveform

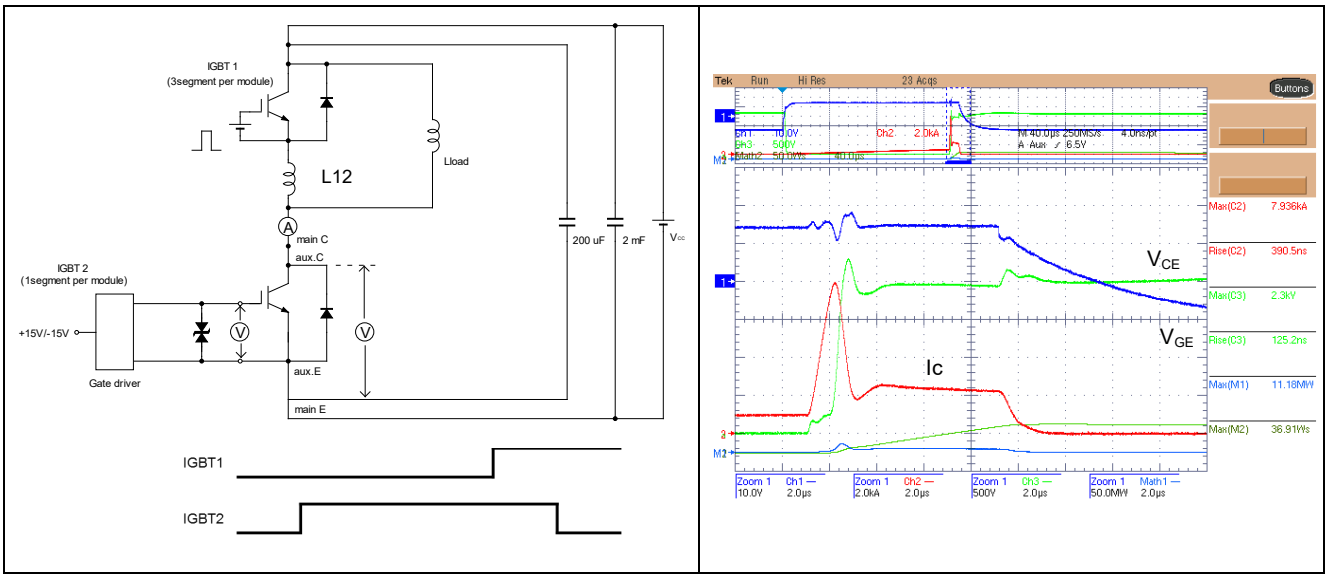



Fig. 3-42 SC type2 test circuit and waveform

In **SC type 1**, as the IGBT turns on, the initial rise rate of $I_C$ is determined by the IGBT turn-on speed and the external short circuit loop inductance, L1. During the rising time of SC-current, the collector-to-emitter voltage, $V_{CE}$, is reduced. When the SC-current is reaching the saturation current density, the IGBT becomes de-saturated by limiting the collector current to its peak value, $I_{CP}$, while the collector-to-emitter voltage, $V_{CE}$, switches back to almost full DC-link voltage, $V_{CC}$. The dv/dt at this time is coupled to the gate through the reverse transfer capacitance thus causing a momentary rise of gate voltage, $V_{GE}$. This positive feedback effect translates to a higher peak collector current, $I_{CP}$. Careful gate drive design should limit this $V_{GE}$-increase in order to prevent the short circuit current, $I_{CP}$, from increasing beyond the limit given in the SCSOA.

In **SC type 2**, an external short circuit occurs while the IGBT is already in an on-state. The initial rise rate of $I_C$ is determined only by the external short circuit inductance, L12. The increasing short circuit current forces the IGBT to de-saturate, causing the collector-to-emitter voltage to rise from $V_{CE(sat)}$ to almost full DC-link voltage, $V_{CC}$. The resulting dv/dt during IGBT desaturation is higher than in SC type 1 thus causing a stronger positive feedback on the gate voltage via the reverse transfer capacitance. Consequently, the resulting peak saturation current, $I_{CP}$, may reach a higher magnitude compared to SC type 1.

For both **SC type 1** and **SC type 2,** the high short circuit current magnitude and high collector emitter voltage cause very high power loss in the IGBT chip during SC-operation. As a result, the IGBT chip temperature rises, causing the saturation current to decrease from its initial peak value, $I_{CP}$. To protect the device from destruction by over-temperature, the short circuit current has to be cut off within a specified SC-time, tw. For a Mitsubishi HVIGBT, this SC-time is specified as $t_{psc}$ on the datasheets.

At turn-off, the di/dt of decreasing collector current, $I_C$, in the inductance L1, causes a voltage spike, $\Delta V_{CE}$. This voltage spike is superimposed to the DC-link voltage, $V_{CC}$. The instantaneous value of this collector-to-emitter, voltage, $V_{CE}$, must not be allowed to go beyond the specified limit given by the SCSOA-curve, which is valid both for SC type 1 and SC type 2.

An example SCSOA (for the CM1500HC-66R) is shown in Fig. 3-43

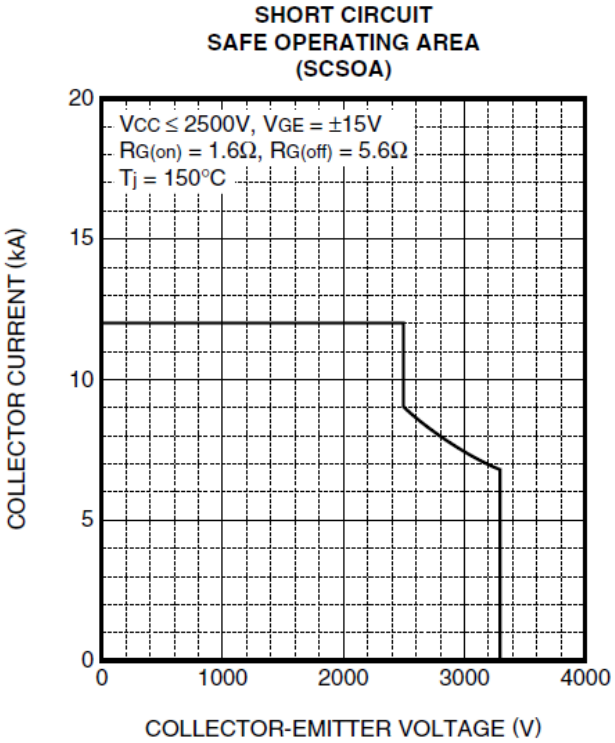



Fig. 3-43 SCSOA curve (for the CM1500HC-66R)

The conditions under which the SCSOA is specified are (CM1500HC-66R example):

- The DC-link voltage, $V_{CC}$, should not exceed the given maximum value ($V_{CC}$ ≤ 2500V).
- The gate driver voltage, $V_{GE}$, should be switched between +15V and -15V
- The junction temperature, $T_j$, at SC-start should not exceed the given value (Tj=150°C)
- The gate resistance at SC-turn-on (case 1) should not be smaller than the given value ($R_{G(on)}$=1.6Ω)
- The gate resistance at SC-turn-off (case 1 and case 2) should not be smaller that the given value ($R_{G(off)}$ =5.6Ω)
- The maximum duration of short circuit should not exceed $t_{psc}$

Besides the above conditions, the following considerations should alsohave to be taken into account for to correctly confirming  confirm the SCSOA in a given application:

- The instantaneous value of collector-to-emitter voltage, $V_{CE}$, during turn-off must be sensed between the auxiliary collector and emitter terminals of the DUT.
- When doing SCSOA confirmation testing, enough time should pass in between 2 SC-tests to ensure a complete $T_j$ relaxation before the next SC-event.
- To limit the overvoltage spike at SC turn-off, it is acceptable to use dedicated gate driving techniques for reducing the di/dt at SC turn-off, such as increased turn-off gate resistance, $R_{G(off)}$, or active gate clamping.
- The non-violation of SCSOA should be confirmed for the complete range of operating conditions $V_{CC}$ and $T_j$.

## 3.9 Reverse Recovery Safe Operating Area (RRSOA)

The RRSOA specifies the limits of the free-wheeling diode (FWD) at reverse recovery. The RRSOA is valid for repetitive switching operation. The RRSOA curve is the locus of points defining the maximum allowable simultaneous occurrence of reverse recovery current, $I_{rr}$, and cathode-to-anode voltage, $V_{EC}$, during FWD reverse recovery.
Three different limits can be distinguished within the RRSOA:
a) The maximum reverse recovery current magnitude, $I_{rr}$(max);
b) The maximum reverse recovery Power, $P_{rr}$(max)
c) The maximum voltage magnitude, $V_{EC}$(max), at reverse recovery

An example RRSOA (for the CM1500HC-66R) is shown in Fig. 3-44.

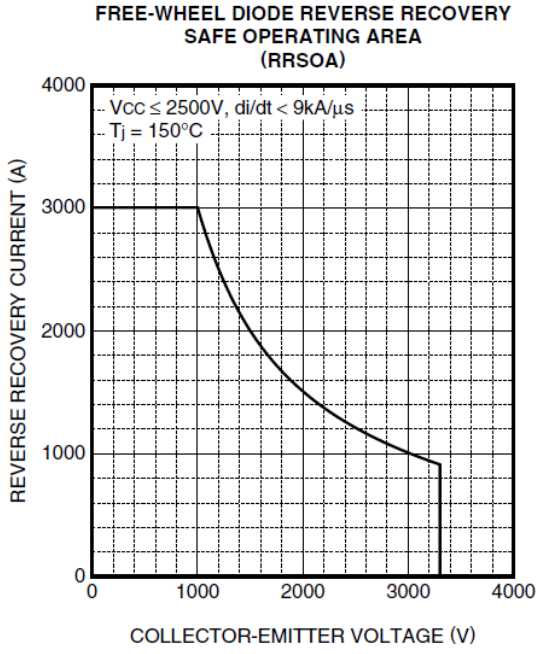



Fig. 3-44 RRSOA curve (for the CM1500HC-66R)

The conditions under which the RRSOA is specified are (CM1500HC-66R example):

- The DC-link voltage, $V_{CC}$, should not exceed the given maximum value ($V_{CC}$ ≤ 2500V).
- The gate resistance for the switching IGBT should not be smaller than the given value ($R_{G(on)}$=1.6Ω)
- The maximum reverse recovery current, $I_{rr}$, should not exceed the given maximum value ($I_{rr}$ ≤ 3000A).
- The junction temperature, $T_j$, should not exceed the given maximum value ($T_j$=150°C)
- The DC-link inductance, $L_s$, should not exceed the value given in the datasheet as condition for $E_{rec}$ ($L_s$=100nH)

The RRSOA must be confirmed during device qualification for each new converter design under real application conditions. For this purpose, the HVIGBT modules should be mounted in the real application circuit by using the intended DC-bus and gate driver. The test should be done by double-pulse testing (see Fig. 3-46) individually **at for each HVIGBT-module's** mounting position in the converter, using the half-bridge switching test circuit with an inductive load (see Fig. 3-45). The suggested individual confirmation testing should ensure that all possible worst case conditions, even with parasitic effects due to the individual mounting position, will be covered.

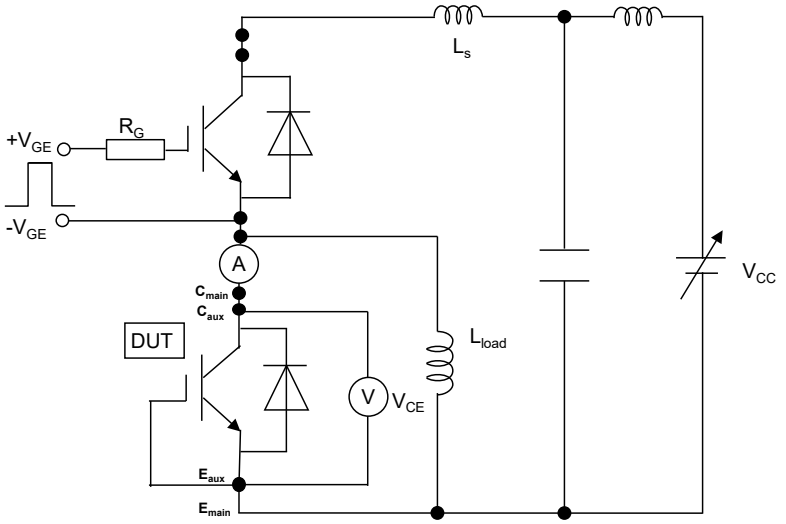



Fig. 3-45 Reverse recovery test circuit

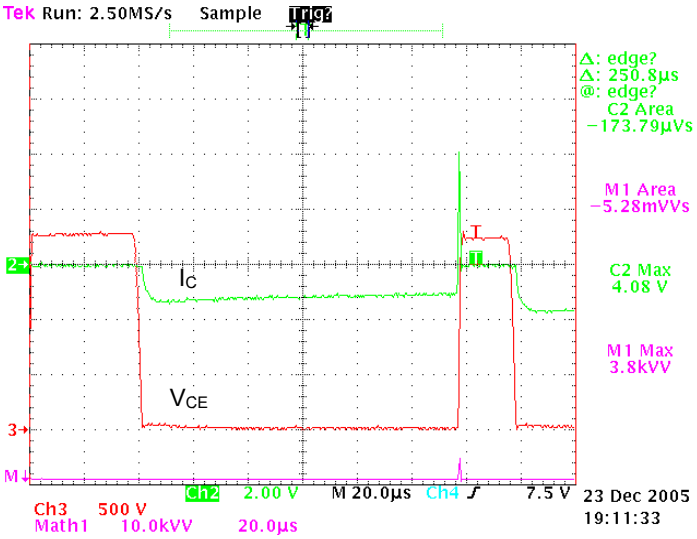



Fig. 3-46 Double pulse test sequence

Typical Irr and Vec-waveforms and their transformation into the RRSOA-curve are shown in Fig. 3-47.

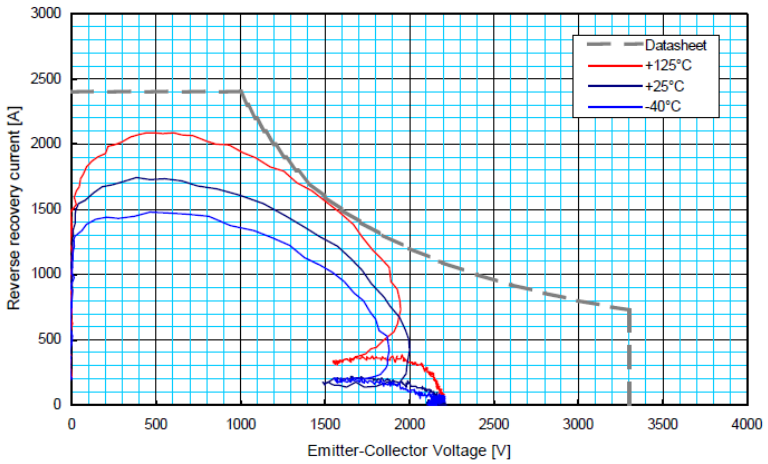



Fig. 3-47 RRSOA with I-V switching curve

To correctly perform the RBSOA confirmation testing, the following considerations should be taken into account:

- The instantaneous value of emitter to collector voltage, $V_{CE}$ must be sensed during a turn-off between the auxiliary collector and emitter terminals of the DUT (see Fig. 3-45 )
- The $I_C$ current sensor should not significantly increase the total DC-link inductance, $L_s$
- If the real value of DC-link inductance, $L_s$, is exceeding the value given as a condition for $E_{off}$ in the datasheet (Ls=100nH for the given example CM1500HC-66R) the RRSOA-limits should be reconfirmed with Mitsubishi application engineering.
- When checking the di/dt-condition at reverse recovery, the $dI_e/dt$-definition for $E_{rec}$ between 0% and 50% should be used (see chapter 3.2)
- When converting the $I_E(t)$- and $V_{EC}(t)$-waveforms obtained by oscilloscope into the $I_E$-$V_{EC}$-curve, special care should be taken to correctly compensate for any delay of the $I_E$ current sensor. Non- compensated $I_E$-waveforms may result in incorrect RRSOA confirmation test results.
- The non-violation of RRSOA should be confirmed for the complete range of operation conditions : $I_E$; $V_{CC}$ and $T_j$. For all application conditions, the tested $I_C$-$V_{CE}$-curves should stay safely within the RRSOA-limits.

# 4. FWDi Forward Surge Current vs. Pulse Width

## 4.1 Expected diode surge current for different pulse lengths

Mitsubishi HVIGBT modules contain one IGBT and an anti-parallel free-wheel diode. The anti-parallel free-wheel diode cannot control current.
During a fault case, as inrush can current occur and cause failures in the inverter. The diode forward surge current appears in various waveforms shown below (Fig. 4-1). Semiconductors also have a temperature limitation. When a semiconductor exceeds its temperature limitation, it typically fails.

$$T_{j\_limit} = I^2t \cdot Z_{th(j-c)} = constant$$

The surge current limitation of the free-wheel diode will depend on the pulse length ($t_p$) and the $T_j$. Transient thermal impedance also becomes especially important when considering the surge current. $I_{FSM}$ and $I^2t$ are defined below.

■ $I_{FSM}$ : Forward surge current

Definition: Maximum allowable value of the forward surge current during a half sine-wave.
Parameter: $T_{j\_start}$, $t_p$

■ $I^2t$ : Surge current load integral

Definition: Maximum allowable value of the power load integral of a half sine-wave surge.
Parameter: $T_{j\_start}$, $t_p$

$$I^2t = \int_0^{t_p} i(t)^2\, dt = \frac{{I_{FSM}}^2}{4f} = \frac{{I_{FSM}}^2 \cdot t_p}{2}$$

$$i(t) = I_{FSM} \cdot \sin(t)$$

The forward surge current ($I_{FSM}$) and the surge current load integral ($I^2t$) are measured and calculated below using the method shown above.

1. Test of the forward surge current to device failure.

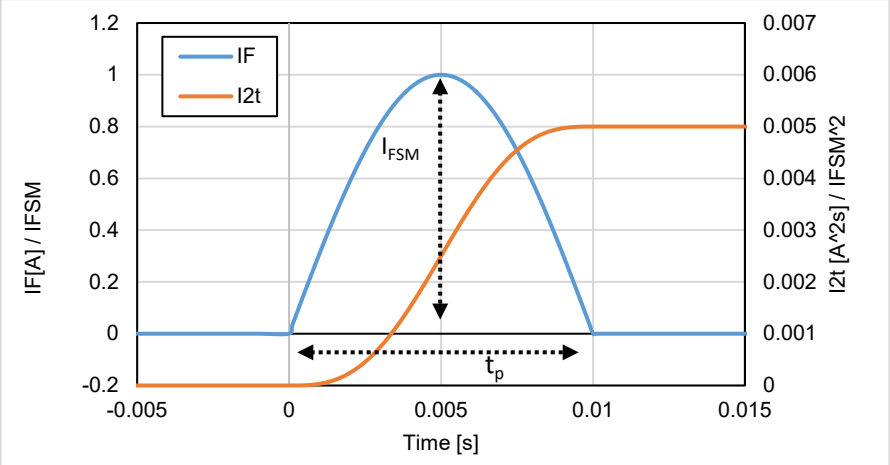



Fig. 4-1 An example of a forward surge current waveform

2. Use the Weibull chart to find the failure rate (see Fig. 4-2).

3. Calculate the pulse length dependency of the IFSM and the I2t using the following equation and the transient thermal impedance characteristics (see Fig. 4-3).

$$I_{FSM}(t_p) = I_{FSM}(@measured\ pulse\ length) \cdot \sqrt{\frac{Z_{th(j-c)}\ (@measured\ pulse\ length)}{Z_{th(j-c)}(t_p)} \cdot \frac{1}{t_p}}$$

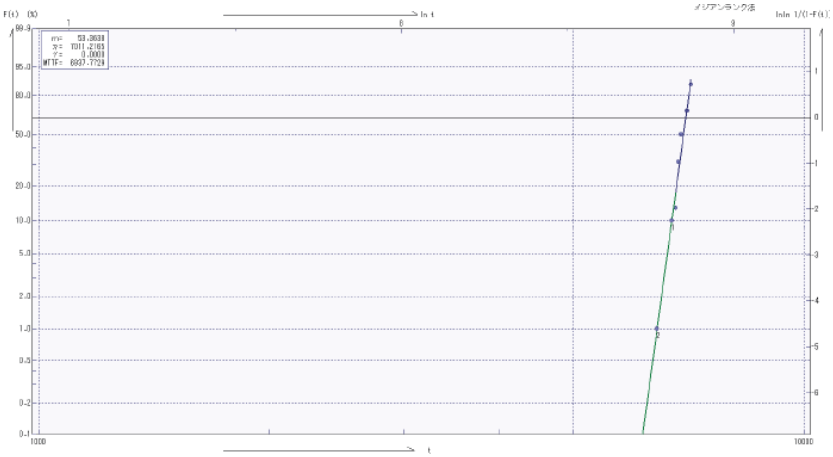


Fig. 4-2 Weibull chart

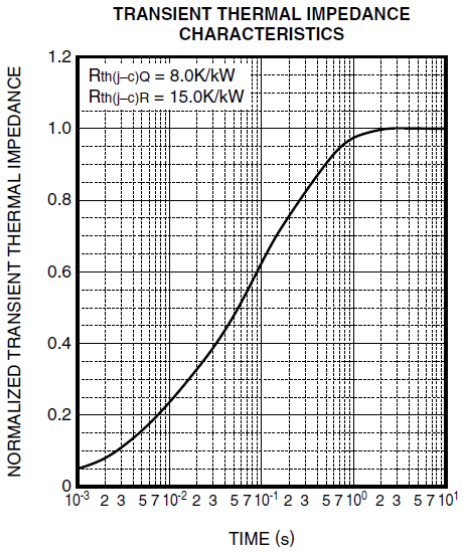



Fig. 4-3 Transient thermal impedance characteristics for a HVIGBT module

# - FWDi Forward Surge Current vs. Pulse Width -

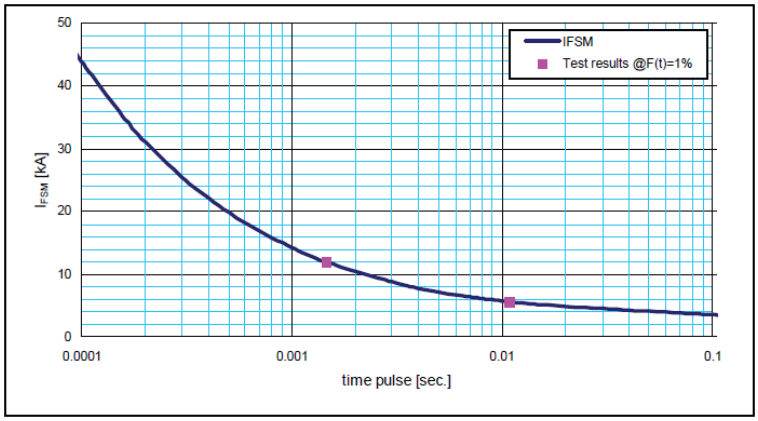



Fig. 4-4 An example of the measured and calculated $I_{FSM}$ capability

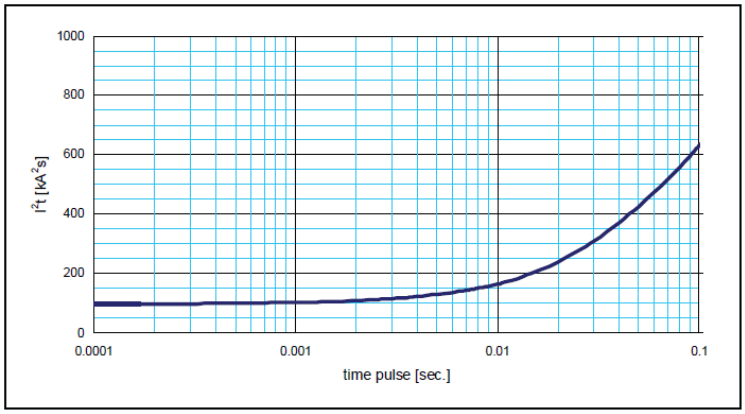



Fig. 4-5 An example of the calculated $I^2t$ capability

# 5. Baseplate Flatness

## 5.1 Baseplate flatness

The shape of the baseplate is an important factor influencing the contact thermal resistance $R_{th(c-s)}$ between the baseplate and the heat-sink. The bigger the residual gap remaining between the baseplate and the heat-sink after mounting, the more thermal compound is needed to fill this gap. As result, the thermal contact resistance $R_{th(c-s)}$ increases. Therefore, it is important to check the baseplate flatness in the mounted condition.
Fig. 5-1 shows an example of convex baseplate flatness under non-mounted condition.

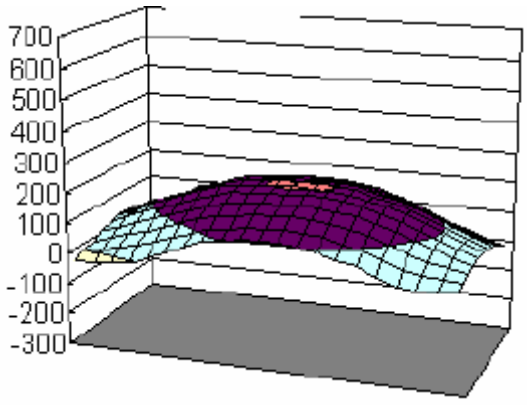



Fig. 5-1 Warping of non-mounted HVIGBT module baseplate

When this module is mounted to a heat-sink by using the recommended mounting procedure, the baseplate edges are pressed down, thus reducing the gap remaining between the baseplate and the heat-sink.

We have special measurement equipment using a perfectly plane mounting plate (see Fig. 5-2). The gap between baseplate and mounting plate is measured at 6 points in the case of 190mm * 140mm footprint modules. The location of each measurement point is in the middle of each AlN ceramic substrate (see Fig. 5-3). The module is mounted to the mounting plate by using the minimum specified mounting torque. Under the described conditions, it is confirmed that the gap does not exceed the maximum specified value.

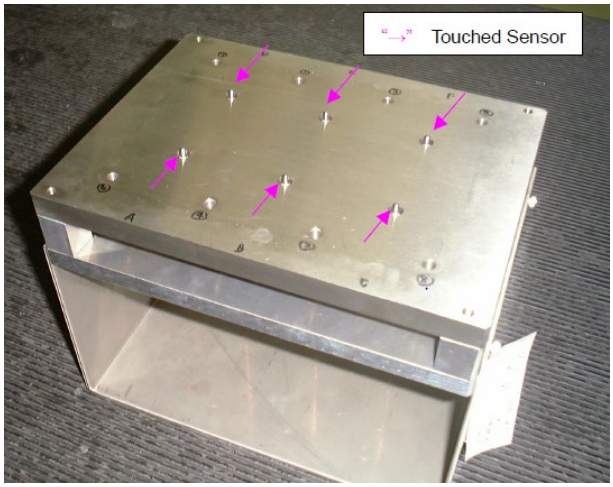



Fig. 5-2 A test jig for measuring baseplate flatness

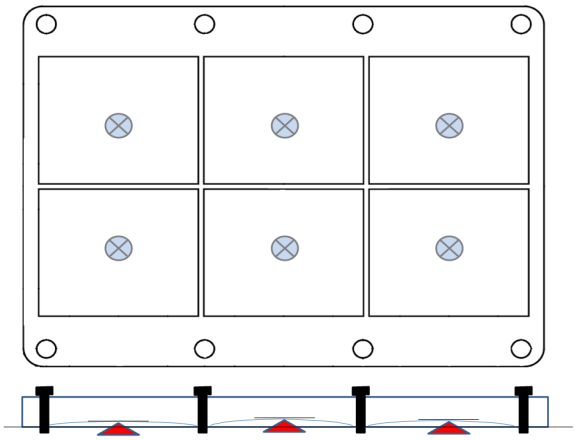


Fig. 5-3 6 measurement points of baseplate flatness

# 6. How to use the HVIGBT

## 6.1 Voltage Rating

The relationship between the voltage rating of HVIGBT modules for inverter use and the AC line voltage of the power supply is

$$[\textbf{Device voltage rating}] > \sqrt{2} \times [\textbf{AC input line voltage}] + [\textbf{Brake voltage increase}] + [\textbf{Surge voltage}] + [\textbf{safety margin}]$$

Table 6-1 shows the relationship of the input line voltage and the voltage rating for HVIGBT modules. The voltage rating of the HVIGBT is recommended to be more than twice the DC link voltage.

Table 6-1: Relationship of the input line voltage and the HVIGBT voltage rating

| Input line voltage | | DC link voltage [V] | Rating voltage of HVIGBT Module | |
|---|---|---|---|---|
| DC input | AC input | | 2 level inverter | 3 level inverter |
| 750 VDC | - | 750 | 1.7 kV | - |
| 1,500 VDC | - | 1500 | 3.3 kV | 1.7 kV |
| 3,000 VDC | - | 3000 | 6.5 kV | 3.3 kV |
| - | 690 VRMS | ~930 | 1.7 kV | - |
| - | 1,000 VRMS | ~1350 | 3.3 kV | - |
| - | 2,300 VRMS | ~3100 | 6.5 kV | 3.3 kV |
| - | 3,300 VRMS | ~4460 | - | 4.5 kV |
| - | 4,160 VRMS | ~5620 | - | 6.5 kV |

## 6.2 Collector Current Rating

The proper selection of an HVIGBT involves two key points. One is that the peak collector current during the operation, including any required overload current, must be within the maximum rating current value. The other is that the IGBT operating junction temperature must always be kept below the maximum rating temperature in all normal operation including any expected motor overload. If the actual current exceeds the rated current, there is a risk of deterioration of IGBT performance, such as a decrease in IGBT life.

Normally, the suggested overload rate of an inverter ranges from 150% to 200%. The nominal operating current should be about 50-60% of the maximum rated IGBT current. In the collector current, $I_C$ , ratings provided in the datasheet are shown in Fig. 6-1. The free-wheel diode is designed to conduct short current pulses. In order to achieve a high efficiency inverter, the duty of the free-wheel diode should be less than that of the IGBT.

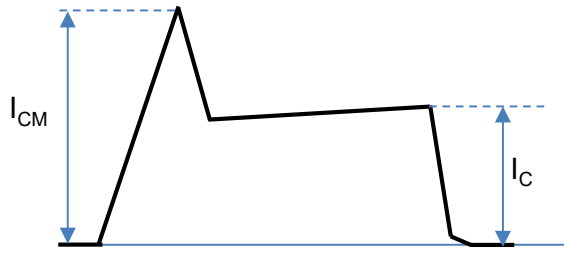



Fig. 6-1 Definition of $I_C$ and $I_{CM}$

## 6.3 Thermal Design

HVIGBT modules will have conduction and switching power losses during operation. Heat is generated because of these losses, which must be conducted away from the power chips and into the environment using a heat-sink. If an appropriate thermal system is not used, the power devices will overheat. Overheating can result in reduced life and premature failure. In many applications, the maximum usable power output of the module will be limited by the system's thermal design.

## 6.4 Estimating Power Losses

The first step in a thermal design is the estimation of total power loss for the IGBTs and diodes. In the power electronic circuits using IGBT modules, the sources of power dissipation are conduction losses and switching losses.

a) IGBT conduction losses

The IGBT conduction losses are losses that occur while the IGBT is on and conducting current. The total power dissipation during conduction is computed by multiplying the on state saturation voltage by the on-state current. In PWM applications the conduction loss should be multiplied by the duty factor to obtain the average power dissipated.

A first approximation of the conduction losses can be obtained by multiplying the IGBT's rated $V_{CEsat}$ by the expected average device current. In most applications, the actual losses will be smaller than the calculated result because $V_{CEsat}$ is lower than the datasheet value at currents less than rated $I_C$.

$$E_{CON} = I_{C(average)} \times V_{CEsat(average)} \times t_w$$

b) IGBT switching losses

The IGBT switching losses are the power dissipated during the turn- on and turn- off switching events. In high frequency, the PWM switching losses can be substantial and have to be considered in thermal design. The most accurate method of determining the switching losses is to plot the IC and VCE waveforms during the switching transition and multiply the waveforms point by point to get an instantaneous power waveform.
Fig. 6-2 shows the area under the power waveform is the switching energy expressed in Joules.

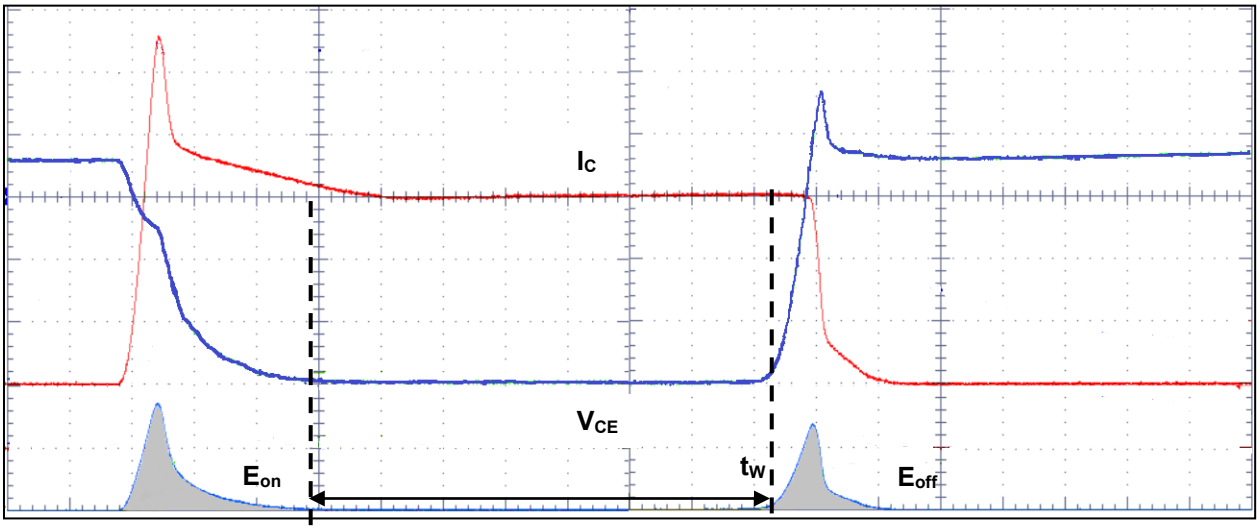



Fig. 6-2 IGBT turn-on and turn-off switching losses

From Fig. 6-2, it can be observed that there are two pulses in the power losses, the turn-on switching energy and the turn-off switching energy. The instantaneous junction temperature rise due to these pulses is not normally a concern because of their extremely short duration. However, the sum of these power losses in an application where the device is repetitively switching on and off at a substantial frequency can be significant.

In cases where the operating current and the applied DC voltage are constant, $E_{on}$ and $E_{off}$ are the same for each turn-on and turn-off event. The average switching power loss can be computed by taking the sum of $E_{on}$ and $E_{off}$ and dividing by the switching period. Noting that dividing by the switching period is the same as multiplying by the frequency results in the most basic equation for the average switching power loss:

$$P_{SW} = f_{sw} \times (E_{on} + E_{off})$$

c) Diode conduction losses

The calculation method for the diode conduction losses is same as that of the IGBT conduction losses. When switching in a circuit with an inductive load, the conduction losses for the free-wheel diode should be considered. The free-wheel diode losses can be approximated by multiplying the datasheet $V_{EC}$ by the expected average diode forward current.

d) Diode switching losses

The calculation method of the diode switching losses is almost same as that of the IGBT switching losses. Energy is dissipated inside the diode during reverse recovery.

## 6.5 VVVF Inverter Loss Calculation

One common application of power modules is Variable Voltage Variable Frequency (VVVF) inverter. In VVVF inverters, PWM is used to synthesize sinusoidal output currents. In this application, because the IGBT current and the duty cycle are constantly changing, estimating power losses is very difficult. The following equations can be used for initial loss estimation in VVVF applications. The actual losses will depend on the temperature, the sinusoidal output frequency, the output current ripple and other factors. Fig. 6-3 and Fig. 6-4 show a typical VVVF inverter circuit and an example of an inverter output waveform respectively.

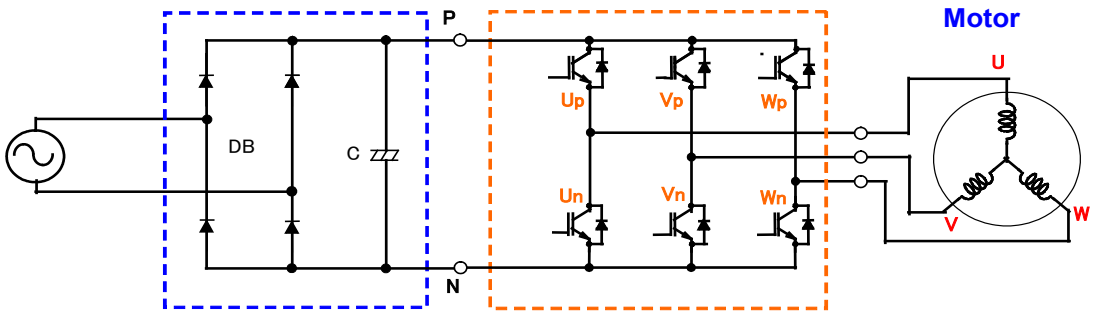



Fig. 6-3 Typical VVVF inverter circuit

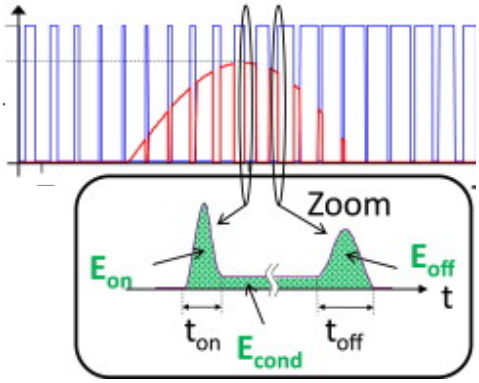



Fig. 6-4 Inverter output waveform

Equations for power loss calculation for sinusoidal inverters;

➢ IGBT loss

1) On-state loss per switching IGBT [where cos Θ = power factor]

$$P_{cond} = I_{C(peak)} \times V_{CEsat} \times \frac{1}{2\pi}\int_0^{\pi} \sin^2 x \cdot \frac{1+\sin(x+\theta)\cdot D}{2}\, dx = I_{C(peak)} \times V_{CEsat} \times (\frac{1}{8} + \frac{D}{3\pi}\cos\theta)$$

2) Switching loss per switching IGBT

$$P_{SW} = (E_{on} + E_{off}) \times f_{SW} \times \frac{1}{2\pi}\int_0^{\pi} \sin x \cdot dx = (E_{on} + E_{off}) \times f_{SW} \times \frac{1}{\pi}$$

3) Total loss per switching IGBT

$$P_{IGBT} = P_{cond} + P_{SW}$$

➢ Diode loss

1) On-state loss per diode

$$P_{cond} = I_{F(peak)} \times V_{EC} \times (\frac{1}{8} - \frac{D}{3\pi}\cos\theta)$$

2) Switching loss per diode

$$P_{SW} = E_{rec} \times f_{SW} \times \frac{1}{\pi}$$

3) Total loss per switching IGBT

$$P_{diode} = P_{cond} + P_{SW}$$

## 6.6 Thermal Calculation

The IGBT and diode chips in the power module have a maximum rated junction temperature. This rating should not be exceeded under any normal operating condition. Good design practice is to limit the worst case maximum junction temperature to the maximum rated junction temperature or less. Reliability can be enhanced by operating the semiconductor junction at lower temperatures. Thermal resistance ($R_{th(j-c)}$) is specified on the power module datasheet for use in thermal calculations to estimate the junction temperature.

Junction temperature is estimated using the following equation.

$$T_j = P \times R_{th(j-c)} + T_c$$

By using the appropriate values of $R_{th(j-c)}$ and P, the above equation can be used to estimate the junction temperature of both the IGBT and the free-wheel diode. For the initial design of heat sink systems, the contact thermal resistance is specified on the datasheet. The contact thermal resistance is the thermal resistance of the module to the heat-sink interface. The specified value assumes that a thermal interface compound such as thermal grease is used. A uniform layer of the non-volatile silicon thermal grease with a nominal thickness of approximately 100μm~ 200μm will give the best results.

The module baseplate temperature can be estimated using the following equation.

$$T_c = P \times (R_{th(c-s)} + R_{th(s-a)}) + T_a$$

*$R_{th(s-a)}$ : Thermal resistance between heatsink and ambient
*$T_a$ : Ambient temperature

The value of $R_{th(c-f)}$ is specified for the entire module. Final thermal analysis should be done using a measured baseplate temperature and total power loss under the worst case condition.

On the other hand, in the case of short or low duty cycle power pulses, the transient thermal impedance curve is given on the datasheet and must be used to calculate the junction temperature rise.

For a power device subjected to a single pulse or very low duty cycle, short duration power pulses, the maximum allowable power dissipation during the transient period can be substantially greater than the steady state dissipation capability. The calculation of the peak transient junction temperature rise depends on the duty factor and the repetition rate of the power pulses. First, consider the power loss as a procession of constant cycles and the constant peak square pulses. In addition, the pulse width and the repetition rate should be such that operating temperature rating ($T_{jop}$) does not exceed the maximum junction temperature ($T_j$). The following equations are for the junction temperature calculation using the transient thermal impedance;

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i \cdot (1 - exp^{-\frac{t}{\tau_i}})$$

$$T_j(t) = \mathrm{P(t)} \cdot Z_{th(j-c)}(t) + T_c(t)$$

## 6.7 Using Melcosim for Thermal Design

The Mitsubishi Power loss simulation tool, Melcosim, simulates the IGBT and free-wheel diode in a 2-level or a 3-level PWM topology with sinusoidal output current as well as several other modulation schemes and topologies.

Melcosim offers a highly accurate estimate of power loss and temperature rise based on data available on the datasheet. The following method is given in order to demonstrates how the power losses and temperature rise output is derived.

1st step: Select a module

2nd step: Select system topology and modulation strategy

3rd step: Input operating conditions (input parameters as below and see Fig. 6-5)
Input parameters: DC-link voltage, Output current, Carrier frequency, Output frequency, Gate resistance, Power factor, Modulation, Duty, Fin or heat sink temperature (just under the chip)

4th step: calculate power losses and temperature rises

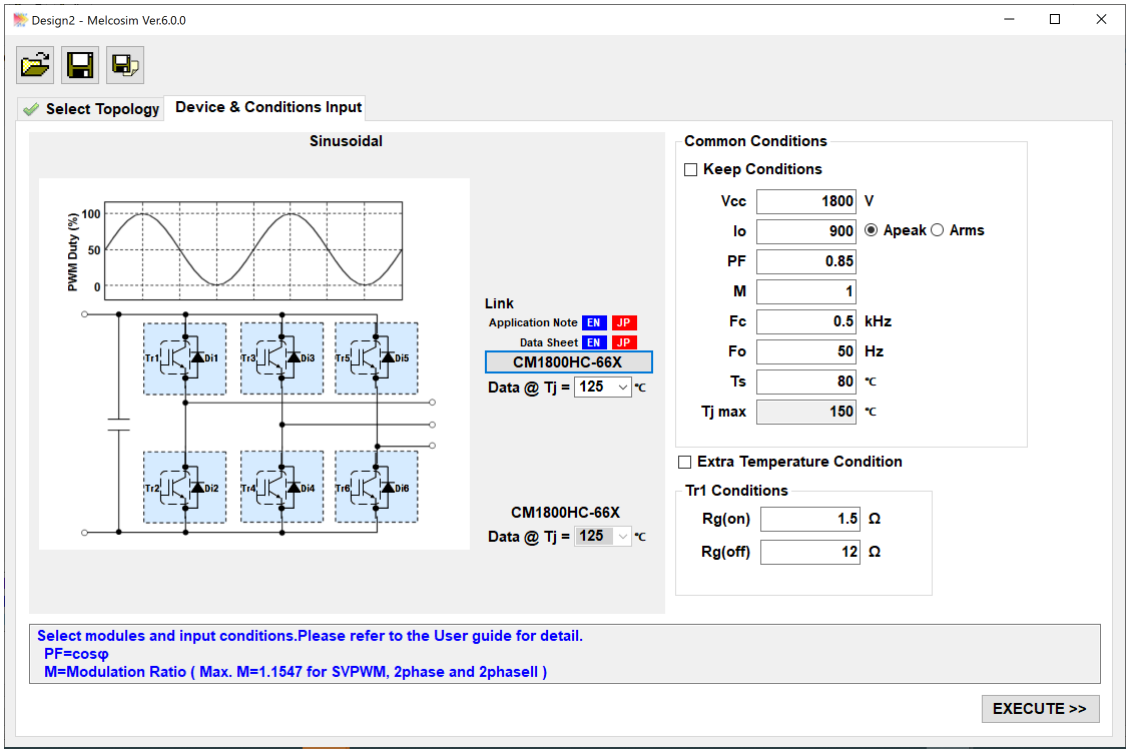



Fig. 6-5 Operation conditions

The calculation results show IGBT and diode losses, $\Delta T_{(j-c)}$, $T_j$, and $T_c$ (Calculation results are as shown as in Fig. 6-6). Additionally, some performance curves can be obtained such as the power loss versus the switching frequency, the output current versus the switching frequency, the junction temperature rise versus the junction temperature, etc.

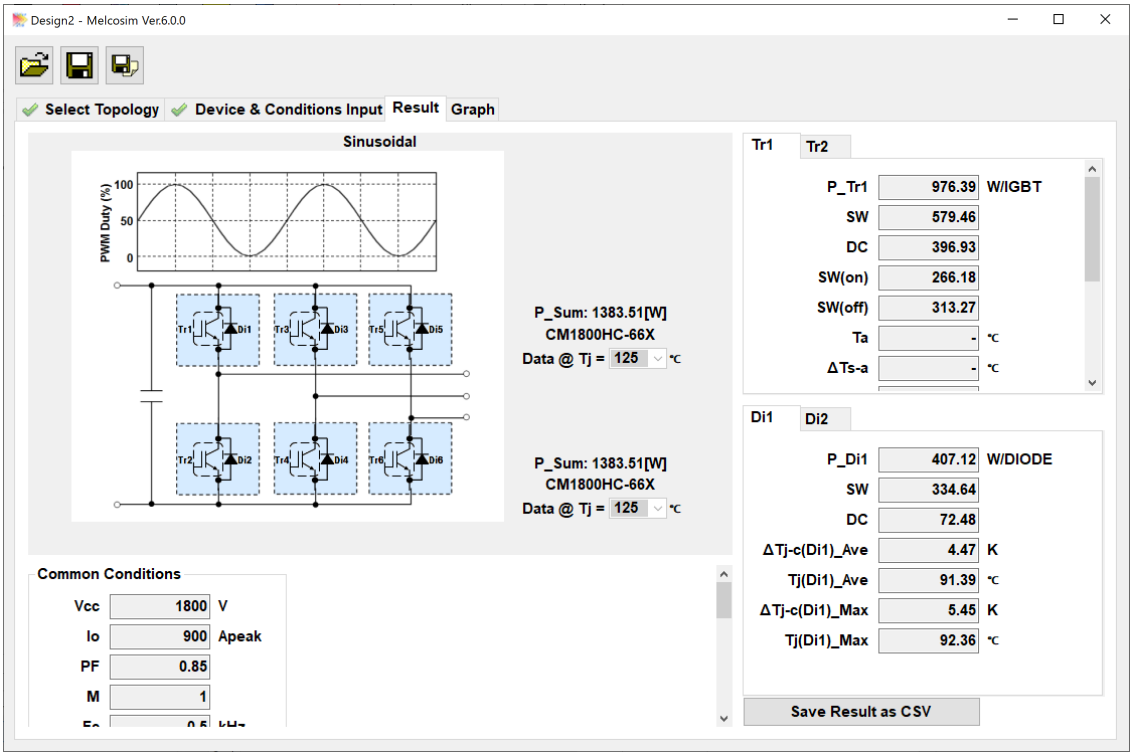



Fig. 6-6 Calculation result example (power losses and temperature rises)

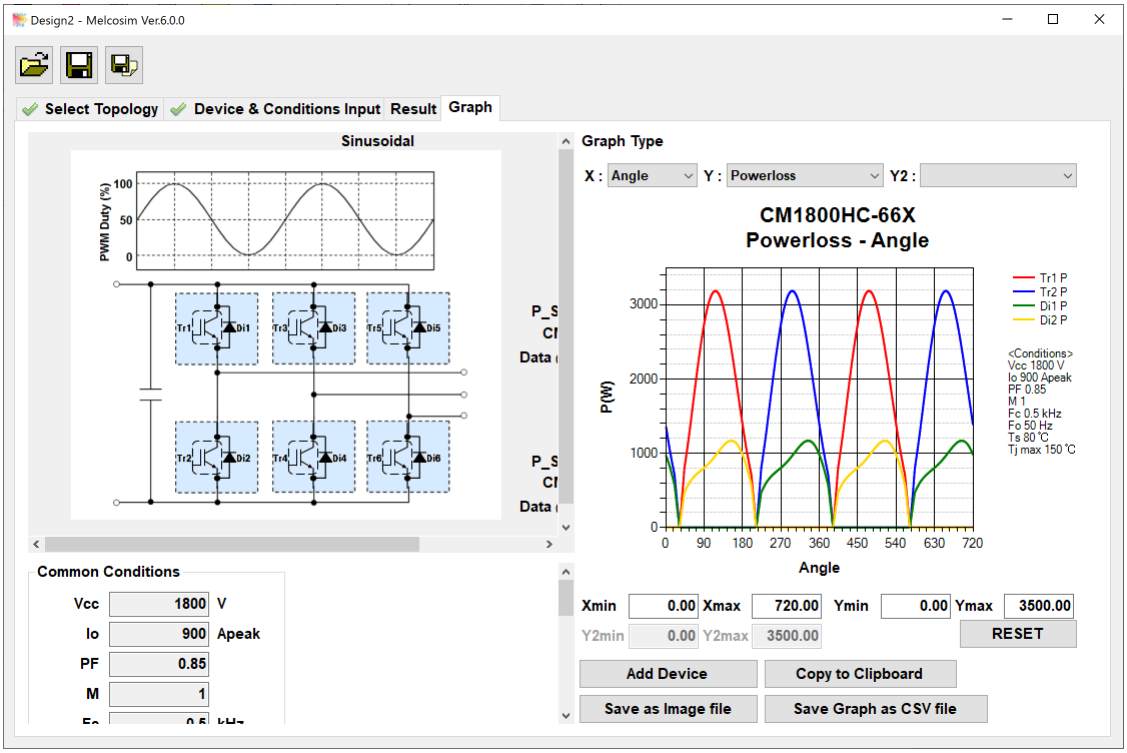



Fig. 6-7 Switching frequency versus power loss

# 7. Gate drive considerations

## 7.1 General Description

The gate driver supplies the power to turn the IGBT module on and off. In order to do so, the gate driver charges the gate of the IGBT up to turn-on gate-emitter voltage (over above $V_{GE(on)}$) or the drive circuit discharges the gate down to turn-off gate-emitter voltage (less than $V_{GE(th)}$). The transition between the two gate voltage levels (turn on gate voltage and turn off gate voltage) requires a certain amount of power to be dissipated in the loop between gate driver and IGBT. The gate driver influences the dynamic behavior of the IGBT and the free-wheel diode.

The following items should be considered in the design of the gate drive:

a) In is necessary that each driver be optically isolated
b) The drive power required depends on the total IGBT gate charge
c) Positive on bias influences the power losses and Short circuit current
d) Reverse off bias influences the power losses and risk of malfunction
e) External series gate resistance influences the SOA and power loss

**a) Optical insulation**

The gate driver must be isolated between the control circuit and the power supply circuit to improve noise immunity and safety. Recently HVICs are being used for the 600V and 1200V IGBTs. This has advantages of controlling the dead time, low cost, and flexibility. However, HVICs to support 1700V and higher class HVIGBTs are not yet available. If the system isn't isolated between the gate driver and the IGBT, when the system is supplied DC link voltage, it will cause gate driver breakdown and system failure.

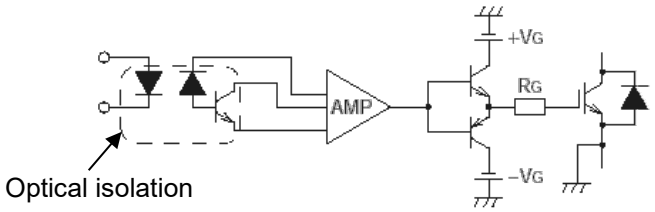



Fig. 7-1 Basic gate drive circuit

**b) Drive power**

The $Q_G$ characteristics must be known to properly design the IGBT gate driver. The IGBT has a MOS gate structure. The MOS gate charges and discharges when the IGBT turns on and turns off. Fig. 2 shows the gate charge characteristics using constant gate current. The gate charge characteristics are used to calculate the gate current values and the necessary amount of power to drive the IGBT. The gate current value can be calculated as the followings.

$$average\ current\ i_G = Q_G \times f_c$$

$$i_G = \frac{+V_{GE} + |-V_{GE}|}{R_G + r_g}$$

Where $V_{GE}$ is the gate voltage; $R_g$ is the gate resistance; $r_g$ is the gate resistance inside the module; $Q_G$ is the amount of the gate charge; and, fc is the switching frequency.

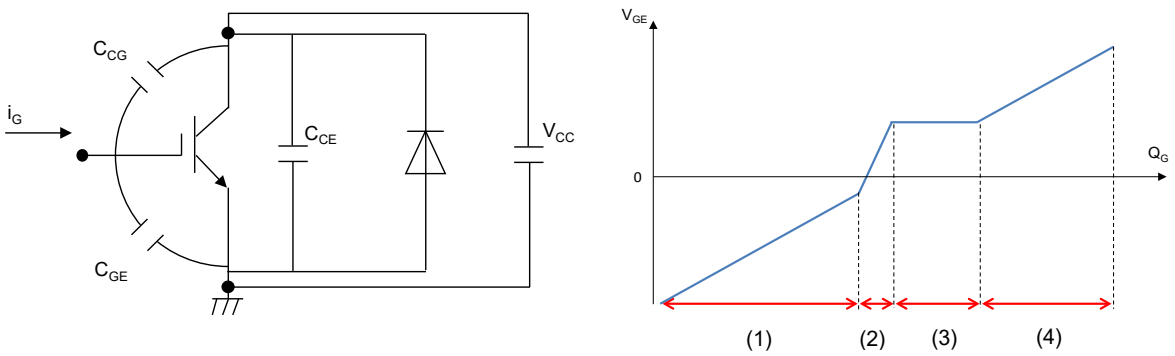



Fig. 7-2 Gate charge characteristics

(1) $i_G$ (gate current) charges parasitic input capacitance $C_{GE}$ and $C_{GC}$.
(2) $i_G$ charges to $C_{GE}$ creating conduction channel
(3) ”Miller effect”
(4) $i_G$ charges to $C_{GE}$ and $C_{GC}$.

### c) Positive bias $+V_{GE}$

Normally, the recommended positive gate bias is +15V. In any case, its magnitude must never exceed the maximum rated gate-emitter voltage. Positive bias influences the following characteristics:

- Short circuit limited current: Higher $+V_{GE}$ means higher current.
- Collector-emitter saturation voltage: Higher +VGE means lower saturation voltage.
- Turn-on di/dt: Higher $+V_{GE}$ causes higher di/dt.
- Turn-on switching energy: Higher $+V_{GE}$ means lower switching energy.

On one hand Also, the positive bias influences the opposite side free-wheel diode’s reverse recovery. It must be confirmed that the diode’s operation remains within its RRSOA.

### d) Reverse bias $-V_{GE}$

Normally, our recommended reverse gate bias is -15V. Lower bias means lower turn-off time and turn-off switching energy. In any case, it must never exceed the minimum rated gate-emitter voltage. In addition, to avoid exceeding the withstand gate voltage of the IGBT during a surge, the optimal reverse bias voltage is smaller than -5V.

### e) Gate resistance

The gate resistance, $R_G$, given in the switching characteristics on the datasheet is the minimum recommended value. The datasheet also gives performance curves as a function of $R_G$. The gate resistance has to be optimized based on actual operating conditions.

Notice 1: Smaller gate resistor means higher di/dt and higher surge voltage. The surge voltage must never exceed the maximum voltage rating.

Notice 2:

- Gate drive connected with wires must be a tightly twisted pair with wire length as short as possible to avoid gate oscillation and induced noise.
- Direct connection of the gate drive PCB to the IGBT auxiliary terminals is better and is preferred over a wired connection.

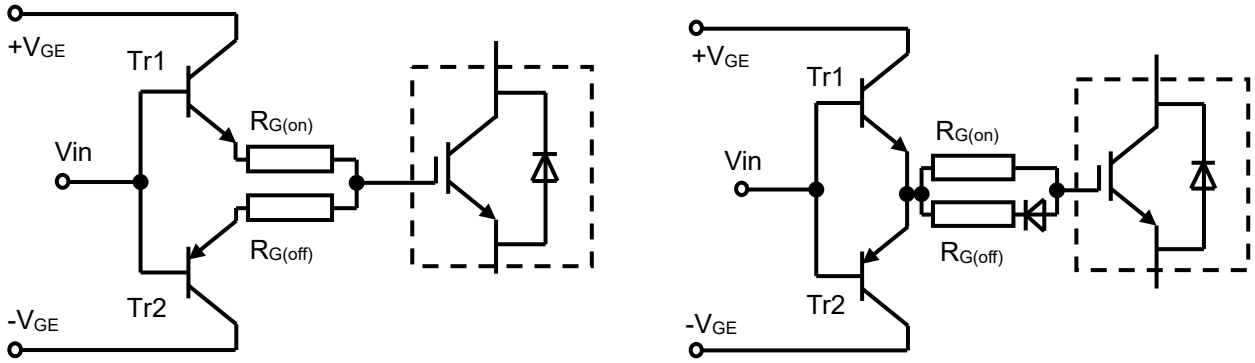



Fig. 7-3 Examples of gate drive circuit design

## 7.2 Gate Resistance $R_G$

The gate resistance strongly influences the switching behavior. Special points of focus are power losses and SOA. In general, the effect of $R_G$ is shown on the datasheet under the heading of switching losses.

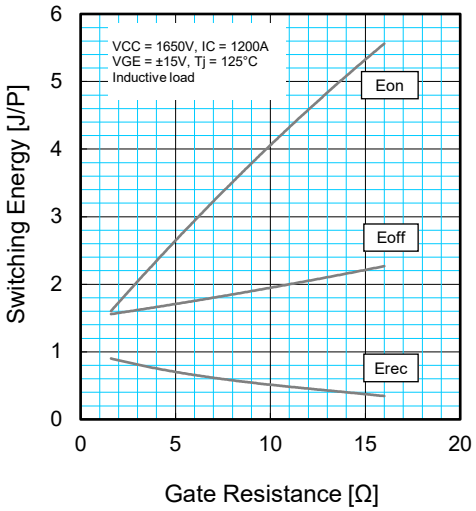



Fig. 7-4 Switching energy versus gate resistance curve for the CM1200HC-66H

**Decreasing $R_{G(on)}$:**
The IGBT has faster switching speed and lower turn-on switching losses as $R_{G(on)}$ is decreased. At the same time, during reverse recovery, free-wheel diode RRSOA attention must be paid to the faster di/dt and increasing $P_{rr}$.

Table 7-1 Effects of decreasing turn-on gate resistance

| Items | Effects |
|---|---|
| $t_{don}$ | Shorter |
| $E_{on}$ | Lower |
| di/dt | Higher |
| $P_{rr}$ | Higher |

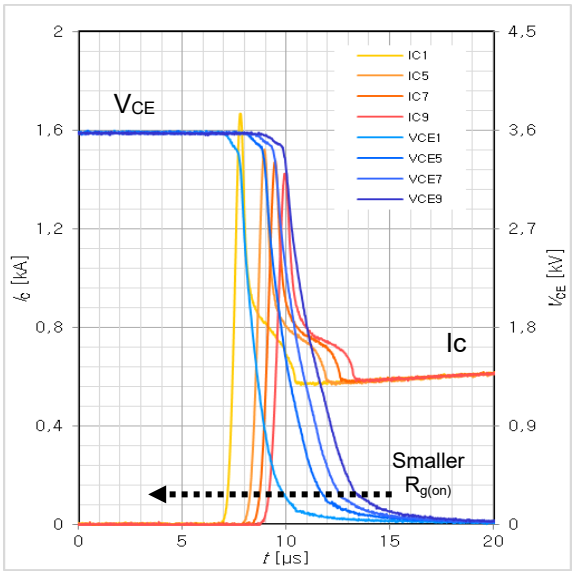



Fig. 7-5 Turn-on switching waveforms of a 6.5kV module ($R_{G(on)}$ dependency)

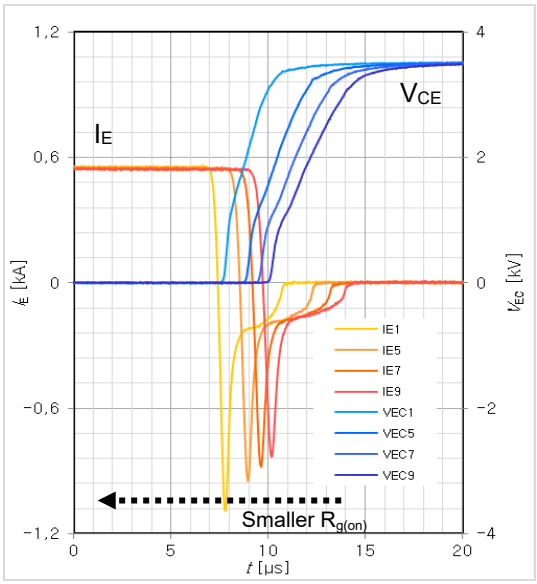



Fig. 7-6 Reverse recovery waveforms of a 6.5kV module ($R_{G(on)}$ dependency)

**Decreasing $R_{G(off)}$:**
The IGBT has faster switching speed and lower turn-off switching losses as $R_{G(off)}$ is decreased. At the same time, attention must be paid to RBSOA due to faster dv/dt and higher surge voltage when operating at maximum turn-off switching conditions.

Table 7-2 Effects of decreasing turn-off gate resistance

| Items | Effects |
|---|---|
| $t_{doff}$ | Shorter |
| $E_{off}$ | Lower |
| dv/dt | Higher |
| $V_{CE(max)}$ | Higher |

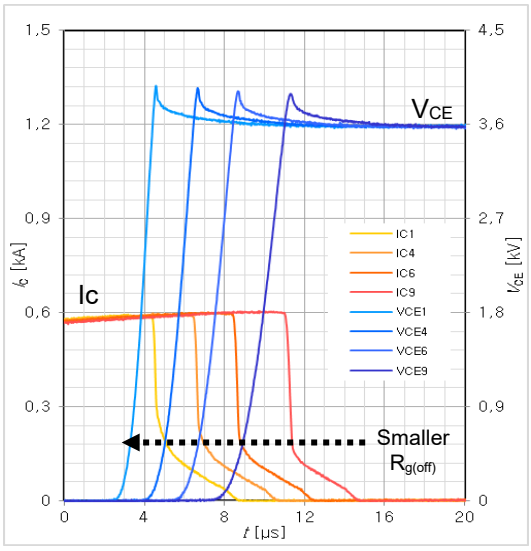



Fig. 7-7 Turn-off switching waveforms of a 6.5kV module ($R_{G(off)}$ dependency)

## 7.3 $C_{GE}$ Effect

One of the methods of decreasing switching losses is the addition of an external capacitor $C_{GE}$ between gate and emitter while decreasing the external gate resistance $R_G$. The capacitor takes up additional charge coming from the Miller capacitance. The gate voltage charge necessary to reach the threshold voltage is increased. Fig. 7-8 shows the turn-on switching waveform. The effect on turn-on switching energy is more effective pronounced than for the other switching energies. Simultaneously, during reverse recovery, $P_{rr}$ is also reduced.

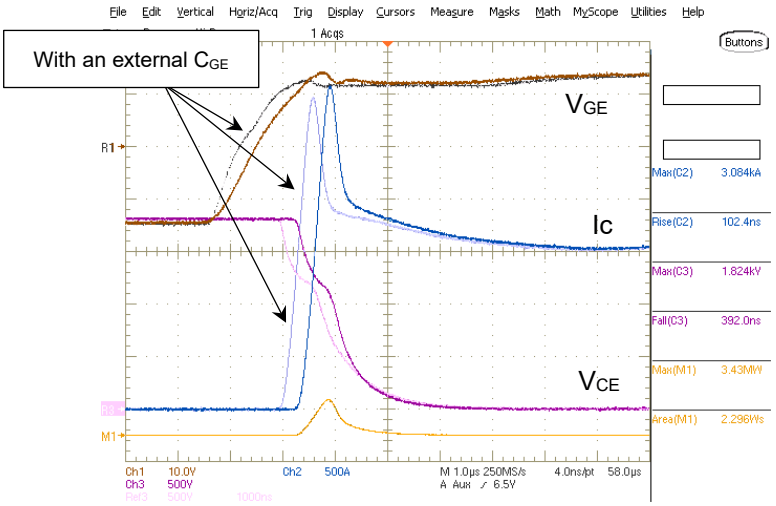



Fig. 7-8 $C_{GE}$ effect on turn-on behavior

## 7.4 Gate Drive with Active Clamping

The maximum instantaneous collector-emitter voltage, $V_{CE(max)}$, during turn off must be kept safely below $V_{CES}$. Several options can be considered to reach the objective of keeping the maximum collector-emitter voltage within the RBSOA limit:

Reducing the DC-link inductance $L_s$
Using additional snubber circuit
Increasing the turn-off gate resistance $R_{G(off)}$
Gate drive with active clamping

One of the options for keeping safely the maximum collector-emitter voltage is using a gate driver with active clamping. The basic circuit diagram for the active clamping model is shown in Fig. 7-9.

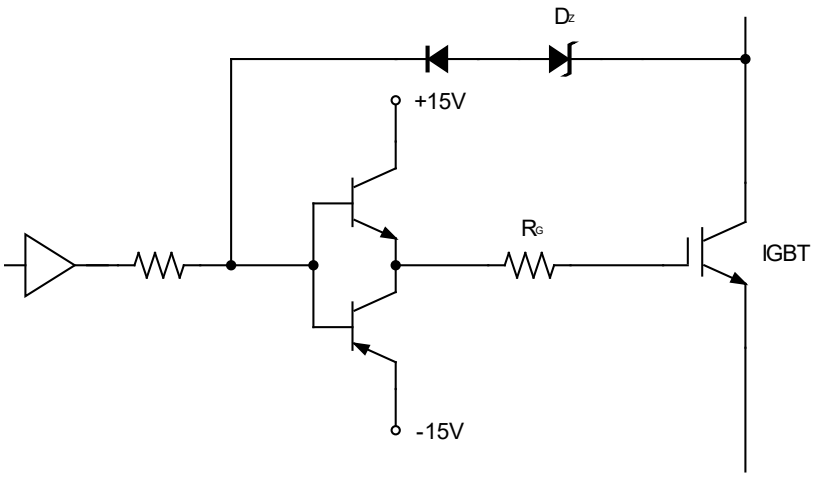



Fig. 7-9 Basic diagram of the active clamping circuit

Active clamping is activated when the collector-emitter voltage during turn off reaches the zener voltage of $D_Z$. As result the turn-off di/dt is reduced and thus the overvoltage spike is limited. Rate of the zener voltage is selected below the maximum rated collector-emitter voltage of the IGBT. An example waveform of CM2400HC-34N (1.7kV, 2400A, N-series module) with active clamping operation by using Power Integrations gate driver 1SD536F2- CM2400HC-34N is shown in Fig.7-10

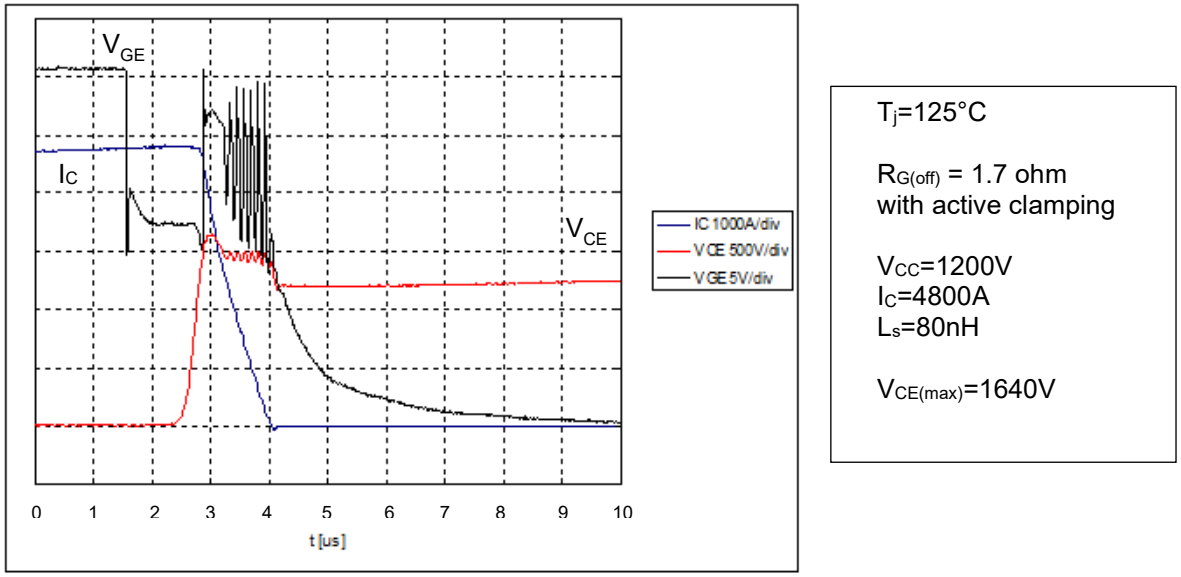



Fig. 7-10 Turn-off switching waveform with the active clamping circuit

## 7.5 Switching Speed

HVIGBTs have an operational frequency limit due to power dissipation limits of the internal series gate resistors. Fig. 7-11 shows the internal series gate resistances connected to the parallel IGBT chips in the module. The gate current, $I_G$, passes through on the external gate resistance and divides between the internal gate resistances and repeats charge and discharge at the operational frequency.

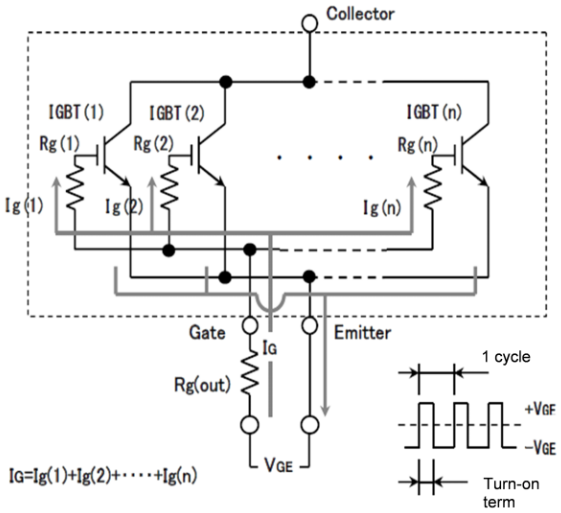



Fig. 7-11 HVIGBT internal circuit diagram

Waveforms of the gate current and gate-emitter voltage during a pulse cycle are shown in Fig. 7-12. Gate current flows only at the beginning of the turn on and turn off. The value of the internal current flowing to each gate depends on the external gate resistance and the limitation of the the gate power capability depends on the gate current and the frequency.

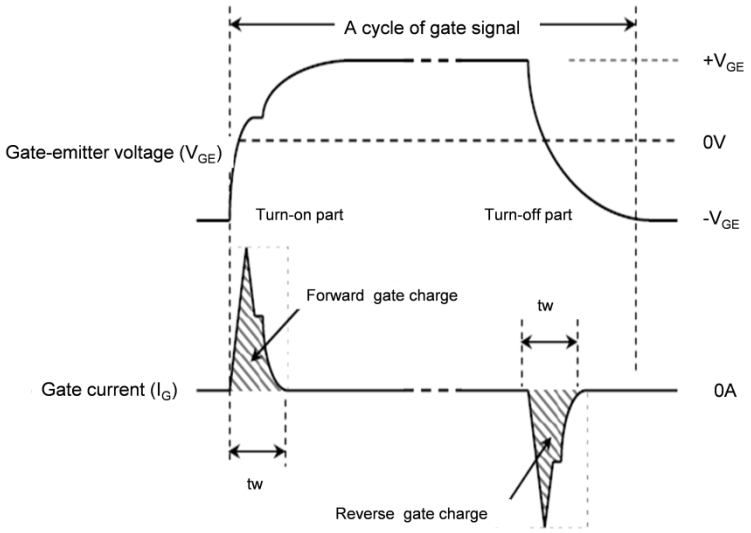



Fig. 7-12 Gate current waveform in a cycle of gate signal

## 7.6 Dead Time

In order to prevent the arm short circuit, a dead time ($t_{dead}$) between high and low side input turn-on and turn-off signals is required to be included in the gate drive control logic system. The dead time needs to be set longer than the difference between IGBT switching times:

$$t_{dead} > t_{off(max)} - t_{on(min)}$$

$$t_{off} = t_{doff} + t_f$$

$$t_{on} = t_{don} + t_r$$

The dead time is measured directly at the IGBT input terminals. If the switching time is longer than $t_{dead}$ due to increased gate resistance, $R_G$, it would be necessary to increase $t_{dead}$. If a shorter dead time is desired, the photo coupler should be changed or the gate resistance should be decreased.

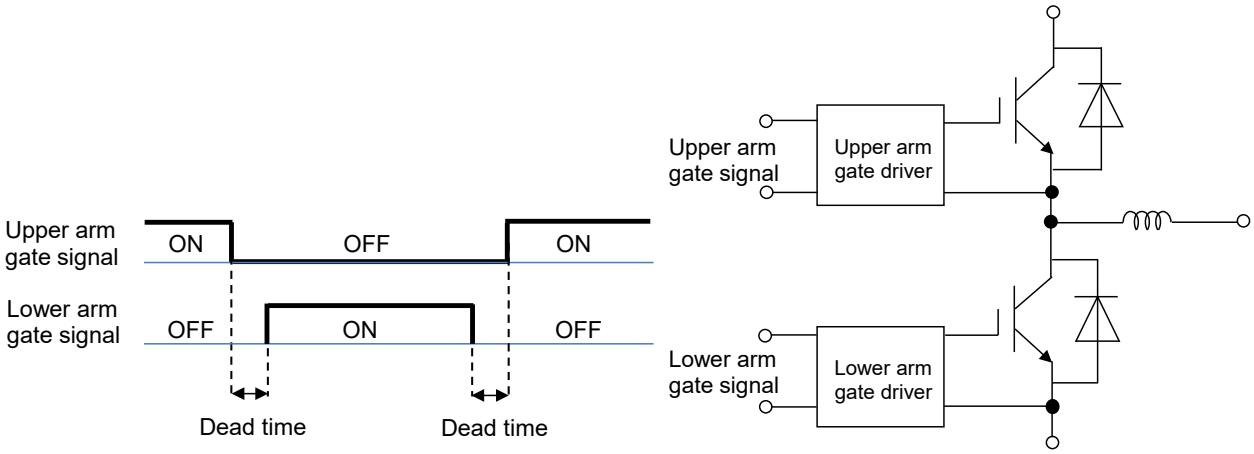



Fig. 7-13 Dead time pulse sequence

# 8. Snubber Circuit

## 8.1 Snubber Circuit

A snubber circuit is usually used in combination with IGBT modules to protect the IGBT or FWDi from transient over voltages which occur during switching events of the transistor. The transient over voltages arise due to stray inductance in the DC link construction. If the stray inductance is too high and it is not possible to stay within the switching SOA, it is preferable to modify the DC link construction to reduce the stray inductance or to use a drive with an active clamping function. If neither option is possible, a snubber capacitor can be used.
The basic function of the snubber capacitor can be described using Fig. 8-2. Fig. 8-1 shows the simplified circuit of a dual IGBT module with a parallel connected main DC link capacitor ($C_{DC\ link}$), and a snubber capacitor ($C_S$). Their respective related parasitic stray inductances, $L_{S1}$ and $L_{S2}$, are also shown in Fig. 8-1.

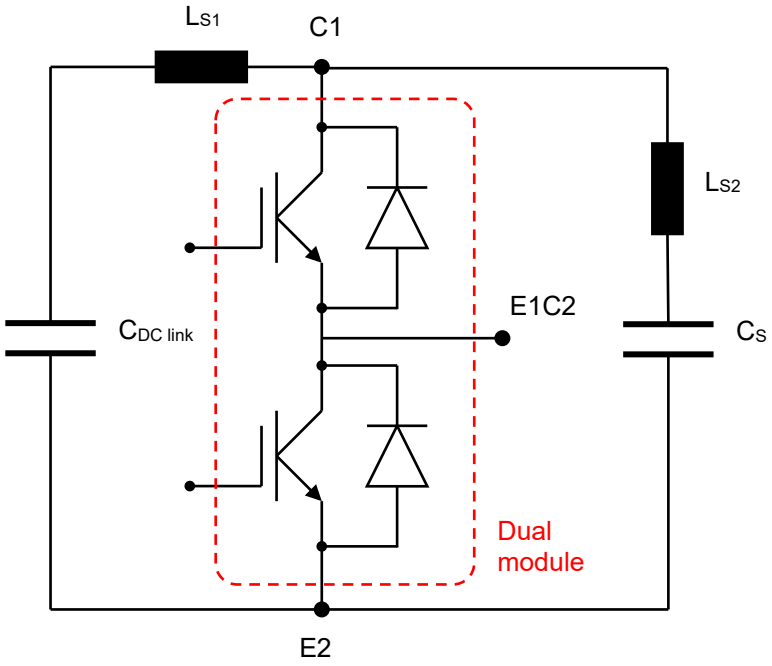



Fig. 8-1 A snubber circuit with a dual IGBT module

The overvoltage transients can appear during turn-off events of IGBT. The overvoltage spike on the IGBT without a snubber capacitor can be calculated by the following equation:

$$\Delta V_{CE1}=L_{S1}\cdot\frac{\Delta I}{\Delta t}$$

The overvoltage spike can be reduced by adding a snubber capacitor under the condition of $L_{S2}<L_{S1}$. In that case, the overvoltage spike $(\Delta V_{CE2})$ could be reduced to:

$$\Delta V_{CE2}=L_{S2}\cdot\frac{\Delta I}{\Delta t}$$

$$\Delta V_{CE1}>\Delta V_{CE2}$$

The snubber capacitance ($C_S$) should be connected as close as possible to the module to minimize its size. The required snubber capacitance can be calculated using the following formula formula:

$$\frac{1}{2}C_S\cdot(\Delta V_{CE3})^2=\frac{1}{2}L_{S1}\cdot{I_O}^2$$

$$C_S=\frac{L_{S1}\cdot{I_O}^2}{{\Delta V_{CE3}}^2}$$

In the above equation, $L_{S1}$ is the DC link inductance, $I_O$ is the maximum turn-off current, $V_{CC}$ is the maximum DC link voltage, and $\Delta V_{CE3}$ is the maximum allowable overvoltage for the maximum DC link voltage.

The typical collector current and the collector-emitter voltage waveforms during a turn-off event are shown in Fig.8-2. The dotted red line shows collector emitter voltage without snubber; the solid red line shows the collector emitter voltage with a snubber capacitor. The gray line is the collector current waveform. It is observed that the collector-emitter peak voltage is significantly reduced by using a snubber capacitor.

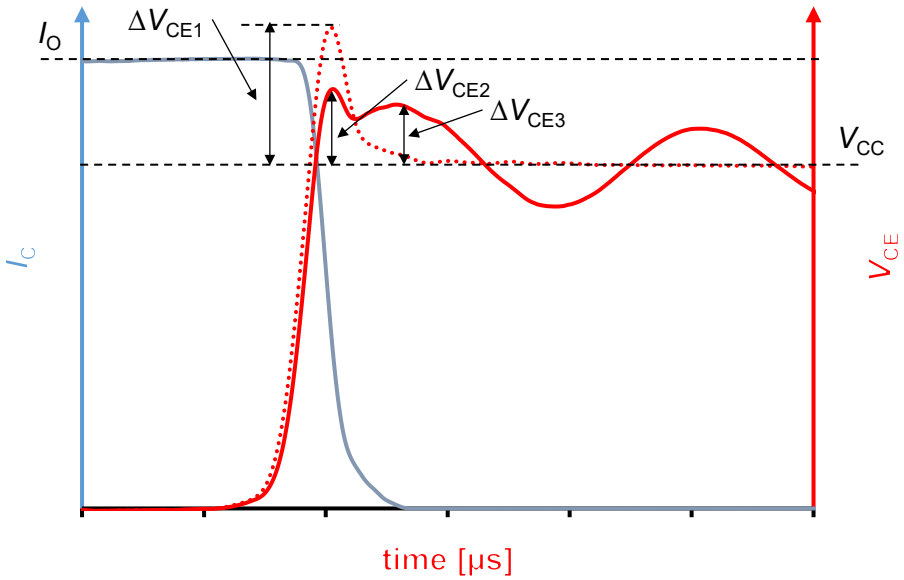



Fig. 8-2 Turn-off switching behavior with snubber circuit

Disadvantages of using a snubber capacitor include: increase of cost, the system losses; the component count; and the reduction of reliability in the system. A snubber capacitor is usually used for the 1.7kV dual module. Snubber use in combination with higher voltage rated modules is not recommended due to the single configuration and the lower switching speed.

## 8.2 Bus Bar

The main bus bar parameters are its resistance, stray inductance, and capacitance. The physical form of the bus bar is different and depends on the construction of the inverter. The main design target of the bus bar is to have enough sufficient current capacity, isolation capability, and to have very low stray inductance between the capacitor bank and the switching IGBT modules. Low stray inductance can be realized by f.e. using a laminated, wide structure. The importance of low inductance increases directly proportional to the level of current being switched.

The influence of the current loop in the bus bar on the control circuit and IGBTs must be considered and proofed by testing.

For paralleling of IGBT modules, the bus bar construction must be symmetrical and designed for well uniform current distribution.

# 9. Mounting Recommendations

Correct mounting of the HVIGBT to the heat-sink is very important crucial for cooling and reliability.
The mounting process has two main steps:

- ✓ Thermal grease application
- ✓ Mounting to the heat-sink

## 9.1 General Description

Heat-sink flatness should be in the range of ±100μm (over the contact area (see Fig. 9-1)).
Important: There should be no steps on the heat-sink surface in the area where the module makes contact. The heat sink surface finish should be 12.5μm or less(peak to peak). The main function of the thermal grease is filling any gaps between the heat-sink surface and the module baseplate surface, thus reducing the thermal contact resistance, $R_{th(c-f)}$.

Furthermore, the grease prevents corrosion of the contact interface surface. The grease must have stable characteristics over the entire expected operating temperature range so that its properties do not change during the operational lifetime. The grease must have long-term stability; this means that the properties of grease must not change during the operational lifetime. If there is concern that the grease life is declining, reapply before heat dissipation is reduced. A torque wrench must be used for tightening the mounting screws with the specified torque.

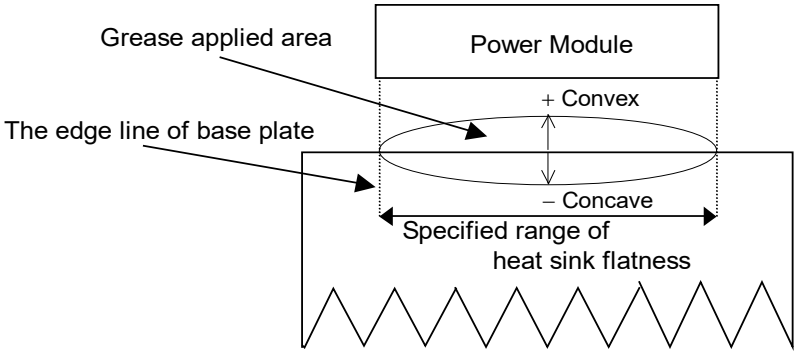



Fig. 9-1 Flatness of heat-sink

## 9.2 Application of Thermal Grease

It is recommended that thermal grease be applied to the baseplate uniformly using screen printing technology (see Fig. 9-2).The recommended thickness of grease is 100μm ~ 200μm. The necessary amount of grease can be calculated based on the desired grease thickness, the baseplate area, and the grease density by using the formula equation below.

$$Amount\ of\ grease\ [g] = Thickness\ of\ grease\ D_{(c-s)}\ [cm] \times Baseplate\ area\ [cm^2] \times Density\ of\ grease\ [g/cm^3]$$

The application method of thermal grease is shown in Fig.9-2.

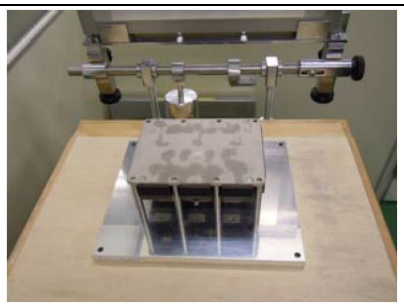
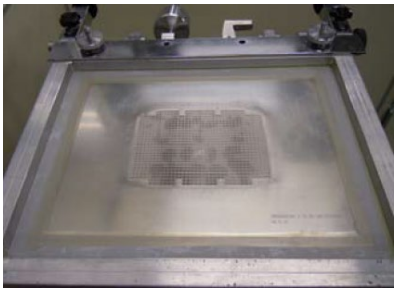
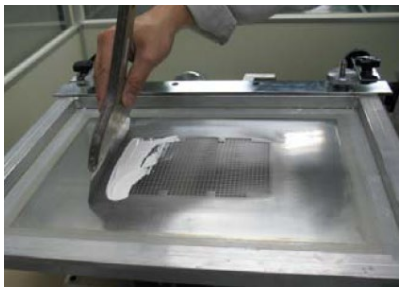
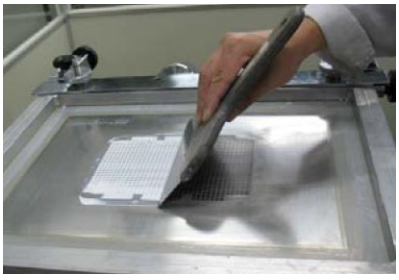
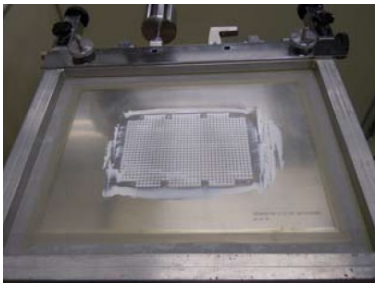
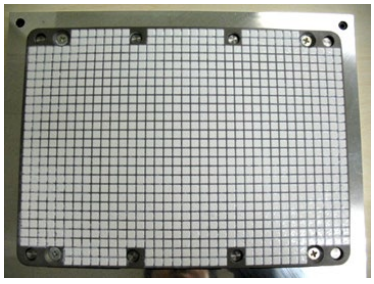
| | | |
|---|---|---|
|  |  |  |
| Step 1:<br>Set the HVIGBT module in the screen printing jig | Step 2:<br>Set the screen printing mask to the correct baseplate location | Step 3:<br>Put the necessary amount of grease on one side of the mask |
|  |  |  |
| Step 4:<br>Spread the grease in a single stroke over the mask (don't repeat if possible) to ensure uniform thickness | Step 5:<br>Confirm that the surface is covered completely with the grease | Step 6:<br>Remove the screen printing mask from the HVIGBT module |

Fig.9-2 Application method of thermal grease

For recommended grease types, please refer to Table.9-1.
When selecting the grease the following items should be considered:

- Ease of application
- Thermal conductivity
- Chemical compatibility (Silicone grease or non-silicone grease)
- Long term stability (e.g. pumping out durability)

Please confirm the suitability of the selected grease for your application conditions.

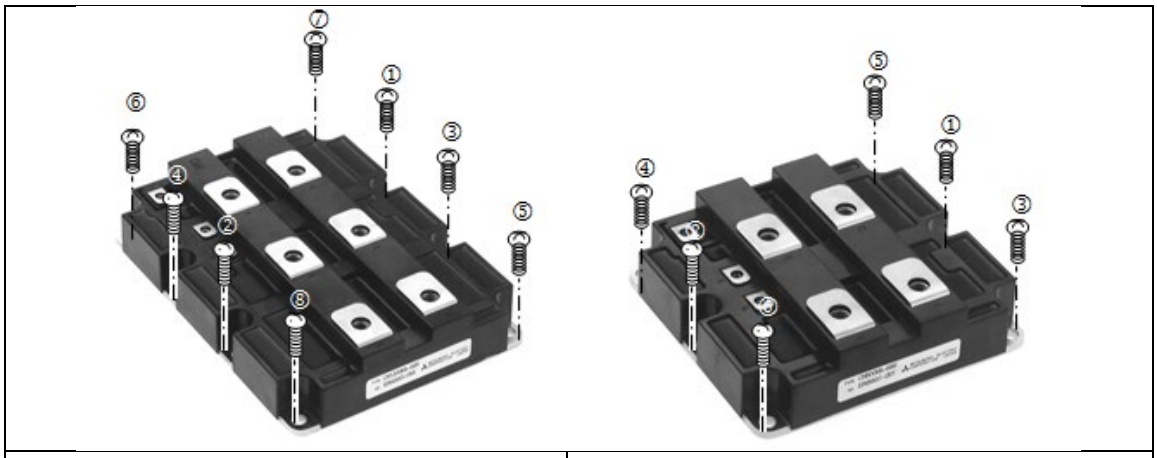
Table 9-1 Recommended grease types

| Manufacturer | Type number | Note | URL |
|---|---|---|---|
| Shin-Etsu Chemical Co., Ltd. | G-747, G-765, G-777 | - | https://www.shinetsu.co.jp/en/ |
| ELECTROLUBE | HTC, HTCP | Non-Silicone | https://electrolube.com/ |
| Momentive | TIG210BX | - | https://www.momentive.com/en-us |
| Dow Corning | DOWSIL 340 | - | https://www.dow.com/en-us/ |
| Wakefield | 120 Series | - | https://wakefieldthermal.com/ |

## 9.3 Mounting

When mounting the HVIGBT to a heat sink, the module can be damaged or degraded if a sudden torque ("one side tightening") is applied at only one mounting hole. In this case, the mechanical stress is applied to the ceramic isolation substrate and chips inside the module. In order to avoid this problem, we recommend the mounting method below. The screws should be tightened by following the numbering order.

Please follow the recommended using a two-step tightening:
First step (Temporary tightening): the 20-30% specified mounting torque
Second step (Final tightening): the 100% specified mounting torque

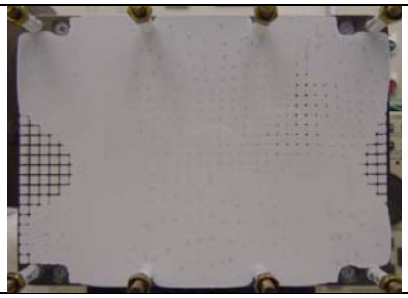



| Eight-point mounting type<br>Temporary tightening<br>①→②→③→④→⑤→⑥→⑦→⑧<br>Final tightening<br>①→②→③→④→⑤→⑥→⑦→⑧ | Six-point mounting type<br>Temporary tightening<br>①→②→③→④→⑤→⑥<br>Final tightening<br>①→②→③→④→⑤→⑥ |
|---|---|

Fig. 9-3 Mounting order of the screws to the heat-sink

**Confirmation test**
Uniform spreading of the grease has been confirmed by using a special transparent acrylic mounting plate (see Fig. 9-4). The result is as below in Fig. 9-5. After temporary tightening, the grease was not yet uniformly distributed. After final tightening, the grease is spread uniformly over the whole baseplate area.

Fig.9-4 A HVIGBT module mounted on an acrylic plate




| After temporary tightening | After final tightening |
|---|---|

Fig. 9-5 Conditions of spreading grease

## 9.4 Handling Precautions & Storage

Semiconductors are sensitive about environment (such as electrical, mechanical stress and temperature…). If you operate unsuitable handling and storage, may lead to damage of HVIGBT modules. Please pay attention to the following our recommendations.

**During transit**

- The shipping cartons cases are designed to keep the modules in the proper orientation keeping correct direction. Putting them upside down, leaning them, or giving subjecting them to uneven stress may cause the terminals to be deformed or the module cases to be damaged.
- Throwing or dropping the cartons cases might may cause the modules to be damaged.
- Wetting the carton cases may cause the breakdown of the HVIGBT modules during operating. Also, has shipping inspection report. Prevent exposure to rain and snow.

**Storage**

- We recommend temperature and humidity in the ranges 5 to 35 °C and 45 to 75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.

**Long term storage**

- When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior. Rechecking the electrical characteristics is recommended after long term storage.

**Surroundings Environment**

- Keep modules away from places where water, liquids, or organic solvents, may attach to them directly or where corrosive gas, explosive gas, fine dust, or salt, etc. may exist. They might cause serious problems.

**Static electricity**

- IGBT chips with a MOS gate structure and are ESD (Electrical Static Discharge) sensitive are used for the HVIGBT modules. Please keep the following notices to prevent modules from being damaged by static electricity.

Excessive voltage applied between the gate and the emitter due to the ESD of human bodies and packaging may damage or destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possible and quick dissipation of the charged electricity.

*Containers that charge static electricity easily should not be used for transit or and for storage.
*Terminals should be always be shorted by conductive wire, tape, or foam parts.
*Do not touch terminals with bare hands.
*During assembly and receiving inspection of the HVIGBT, always earth ground the equipment and the human body. It is recommended to cover the work bench and its surrounding floor with earthed grounded conductive mats.
*We should be noted that devices may be damaged by the static electricity charged to a printed circuit board if the gate to emitter of the circuit board is open.
*If using a soldering iron, earth its tip must be grounded.

Precaution when the gate to emitter is open
* When the control (gate and emitter) terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction.
*Short the gate and emitter terminals before removing a module from a system.

# 10. Series Connection

This section is a proposal concerning two series connection of HVIGBT Modules for high power electronics application.
In such applications series connection operation should only be considered when the highest voltage module available is not large enough. Use of a single HVIGBT module rather than smaller series module is recommended because it eliminates concerns about static and dynamic voltage balance among the series connection modules. With proper attention to circuit design and module selection can be reliably operated in series. The following sub-sections outline the basic requirements and considerations for series operation of single HVIGBT modules.

## 10.1 Static voltage balance

a) Series connected modules should be considered collector cutoff current ($I_{CES}$). And, it is necessary to connect the balance resistance for static voltage balance. The balance resistance Rs can be calculated by the following formula.

$Rs < (nEs-Em) / [ (n-1)x\Delta I_{CES} ]$
$P = Erms^2 / Rs$ $\Delta I_{CES}$ : $\Delta I_{CES}$ between IGBT1 and IGBT2

b) Under static off state the junction temperature has influence on voltage sharing. Temperature differences between series connection modules are also a factor because of the resulting effect on collector cutoff current ($I_{CES}$).
Modules should be mounted on the heat sink near to each other with cooling arranged to maintain uniform base plate temperatures between series connection modules.

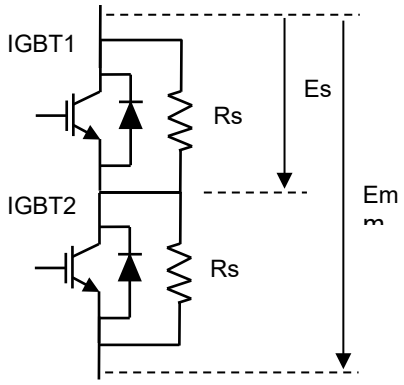



Fig. 10-1

## 10.2 Dynamic voltage balance

It is very important that turn-on, turn-off switching timing of two modules be matched for the dynamic voltage balance.

a) It is effective to make them match the turn-on, turn-off delay time of two modules for the voltage balance.
b) Difference between gate drive wirings may result in Imbalance switching and voltage imbalance.
The output impedance of gate drive circuit has influence on voltage balance. High impedance consisting of gate resistance and stray inductance of drive circuit may raise switching speed difference at turn-on or turn-off and increase voltage imbalance.

- Use short tightly twisted wires of equal length.
- Avoid running a gate drive circuit parallel to the main circuit.

*Please replace two HVIGBT modules connected in series operation when the module failed.

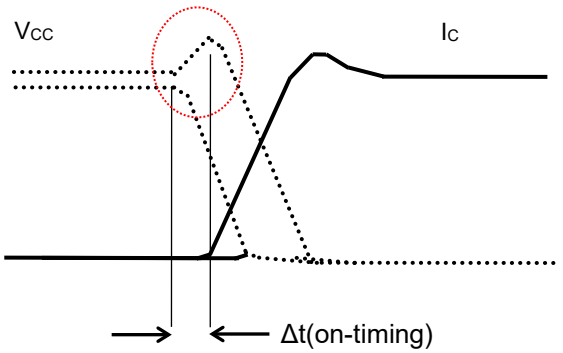



Fig. 10-1 Voltage Imbalance at turn-on

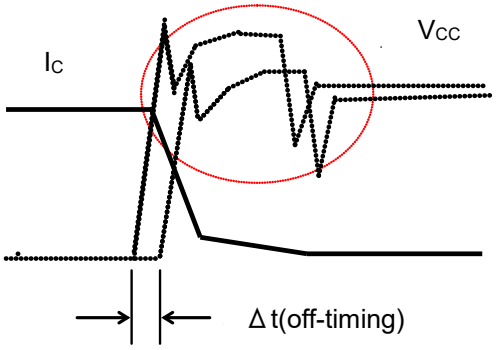



Fig. 10-2 Voltage Imbalance at turn-off

# 11. Parallel Connection

Mitsubishi HVIGBT modules can be connected in parallel for applications requiring very high currents. In such applications parallel operation should only be considered when the highest current module available is not large enough. Use of a single large HVIGBT module rather than smaller parallel module is recommended because it eliminates concerns about static and dynamic current balance among the paralleled devices.
With proper attention to circuit design and device selection several modules can be reliably operated in parallel. The following sub-sections outline the basic requirements and considerations for parallel operation of single HVIGBT modules.

Table 11-1: IGBT Module Parallel Operation, Current Sharing

Factors related to current sharing and their effect.

| | | Categories of Current Sharing | | | |
|---|---|---|---|---|---|
| | | IGBT Switching | | Steady State | |
| Factors Effecting Current Sharing | | Turn-on | Turn-off | di/dt = 0 | di/dt ≠ 0 |
| Device Characterization | $\Delta V_{CE}$(SAT) | X | X | ● | X |
| | Δ Temperature | ● | ● | ● | X |
| Main Circuit Wiring Inductance | ΔL (Supply to Device) | ● | ∂ | X | X |
| | ΔL (Total Loop Including Load) | X | X | X | ● |
| Driver Wiring | Driver to Device Wiring Length Diff. | ● | ● | X | X |
| | Output Impedance of Driver | ● | ● | X | X |

● - Relation Exists  X - No Relation  ∂ - Relation Ambiguous or Weak

## 11.1 Static current balance

Table 11-1 outlines the factors influencing parallel operation of HVIGBT modules. Under static on state or DC operating conditions the collector to emitter saturation voltage($V_{CE(sat)}$) and junction temperature have the biggest influence on current sharing. To achieve reliable and consistent static current balance devices should be mounted on the heat sink near to each other with cooling arranged to maintain uniform base plate temperatures between paralleled modules.
A good general design guideline is to maintain a base plate temperature difference between paralleled devices of 15 degree C or less. Parallel connected devices should be selected with matched $V_{CE(sat)}$.
Fig. 11-1 shows how the imbalance shown in Fig. 11-2 is derating ratio parallel operation. For example, in the case of 3300V H-series, the current imbalance of 2 parallel connection is about 8% at $\Delta V_{CE(sat)}$ =0.25V(this is recommended value).

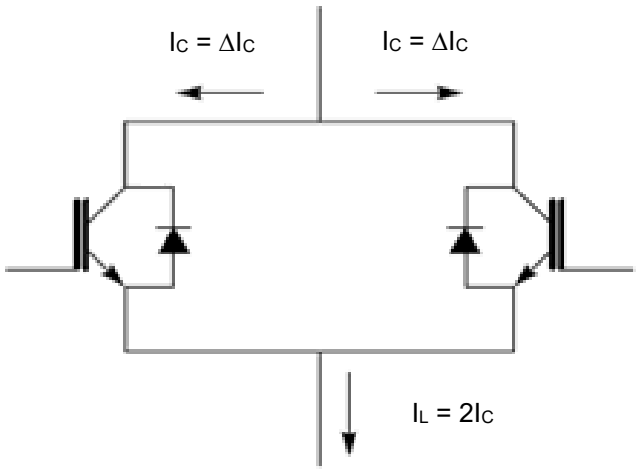



Fig.11-1 Circuit Showing the Definition of Current Imbalance

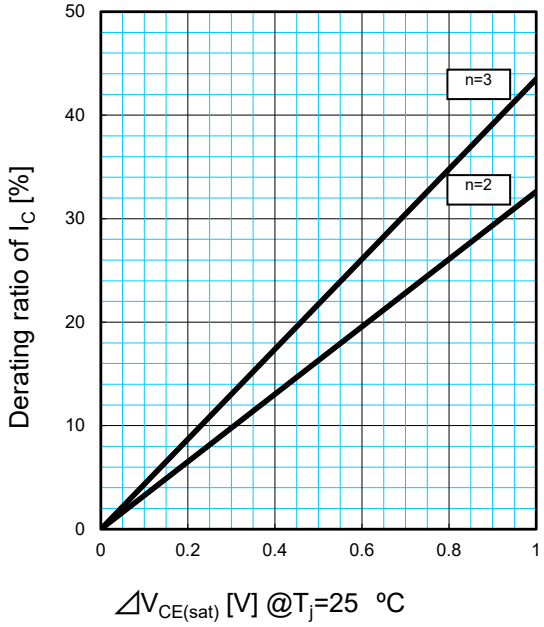



Fig.11-2 Circuit Showing the Definition of Current Imbalance

## 11.2 Dynamic current balance

Matching $V_{CE(sat)}$ is effective for maintaining good static steady state current balance. This matching also helps some with turn off current balance because of the fundamental inverse relationship of fall time and saturation voltage. However, gate drive conditions and power circuit layout have by far the greatest impact on dynamic current balance between paralleled devices. The application circuit of HVIGBT modules should be connected with a short, low impedance symmetric connection in order to minimize the current imbalance.

■ **Current Imbalance factors and notes**

① Device characteristics

a) On-state Voltage Difference
Under static on state (di/dt=0) the collector to emitter saturation voltage $V_{CE(sat)}$ has influence on current sharing.

b) Temperature Difference
Under static on state (di/dt=0) the junction temperature has influence on current sharing.
Temperature differences between paralleled modules are also a factor because of the resulting effect on delay time.

* Power loss imbalance due to instantaneous transient current imbalance is very small. (See Fig.11-3)

Devices should be mounted on the heat sink near to each other with cooling arranged to maintain uniform base plate temperatures between paralleled modules.

② Main Circuit Layout: (See Fig.11-4)
Difference of the inductance in the power circuit between the main supply capacitors and devices may result in current imbalance at the moment of turn-on or turn-off switching.

An asymmetric connection can result in current imbalance at the moment of turn-on or turn-off switching. In order to minimize the current imbalance, circuit connection should be low inductance symmetric.

③ Gate Drive Wiring: (See Fig.11-4,11-5)

1) Difference between gate drive wirings may result in Imbalance switching and current imbalance.
2) The output impedance of gate drive circuit has influence on current balance. High impedance consisting of gate resistance and stray inductance of drive circuit may raise switching speed difference at turn-on or turn-off and increase current imbalance.

Use short tightly twisted wires of equal length.
Avoid running a gate drive circuit parallel to the main circuit.
* Please replace all HVIGBT modules connected in parallel operation when the module failed.

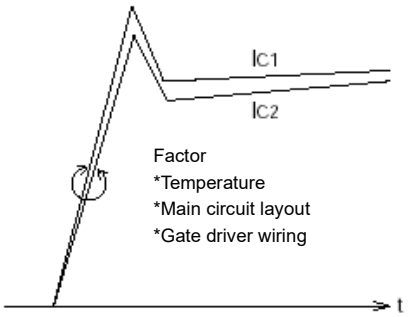



Fig.11-4
Circuit Showing the Definition of Current Imbalance

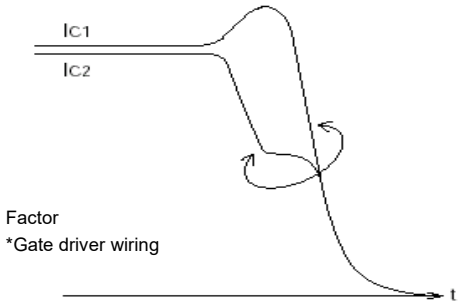



Fig.11-5
Circuit Showing the Definition of Current Imbalance

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