

PV-IPM Application Note

Dec. 2012

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PV-IPM Feature, Product Line-up

1.PV-IPM Feature

A small, decentralized power supplies such as the photovoltaic generation, wind power generation, and fuel cells are spreading from the rise of environmental problems. In addition, the spread of a domestic photovoltaic generation system and the fuel cell system will be expected in the future. Because the voltage to which these generate electricity is DC, it is necessary to convert it into AC to use it at home.

The device for the DC-AC conversion is a power conditioner, and the power device is used for it. Efficiency is requested in the power conditioner, and the power device with low loss is requested. It is IPM for the photovoltaic generation to have satisfied such a demand.

Features

Integration of 5th generation trench chip (CSTBT™) achieves lower saturation voltage

Equipped with newly developed control IC

Using small package as same outer dimensions as L-series IPM

The single phase output inverter circuit and the chopper circuit are built into IPM
(type4: no chopper circuit, type5: chopper circuit*1, type6: chopper circuit*2)

Applications

Power conditioner for Photovoltaic generation and other small capacity generation system.

2.Product Line-up

Single phase inverter circuit (type4)

Screw type package

PM50B4LA060

PM75B4LA060

Pin type package

PM50B4LB060

PM75B4LB060

Single phase inverter circuit and 1 chopper circuit (type5)

Screw type package

PM50B5LA060

PM75B5LA060

Pin type package

PM50B5LB060

PM75B5LB060

Single phase inverter circuit and 2 chopper circuit (type6)

Screw type package

PM50B6LA060

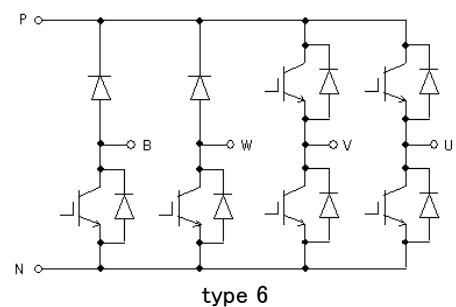
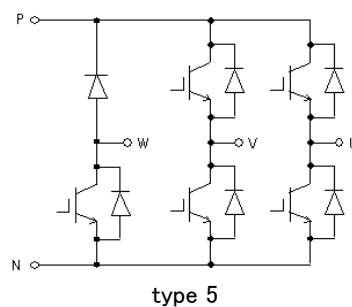
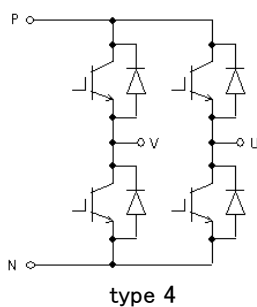
PM75B6LA060

Pin type package

PM50B6LB060

PM75B6LB060

Internal circuit



Package



Screw type package



Pin type package

Term Explanation

3. Term Explanation

General 1

Symbol	Parameter	Definition
IGBT	Insulated Gate Bipolar Transistor	
FWDi	Free Wheeling Diode	Anti-parallel to the IGBT
IPM	Intelligent Power Module	
t _{dead}	Dead Time	Low side turn-off to high Side turn-on & High Side turn-off to low side turn-on
IPM Motor	Interior Permanent Magnet Motor	
(PC)	Photo-Coupler	
PC	Programable Controller	
CMR	Common Mode Noise Reduction	The maximum rise ratio of common mode voltage
CM _H		The maximum rise ratio of common mode voltage at the specific high level
CM _L		The maximum rise ratio of common mode voltage at the specific low level
CTR	Current Transfer Ratio	the ratio of the output current to the input current

General 2

Symbol	Parameter	Definition
T _a	Ambient Temperature	Atmosphere temperature without being subject to thermal source
T _c	Case Temperature	Case temperature measured at specified point

Absolute maximum Ratings

Symbol	Parameter	Definition
V _{CEs}	Collector-Emitter Blocking Voltage	Maximum Off-state collector-emitter voltage with gate-emitter shorted
I _C	Continuous Collector Current	Maximum collector current – DC
I _{CM}	Peak Collector Current Repetitive	Peak collector current, T _j ≤ 150°C
I _E	Continuous Diode Current	Maximum diode current – DC
I _{EM}	Peak Diode Current Repetitive	Diode peak current, T _j ≤ 150°C
P _C	Power Dissipation	Maximum power dissipation, per device, T _c = 25°C
T _j	Junction Temperature	Allowable range of IGBT junction temperature during operation
T _{stg}	Storage Temperature	Allowable range of temperature within which the module may be stored or transported without being subject to electrical load.
V _{iso}	Isolation Voltage	Minimum RMS isolation voltage capability applied electric terminal to base plate, 1 minute duration
-	Mounting Torque	Allowable tightening torque for terminal and mounting screws

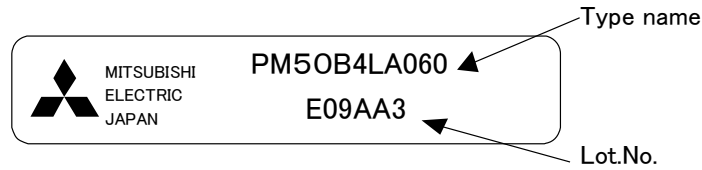
※I_E and I_F are using by the difference of the connection and so on like the following figure.

Electrical Characteristics

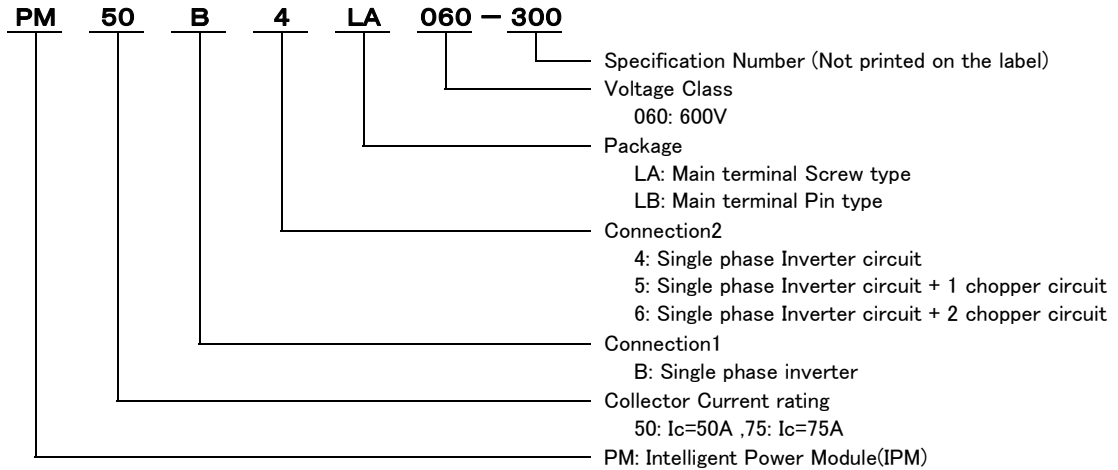
Symbol	Parameter	Definition
I _{CEs}	Collector-Emitter Leakage Current	I _C at V _{CE} = V _{CEs} , V _{GE} = 0V
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _{CE} at I _C = rated I _C and V _{GE} = 15V
t _{c(on)}	Turn-on Delay Time	Time from I _C = 10V to V _{CE} = 10% of final value
t _{c(off)}	Turn-off Delay Time	Time from V _{CE} = 10% of final value to I _C = 10% of final value
E _{on}	Turn-on Switching loss	Energy dissipated inside the IGBT during the turn-on of a single collector current pulse. Integral time starts from the 10% rise point of the collector current and ends at the 10% of the collector-emitter voltage point.
E _{off}	Turn-off Switching loss	Energy dissipated inside the IGBT during the turn-off of a single collector current pulse. Integral time starts from the 10% rise point of the collector-emitter voltage and ends at the specified low collector current point, x% of I _C .
t _{rr}	Diode Reverse Recovery Time	Time from I _C = 0A to projection of zero I _C from I _{rr} and 0.5 × I _{rr} points with I _E = rated I _C .
V _{EC}	Forward Voltage Drop of Diode	V _{EC} at -I _C = rated I _C
R _{th}	Thermal Resistance	The rise of junction temperature per unit of power applied for a given time period
R _{th(j-c)}	Thermal Resistance, Junction to Case	I _C conducting to establish thermal equilibrium
R _{th(c-f)}	Thermal Resistance, Case to Fin	I _C conducting to establish thermal equilibrium lubricated

4. Numbering System

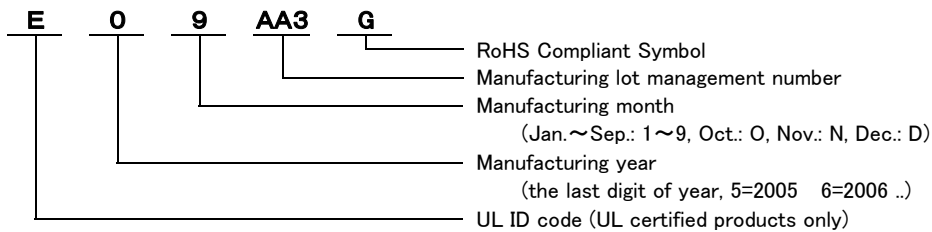
Label)



Type Name)

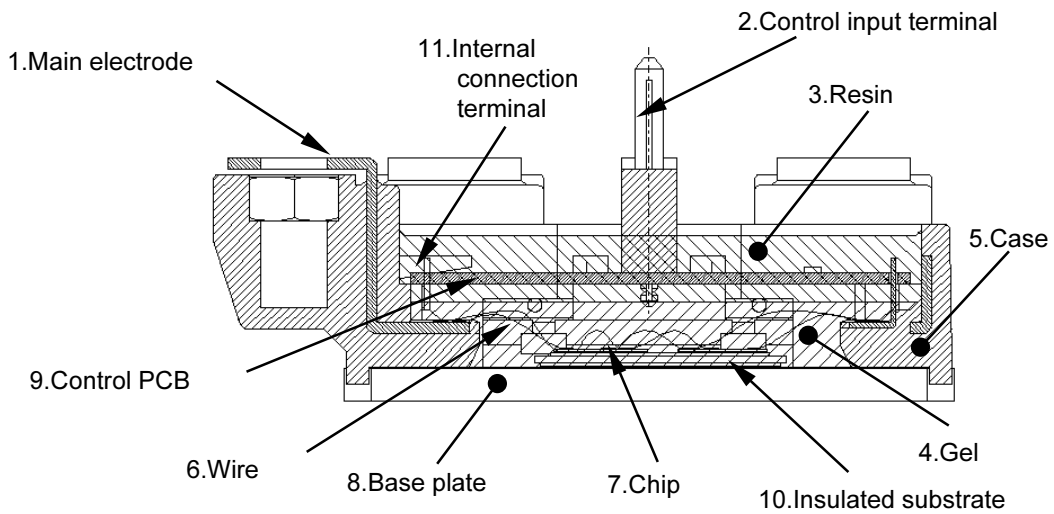


Lot Number)



5. Structure

ex.) Screw type Package



	Part	Quality of the material	UL Flame class
1	Main electrode	Copper plated with nickel	
2	Control input terminal	Brass plated with gold	
3	Resin	PPS resin	UL 94-V0
4	Gel	Epoxy	UL 94-V0
5	Case	Silicone	
6	Wire	PPS resin	UL 94-V0
7	Chip	Aluminum	
8	Base plate	Silicon	
9	Control PCB	Copper	
10	Insulated substrate	Glass epoxy	UL 94-V0
11	Internal connection terminal	Ceramic*	
		Copper plated with nickel	


Note of Insulated substrate

* : All about its structure, material, thickness, and manufacturer is the same as S-series IPM.
S-series IPM has UL(Underwriters Laboratories Inc) Yellow Card #80276 (file. #80271).

Correct and Safety Use of Power Module

6. Correct and Safety Use of Power Module

Unsuitable operation (such as electrical, mechanical stress and so on) may lead to damage of power modules. Please pay attention to the following descriptions and use Mitsubishi Electric's IGBT modules according to the guidance.

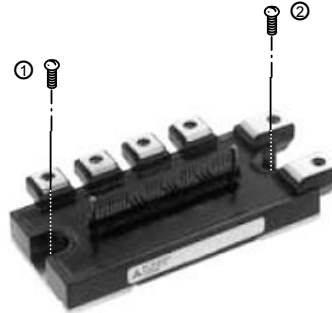
 <h1 style="margin: 0;">Cautions</h1>	
During Transit	<ul style="list-style-type: none"> • Keep shipping cartons right side up. If stress is applied by either placing a carton upside down or by leaning a box against something, terminals can be bent and/or resin packages can be damaged. • Tossing or dropping of a carton may damage devices inside. • If a device gets wet with water, malfunctioning and failure may result. Special care should be taken during rain or snow to prevent the devices from getting wet.
Storage	<ul style="list-style-type: none"> • The temperature and humidity of the storage place should be 5~35°C and 45~75% respectively. The performance and reliability of devices may be jeopardized if devices are stored in an environment far above or below the range indicated above.
Prolonged Storage	<ul style="list-style-type: none"> • When storing devices more than one year, dehumidifying measures should be provided for the storage place. When using devices after a long period of storage, make sure to check the exterior of the devices is free from scratches, dirt, rust, and so on.
Operating Environment Flame Resistance	<ul style="list-style-type: none"> • Devices should not be exposed to water, organic solvents, corrosive gases, explosive gases, fine particles, or corrosive agents, since any of those can lead to a serious accident. • Although the epoxy resin and case materials are in conformity with UL 94-V0 standards, it should be noted that those are not non-flammable.
Anti-electrostatic Measures	<p>(1) Precautions against the device rupture caused by static electricity</p> <p>Static electricity of human bodies and cartons and/or excessive voltage applied across the gate to emitter may damage and rupture devices. The basis of anti-electro static build-up and quick dissipation of the charged electricity.</p> <ul style="list-style-type: none"> * Containers that are susceptible to static electricity should not be used for transit nor for storage. * Gate to emitter should be always shorted with a carbon cloth or the like until right before a module is used. Never touch the gate terminals with bare hands.
Anti-electrostatic Measures	<ul style="list-style-type: none"> * Always ground the equipment and your body during installation (after removing a carbon cloth or the like. It is advisable to cover the workstation and it's surrounding floor with conductive mats and ground them. * It should be noted that devices may get damaged by the static electricity charged to a printed circuit board if the gate to emitter of the circuit board is open. * Use soldering irons with grounded tips. <p>(2) Precautions when the gate to emitter is open</p> <ul style="list-style-type: none"> * Voltage should not be applied across the collector to emitter when the gate to emitter is open. * The gate to emitter should be shorted before removing a device from a unit.

Correct and Safety Use of Power Module

⚠ Cautions

Mounting

When mounting a module on a heat sink, a device could get damage or degrade if a sudden torque ("one side tightening ") is applied at only one mounting terminal, since stress is applied on a ceramic plate and silicon chips inside the module. Shown in Fig.1 is the recommended torquing order for mounting screws.



(a) Two-Point Mounting Type
 Temporary tightening ①→②
 Final tightening ②→①

*:Temporary tightening torque should be set at 20~30% of maximum rating.

Also, care must be taken to achieve maximum contact (i.e. minimum contact thermal resistance) for the best heat dissipation.)

The flatness of a heat sink where a module is mounted (ref.Fig.2) should be as follows. Also, the surface finish should be less than Rz12s.

Copper base plate module: $-100\mu\text{m}\sim+100\mu\text{m}$

Thermal compound with good thermal conductivity should be applied evenly about Aluminum base plate modules: $-100\mu\text{m}\sim+200\mu\text{m}$ on the contact surface of a module and a heat sink.

Heat sink flatness: Less than ± 20 micrometers on a length of 100mm
 /Less than 10 micrometers of roughness

Thermal grease thickness: $+50\sim+100\mu\text{m}$

Grease on the contact surface prevents the corrosion of the contact surface. However, use the kind of grease that has a stable characteristic over the whole operating temperature range and does not change its properties for several years.

A torque wrench shall be used in tightening mounting screws and tighten screws to the specified torque. Excessive torquing may result in damage or degradation of a device.

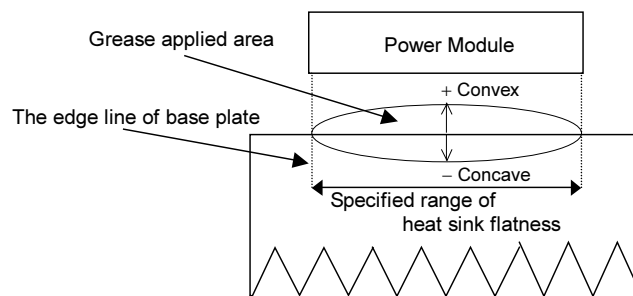


Fig.2 Heat Sink Flatness

7. Reliability

7-1. Introduction

It has only been somewhat over 30 years since semiconductor devices such as rectifier diodes, thyristors, and transistors gained widespread acceptance for use in industrial machinery and consumer appliances, but during that period the reliability standards for these devices have made rapid advances.

In equipment where high reliability is a must, failure rate of the semiconductor devices must range from 10 to 100 FIT (1 FIT=10⁻⁹/hours). Of course, to achieve such reliability in the equipment itself, not only must each individual device be reliable, but also it is also extremely important to match the specific characteristics of the device with its application within the piece of equipment. In fact, information obtained in field studies show that for semiconductor devices manufactured using identical procedures, failure rates in the field could vary by a factor of 10 depending simply on how the device was used.

The following information covers device reliability with regards to how a device is used. An introductory discussion is also presented on quality-control procedures, and some examples of reliability testing data are given.

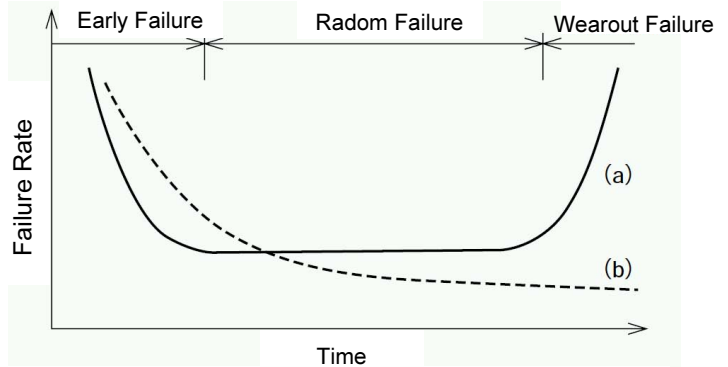


Fig.7.1 Failure Rate Versus Time

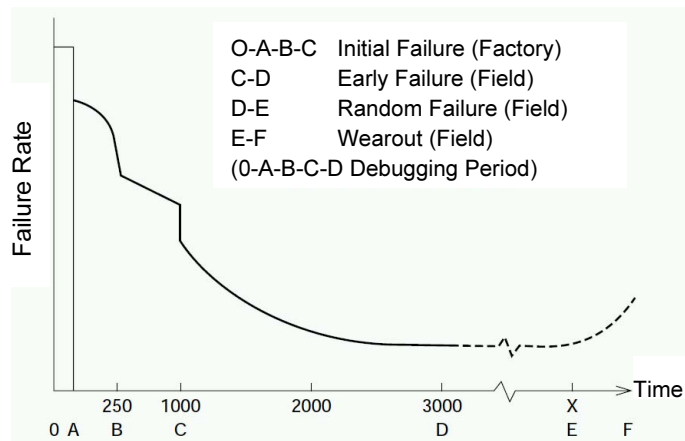


Fig.7.2 Semiconductor Device Failure Rate Versus Time

7-2. Basic Concepts of Semiconductor Device Reliability

7-2-1. Semiconductor Device Failure Rate Varied with The Lapse of Time

The failure rate of devices used in an average piece of equipment can be expressed by using the bathtub curve shown in Fig.7.1, line (a). Taken from the standpoint of time, device failures can be classified as an early failure, random failure and wear out failure period. Three points must be considered regarding the service life of a device; early and random failures rate, and lifetime before wear out.

But the failure rate of semiconductors is illustrated by line (b) in the graph, where failure rate is shown to gradually diminish as a factor of time. In other words, a notable feature of semiconductor devices is that the longer a particular device has been used, the more stable it will be. Viewed from a different perspective, even though random failure rate has been reduced to virtual stability, the failure distribution pattern shows early failures to still be prevalent. As shown by Fig.7.2 where failure rate versus time is given for an actual device, the highest failure rate occurs immediately after manufacture, but the process of ageing and debugging gradually lowers this failure rate.

The next step is with the user, who assembles, adjusts, and takes the device aging. Failure rates continue to decline during this period also. Generally, the rate for major defect during this period drops to less than 0.1%, and if this rate is exceeded by a substantial margin, one must look for a fault in the circuit design, assembly procedure, or the device itself. Unless the problem is found and corrected, frequent field failures will be the likely result. In most cases, the field failure rate can be correlated to major defect during this period, so this is an important aspect of device reliability.

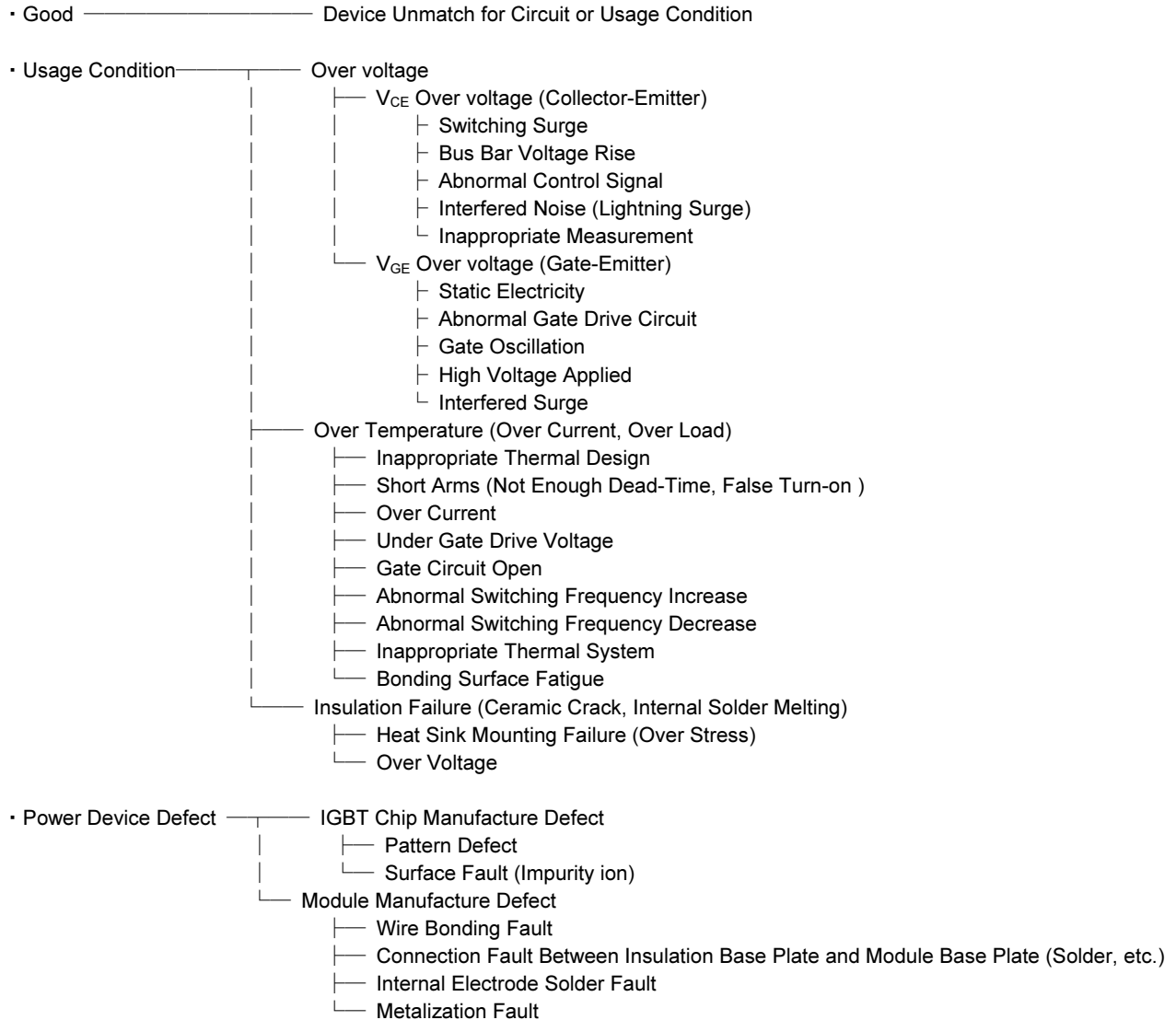
Upon transferring the equipment to field service, the stress level is reduced further, with a corresponding drop in failure rates. Failure rates normally range from several FIT to several hundred FIT during this period.

On the other hand, the user must design greater margins. For example, diodes and thyristors should be operated at 50 ~ 60% of their maximum voltage ratings or lesser, and junction temperatures should not exceed 70 ~ 80% of maximum rating. It is also important to remember that a device must be in working harmony with other components in the circuit for maximum reliability standards can be assured.

When designing a piece of equipment for reliable service, device selection must be considered from a standpoint of performance, reliability, and economy. Since it is not easy to achieve high performance/reliability and economy at the same time, a balance must be struck on the side of practical value. In other words, device selection should be based on the user's expectations for the machine he is designing.

7-2-2. Power Module Failure Reason

After a piece of equipment has been assembled and adjusted, or has been placed in field service, failed devices that are returned to the factory are analyzed to determine the cause of failure. This procedure is intended to determine whether the problem lays with the device itself, or the manner in which it was used. This section will list potential reasons of failure.



Operation life is dependent on the internal wire bonding, thermal fatigue between insulation base-plate and module base-plate. The thermal fatigue will be described in the next page.

7-2-3. Thermal Fatigue of Power Module

7-2-3-1 Operating Temperature Pattern

The operating temperature pattern of power module is displayed in Fig.7.3. It is important to consider two patterns that are independent each other in thermal fatigue life of power module.

■ Operation Mode 1

Power cycle life is called when change of case temperature is small, but frequent change of junction temperature occurs.

■ Operation Mode 2

The other one is thermal cycle life when comparatively slow change of temperature occurs by start and stop of the system.

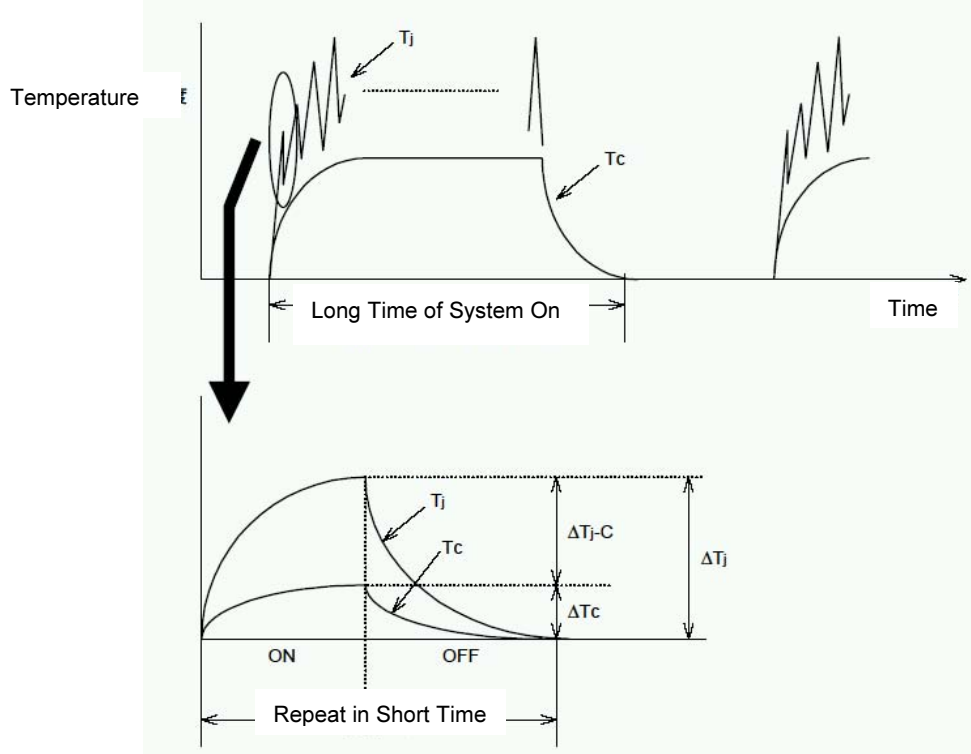


Fig.7.3 Operating Temperature Pattern

7-2-3-2. Power Cycle Failure Mechanism

Fig.7.4 shows the typical construction of power module. When junction temperature of power module is changed, stress strain between aluminum wire and silicon chip, and between silicon chip and insulation substrate occurs due to the difference of coefficient of linear expansion. If this stress is supplied repetitively, thermal fatigue for the junction becomes failure.

For inverter use, power cycle life is a necessary concern, which should be given during designing system. An example is given in Fig.7.5. The failure mode is that the crack of bonding surface makes progress by stress due to the difference of linear expansion between aluminum wire and silicone chip and finally lead to the peel failure mode.

A power cycle testing result of Mitsubishi Electric's module is shown in Fig.7.6.

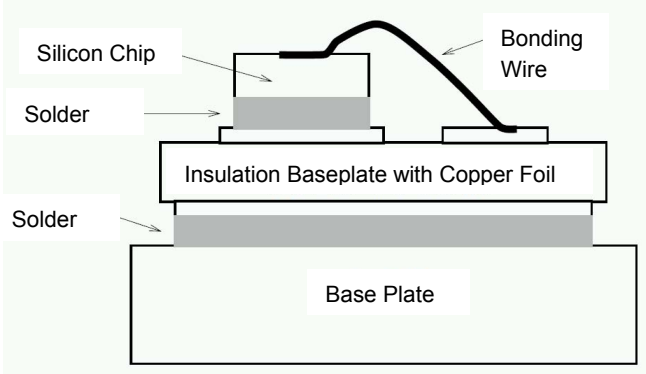


Fig.7.4 Module Structure

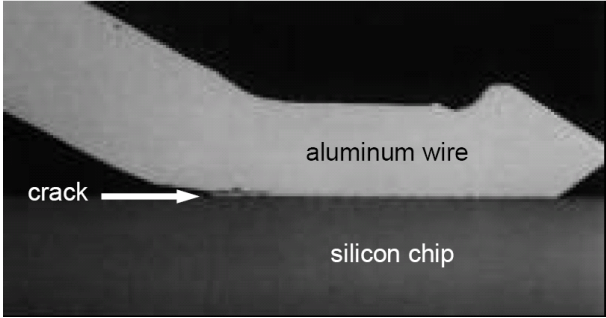
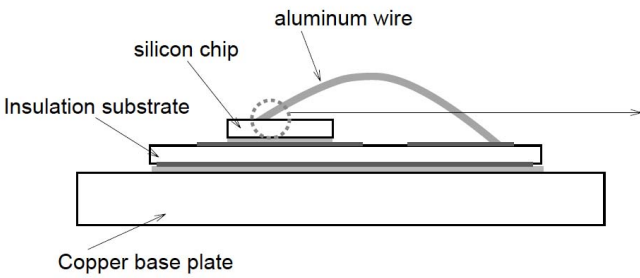


Fig.7.5 Bonding Surface Fatigue Caused by Power Cycle Testing

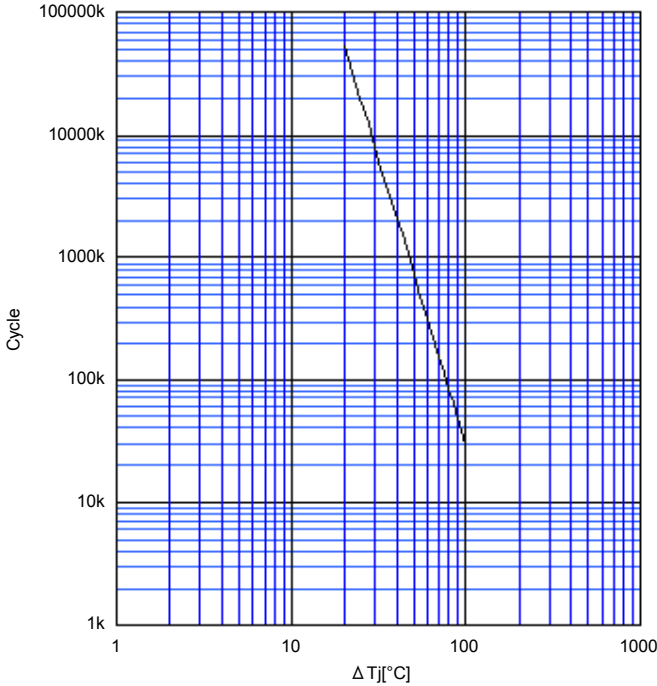


Fig.7.6 Power Cycle Curve

7-3. Mitsubishi's Quality-Assurance Program

One of the basic goals of Mitsubishi Electric is to offer our customers quality products. As a consequence, product quality, price, timely delivery, and service are equally important aspects deserving an equal amount of attention. Still, product quality must stand above all others from a standpoint of customer confidence.

Quality standards in the semiconductor industry are extremely high; production of wafers is a carefully controlled, precision process, and assembly processes are done under microscopes to assure that there are no sacrifices made in technology, or in quality.

The following subsections outline the quality-assurance programs Mitsubishi Electric uses in its mass-production.

7.3.1 The Path to a Mass-Production Device

From research prototype, through mass-production, a serial type tests are run at each stage to assure performance and reliability of the ultimate product. At the same time, the design drawings are also closely checked. The path from the research stage to mass-production is shown in the flow chart of Fig.7.7 The subsections that follow briefly describe the reliability tests used to check for device reliability.

7.3.2 Environmental Controls

The semiconductor industry as a whole recognizes the affect environmental factors have on product quality, and rigorous standards have been established regarding the control of dust, humidity, and temperature in manufacturing facilities. The same level of standards is also used for the various gases, and the water used in the manufacturing process.

7.3.3 Periodic Inspection and Maintenance of Manufacturing Equipment and Instrumentation

The various equipment and measuring instruments used in semiconductor production are an extremely important element of the total process. It is therefore imperative that a periodic program be implemented to inspect and adjust these components so that optimum precision standards are maintained, and to forestall any interruptions in the production process.

7.3.4 Quality-Control of Materials Purchases

Materials are subjected to rigorous acceptance tests using equipment such as spectrometers, helium leak detectors, etc. Before placing full orders, thorough sample testing is done, and all problem areas are worked out before making an official decision. Quality-control procedures at the supplier's plant are also considered in any procurement decision.

7.3.5 Control of the Manufacturing Process

Various measures have been taken to control the elements that have a decisive influence on the quality of the product. Measuring instruments are used to monitor water purity, atmospheric conditions, furnace temperatures, gas flow, and other factors. Check-sheet inspections are made, and recorders keep automatic records. These records are carefully correlated with the records kept on matters such as diffusion depth and surface density to establish proper working conditions.

7.3.6 In-Process and Final Inspections

The goals of the in-process and final inspections are twofold: the first is to assure product quality from the standpoint of outer appearance, dimensions, structural integrity, and mechanical and electrical characteristics. The second is to feed this information back upline to improve quality, and to reduce variations in future batches.

In-process inspections are intended to check the wafer and assembly processes, and serve two purposes; one being self-imposed checks on the production process, the other for use as a quality-control tool. As its name implies, production personnel to correct deficiencies they clearly recognize use the self-imposed check, and emphasis is placed on points that are difficult to detect in completed devices. After the device is completed, it is subjected to the final inspection and the quality-assurance inspection. The final inspection is run on all devices, and consists of testing electrical characteristics and outer appearance. Quality-assurance personnel assume the role of the end user, and inspect samples for correct electrical characteristics, outer appearance, and reliability before devices are packed in storage.

The flow chart for the quality-assurance program covered in the above is noted in Fig.7.9.

7.3.7 Quality Information

Mainly the quality assurance division compiles various kinds of quality information such as inspection results and customer-supplied information. They are quickly fed back to related divisions including the production division for maintenance and improvement of quality.

In addition, we employ computer-based, streamlined, and effective quality control systems in order to modernize the information management.

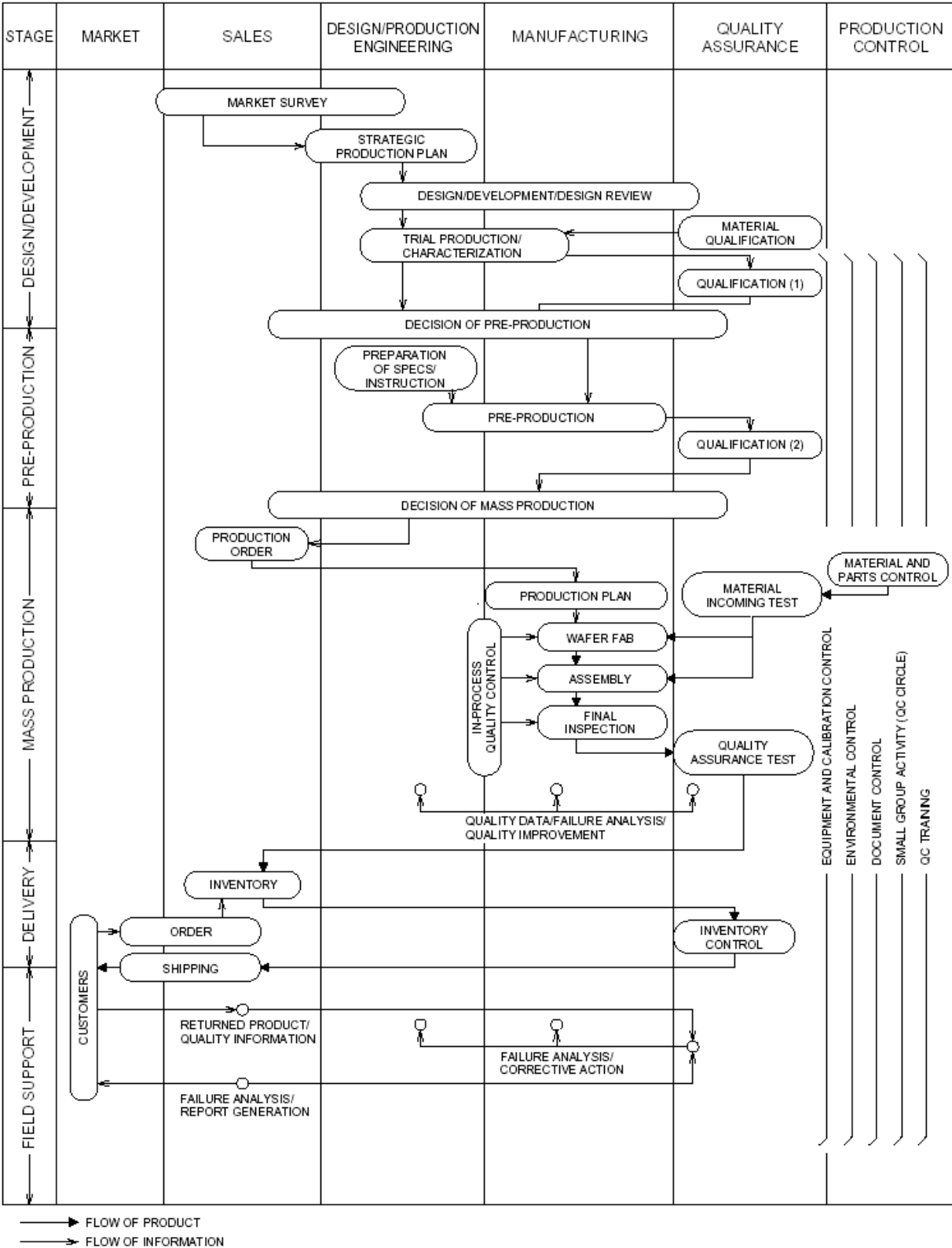


Fig.7.7 Flow Chart of Quality Assurance Program

7-4. Reliability Testing

7-4-1 Reliability Testing Procedures

High reliability standards are assured with Mitsubishi semiconductor devices through the rigorous quality-control inspections, which the devices are subjected to in the design and manufacturing stages, and through the quality-assurance inspections run on each production lot. Numerous reliability tests have been implemented in order to maintain this standard of reliability.

This section provides an overview of the reliability testing of thyristor devices. Test parameters are shown in Table 7.1, and as noted, conform to the procedures specified by the Japan Electronics and Information Technology Association (JEITA) handbook. (Related standards: International Electro technical Commission (IEC))

7-4-2 Results of Reliability Test of IGBT Module

Table 7.2 lists the results of the reliability tests performed on PM75B6LA060, a resin sealed type with current rating up to 75A to date. Failure criterion information is noted in Table 7.3.

Table 7.1. Mitsubishi Power Module Reliability Testing

	Test Parameter	Test Method		Test Conditions
Environmental Test	Thermal Shock	ED-4701	B-141	[Condition A] 100°C : 5 min, 0°C: 5 minutes, 10 cycles
	Temperature Cycling	"	B-131	Tstg min 60 min~Tstg max 60 min, 10 cycles
	Vibration	"	A-121	[Condition B] 10~500Hz/15 minute, 98.1m/s ² , 6h
	Robustness of Termination	"	A-111- I	9.8~40N, 10±1s
	Solder Heat Resistance	"	A-132	[Condition A] 260±5°C, 10±1s, Rosin flux used
	Solderability	"	A-131	[Condition A] 235±5°C, 5±0.5s, Rosin flux used
	Mounting Torque	"	A-112- II	M5:1.96~3.5N·m, 10±1s
Endurance Test	High Temperature Storage	"	B-111	Ta=Tstg max, 1000 h
	Low Temperature Storage	"	B-112	Ta=Tstg min, 1000 h
	Wetproof	"	B-121	[Condition B] Ta=60°C, RH=90%, 1000h
	Intermittent Current Flow	"	—	Δ Tc=50°C(Δ Tc=100°C), 5000 cycles
	High Temperature Reverse Bias	"	—	Ta=Tstg max, VCE=85%VCEs, VGE=0V, 1000h
	High Temperature Gate Bias	"	—	Ta=Tstg max, VCE=20V, VGE=0V, 1000h

*:Environmental and resistance testing conforms to standards specified in JEITA ED-4701 for discrete semiconductor devices.

Table 7.2. PM75B6LA060 Reliability Test Results

	Test Parameter	Test Method		Test Conditions	No of Samples	No of Failures
Environmental Test	Thermal Shock	ED-4701	B-141	[Condition A] 100°C(5min), 0°C(5min), 10 cycles	5	0
	Temperature Cycling		B-131	-40°C(60 min)~125°C(60 min), 10 cycles	5	0
	Vibration		A-121	[Condition B] 10~500Hz / 15 min, 98.1m/s ² , 6h	5	0
	Robustness of Termination		A-111- I	9.8N, 10±1 s	5	0
	Mounting Torque		A-112- II	Mounting Screws:M5, 3.5N·m, 10±1 s Main Terminal Screws:M5, 3.5N·m, 10±1 s	5	0
Endurance Test	High Temperature Storage		B-111	Ta=125°C, 1000h	5	0
	Low Temperature Storage		B-112	Ta=-40°C, 1000h	5	0
	Wetproof		B-121	Ta=60°C, RH=90%, 1000 h	5	0
	Intermittent Current Flow	—		Ta=50~100°C, , 5000h	5	0
	High Temperature Reverse Bias	—		Ta=125°C, VCEs=510V, 1000h	5	0

Table 7.3. PM75B6LA060 Failure Criterion

Test Parameter	Test Conditions	Failure Criterion		Note
		Lower Limit	Upper Limit	
ICES	VCE=600V, VD=0V	—	U.S.L × 2.0	
VCE(sat)	IC=75A, VD=15V	—	U.S.L × 1.2	
VEC	-IC=75A, VD=0V	—	U.S.L × 1.2	
SC	VD=15V, VCIN=0V	L.S.L × 0.9	—	
UV	trip	L.S.L × 0.9	—	
Electrical Stress	AC2500V 1 min	Insulation breakdown		

Note. U.S.L: Upper Specification Limit / L.S.L: Lower Specification Limit

7-5. Failure Analysis

Failure analysis is one of the sources of information used in maintaining, and making improvements in standards of quality and reliability. Failure analysis procedures are performed on failed devices at all stages of their life cycle, ranging from the development state to failure while in use. Failure analysis procedures are generally divided into area of external inspections, electrical testing, internal inspections, and chip analysis. The flow chart for these procedures is shown in Fig.7.8, while Table 7.4 lists the nature of the tests.

The results of the various reliability and failure analysis tests reveal the failure mode and mechanism, and this information is fed back to the process technology and manufacturing personnel so that they can take the appropriate measures to improve the final product.

7-6. Derating and Reliability Projections

The degree of reliability for a semiconductor device varies considerably depending on usage and environmental conditions. Design standards, the method of manufacture, and quality-control procedures also play a role in establishing the intrinsic reliability for semiconductors. Correlating device derating with reliability is also not an easy task. Please refer to Mitsubishi device reliability handbook for more information in detail.

<http://www.semicon.melco.co.jp/confidence/index.html>

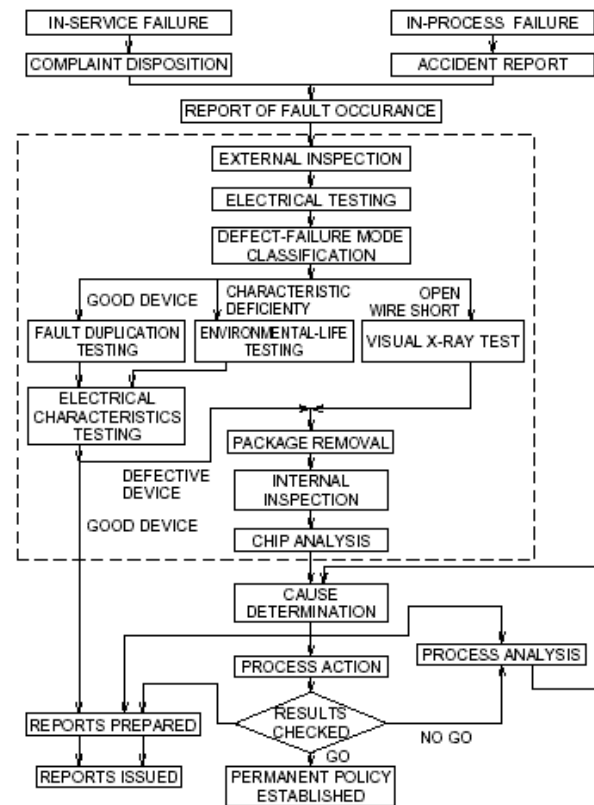


Fig.7.8 Failure Analysis Procedure

Table7.4. Failure analysis inspections and equipment used

Category	Inspection Items	Equipment
External Inspection	<ul style="list-style-type: none"> ○ Condition of leads, plating, soldering, and welds ○ Packaging defect ○ Solderability 	Stereoscopic microscope Metallurgy microscope
Electrical Characteristics Testing	<ul style="list-style-type: none"> ○ Static electrical characteristics, voltage and temperature margins, checking for broken bond wire, wire ○ Internal wiring 	Oscilloscope Curve tracer Characteristics tester X-ray equipment
Internal Inspection	<ul style="list-style-type: none"> ○ Device removed from package and chip surface observed for defects ○ Electrical characteristic check using microprobe ○ Check for hot spots and other abnormalities 	Metallurgy microscope microprobe Scanning electron microscope
Chip Analysis	<ul style="list-style-type: none"> ○ Analysis techniques used to supplement chip surface observation in internal inspection ○ Cross-section of chip observed for analyzing oxide film, diffusion and metallizing 	X-ray micro-analyzer Infrared micro-scanner Spectrum analyzer

7-7. Conclusion

The above is a simple introduction to general ideas about reliability, reliability tests, and derating and forecasting of reliability of high power semiconductor, which are semiconductor devices for electric power. As explained above, it is vital for higher reliability in practical use of semiconductor devices to understand their features and select those, which are suitable for equipment and sets. It is also important to design semiconductor devices with some allowance to improve reliability, fully taking their derating into consideration in relation to operating and environmental conditions.

Other essential things to do are to “debug” equipment and sets, and to analyze data obtained in fabrication process and actual operation to feed them back to design and fabrication stages. To improve the reliability by design of high power semiconductor requires considerations on many issues as described above. Utilize the semiconductor devices successfully with the utmost care with comprehensive understanding of their quality, reliability, and economy.

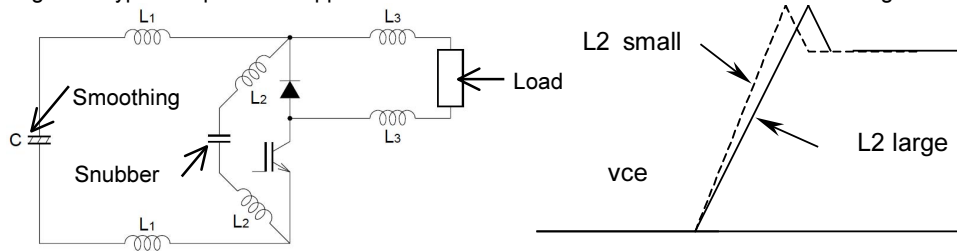
8. Installation of power Module

8-1 Installing Capacitor

During switching, voltage is induced in power circuit stray inductance by the high di/dt of the main current. This voltage can appear on the IPM and cause damage. In order to avoid this problem, guidelines that should be followed in designing the circuit layout are:

- ① Located the smoothing capacitor as close as possible to the IPM
- ② Use ceramic capacitor near the IPM to bypass high frequency current
- ③ Adopt low impedance electrolytic capacitor as smoothing capacitor
- ④ Use snubber circuit to absorb surge voltage
- ⑤ Decrease switching speed in order to lower di/dt .

② and ⑤ are the most effective to reduce surge voltage. The stray inductance of snubber circuit generally is not considered to avoid complicating the circuit. In addition, combination of ②, ④, ⑤ is needed since there is a limit on the length of wiring. The bypass capacitor of approach ② act as a snubber when oscillation is occurring.



- L1 : Stray inductance between the electrolytic capacitor and the IPM.
 L2 : Stray inductance between the filter capacitor and the driver.
 L3 : Stray inductance between the load and the power circuit's output stage

8-2 Installation Hints

When mounting IPM on a heat-sink, uneven mounting can cause the modules ceramic isolation to crack.

To achieve the best thermal radiation effect, the bigger the contact area is, the smaller the thermal resistance is Heat-sink should have a surface finish in range of Rz6 ~ Rz12, curvature within 100 μ m.

Uniform coating of thermal grease between the module and heat-sink can prevent corrosion of contact parts. Select a compound, which has stable characteristics over the whole operating temperature range and does not change its properties over the life of the equipment.

Use a uniform coating of thermal interface compound. The thickness of thermal grease should be ranked in 100~200 μ m according to the surface finish.

Mounting screws should be tightened by using a torque wrench to the prescribed torque in progressive stages in a cross pattern. As mentioned before, over torque terminal or mounting screws may result in damage of IPM.

When an electric driver is used, thermal grease with low viscosity is recommended and extra grease must be extruded before final tightening screws.

* For the recommended torque order for mounting screws referring to "Installation Method" in the section of "Correct and Safety Use of Power Module"

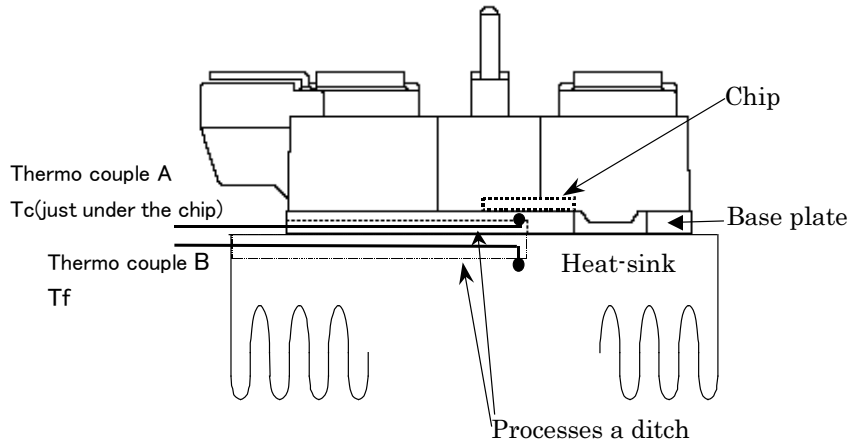
Note) Maximum torque specifications are provided in device data sheets. The type and quantity of thermal compounds having an effect on the thermal resistance are determined by consideration of both thermal grease and heat-sink. Typical value given in datasheet is measured by using thermal grease produced by Shin-Etsu Chemical Co.,Ltd. (G-746, which has not issued in Shin-Etsu's publications, is almost the same as G-747.)

Installation of power Module

8-3 Thermal Impedance Considerations & Chip Layout

The junction to case thermal resistance $R_{th(j-c)}$ and the case to heat-sink thermal resistance $R_{th(c-f)}$ are given in datasheet. The case temperature has been measured at the just under the chip.

The case temperature measurement point of various products is shown in Table 3. It is measured by uniform $100\mu\text{m}\sim 200\mu\text{m}$ coating of thermal grease with thermal conductivity of $0.92\text{W}/\text{m}\cdot^\circ\text{C}$ between the module and heat-sink. A Thermo-couple is used to measure the temperature of case and heat-sink at the same point shown in the following tables. (0.8ϕ 3mm depth, 0.3ϕ thermo-couple)



·Note

*The thermal impedance depends on the material, area and thickness of heat-sink. The smaller the area and the thinner the heat-sink is, the lower the impedance is for the same material.

*The type and quantity of thermal compounds can affect the thermal resistance.

Table 3: Thermal resistance and chip layout of PV-IPM

Thermal resistance

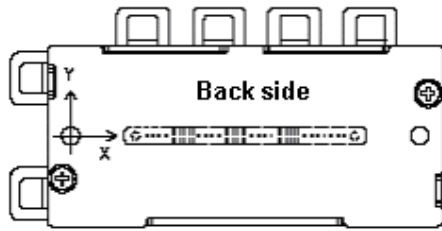
Type Name	Inverter		Chopper			contact thermal resistance
	Just under the chip		Just under the chip			Under the module
	IGBT-chip $R_{th(j-c)Q}$	FWDi-chip $R_{th(j-c)}$	IGBT-chip $R_{th(j-c)Q}$	FWDi(P)-chip $R_{th(j-c)}$	FWDi(N)-chip $R_{th(j-c)}$	$R_{th(c-f)}$
PM50B4LA/LB060	0.95	1.61	—	—	—	0.038
PM50B5LA/LB060	0.95	1.61	0.95	0.95	1.61	0.038
PM50B6LA/LB060	0.95	1.61	0.95	0.95	1.61	0.038
PM50B4LA/LB060	0.32	0.53	—	—	—	0.038
PM50B5LA/LB060	0.32	0.53	0.32	0.33	0.53	0.038
PM50B6LA/LB060	0.32	0.53	0.32	0.33	0.53	0.038

Chip Layout

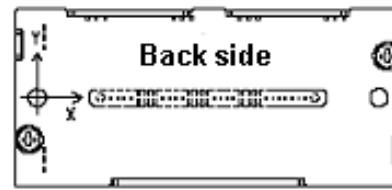
Unit(mm)

		UP		VP		WP	BP	UN		VN		WN		BN	
		IGBT	FWDi	IGBT	FWDi	FWDi	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
PM50B4LA/LB060	X	31.1	30.6	61.0	60.5	—	—	38.2	40.7	52.9	50.4	—	—	—	—
	Y	-10.0	-2.2	-10.0	-2.2	—	—	8.0	0.2	8.0	0.2	—	—	—	—
PM50B5LA/LB060	X	32.7	32.2	62.8	63.3	82.9	—	38.8	39.3	53.0	52.5	75.6	75.1	—	—
	Y	-10.0	-0.2	-8.8	-2.0	-8.4	—	8.0	0.8	3.8	-2.8	3.8	-2.8	—	—
PM50B6LA/LB060	X	32.7	32.2	62.8	63.3	82.9	21.8	38.8	39.3	53.0	52.5	75.6	75.1	18.1	25.9
	Y	-10.0	-0.2	-8.8	-2.0	-8.4	6.8	8.0	0.8	3.8	-2.8	3.8	-2.8	-10.0	-8.4
PM75B4LA/LB060	X	30.4	30.4	61.7	61.7	—	—	39.7	39.7	52.4	52.4	—	—	—	—
	Y	-8.3	-0.8	-8.3	-0.8	—	—	6.3	-1.2	6.3	-1.2	—	—	—	—
PM75B5LA/LB060	X	33.6	31.2	66.0	66.0	85.8	—	40.5	41.6	56.2	56.2	76.3	76.3	—	—
	Y	-7.5	4.5	-8.6	0.6	-3.1	—	8.0	0.0	2.7	-5.5	2.7	-6.5	—	—
PM75B6LA/LB060	X	33.6	31.2	66.0	66.0	85.8	22.7	40.5	41.6	56.2	56.2	76.3	76.3	18.7	26.1
	Y	-7.5	4.5	-8.6	0.6	-3.1	7.2	8.0	0.0	2.7	-5.5	2.7	-6.5	-10.1	-9.0

Installation of power Module



1) Screw type



2) Pin type

8-4 Coating Method of Thermal Grease (Example)

The coating method of thermal grease is introduced in this section. The thermal grease is called as grease in the following.

- ① Preparations: power module, grease, scraper or roller, electronic mass meter and gloves
- ② Relationship between the coating amount and thickness is,

$$\text{Thickness of grease} = \frac{\text{amount of grease [g]}}{\text{base area of module [cm}^2\text{]} \times \text{density of grease [g/cm}^3\text{]}}$$

The recommended thickness of grease is 100 μm ~200 μm .

The amount of grease can be obtained as the following example.

For example : For case with size of 110 \times 89(PM100CSD060), the amount of Shin-Etsu Chemical Co.,Ltd. grease G-746 can be calculated through the equation below.

$$100\sim 200\mu\text{m} = \frac{\text{amount of grease [g]}}{97.9[\text{cm}^2] \times 2.66[\text{g/cm}^3]}$$

\therefore The amount needed is \approx 2.6~5.2 [g]

- ③ Measure the mass of module
- ④ Measure the grease with the same amount as calculated
- ⑤ Coating the module base uniformly by using scraper or roller
- ⑥ Mask print of grease.

Finally it is fulfilled to uniformly cover thermal grease on the module base with specified thickness.

Table 4 Thermal Compounds

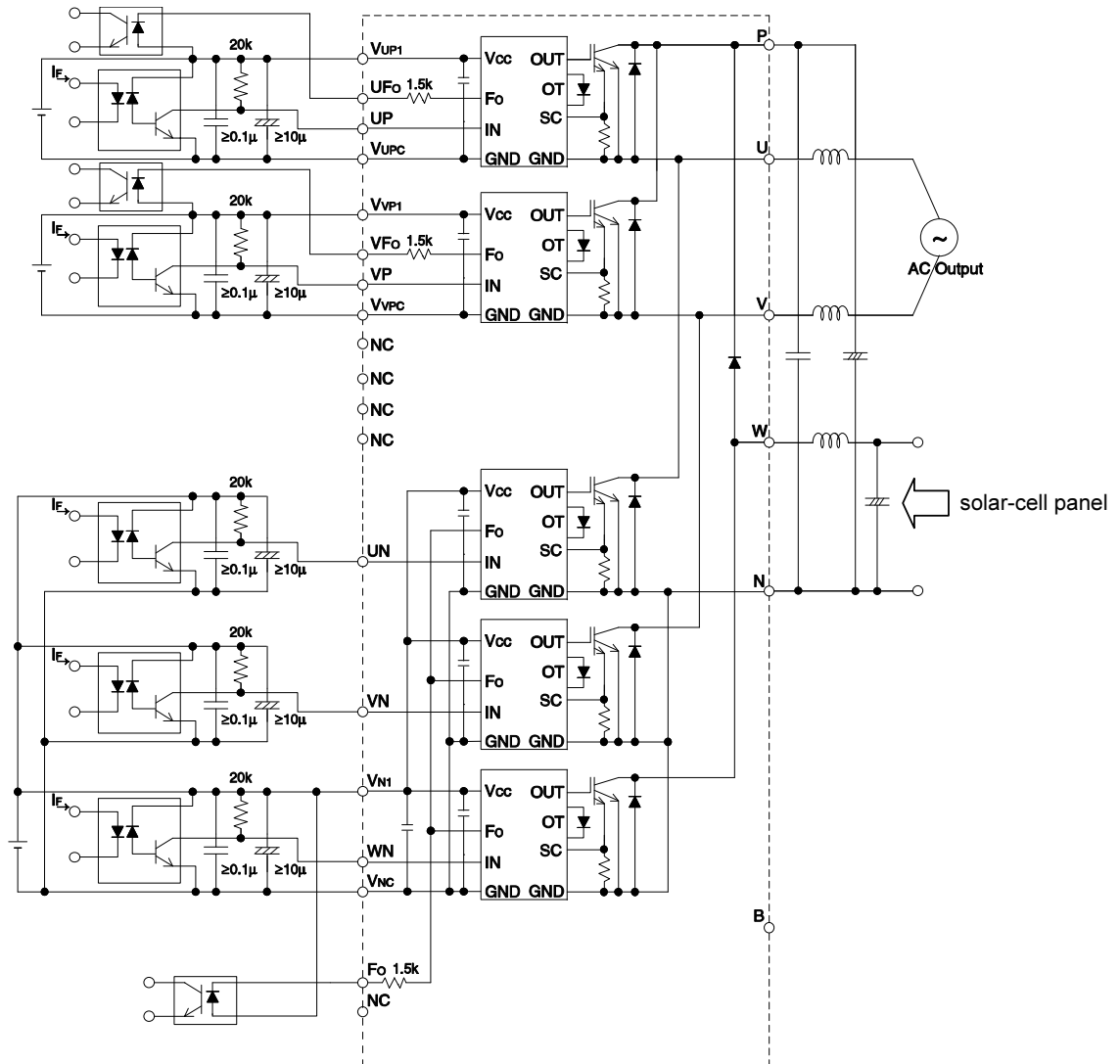
Manufacturer	Type	Note
Shin-Etsu Chemical Co., Ltd. GE Toshiba Silicones	KS-609, G-747, else YG6260	
ALCAN	UNIVERSAL JOINTING-COMPOUND	For non-insulation type

For more information, please refer to manufacturers.

9. Using IPM

9-1 Applications of PV-IPM to Photo voltaic power generator

(ex. PM50B5LA/LB060, PM75B5LA/LB060)



Notes for stable and safe operation ;

- Design the PCB pattern to minimize wiring length between photo-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of photo-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching photo-coupler.
- Fast switching photo-coupler : $t_{pLH}, t_{pHL} \leq 0.8 \mu s$, Use High CMR type.
- Slow switching photo-coupler : $CTR > 100\%$
- Use 3 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. $4.7nF$) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

Using IPM

9-2 Interface of control side of IPM

IPM (Intelligent Power Modules) is easy to operate. The integrated drive and protection circuits require only an isolated power supply and a low level on/off control signal. A fault output is provided for monitoring the operation of the module internal protection circuits.

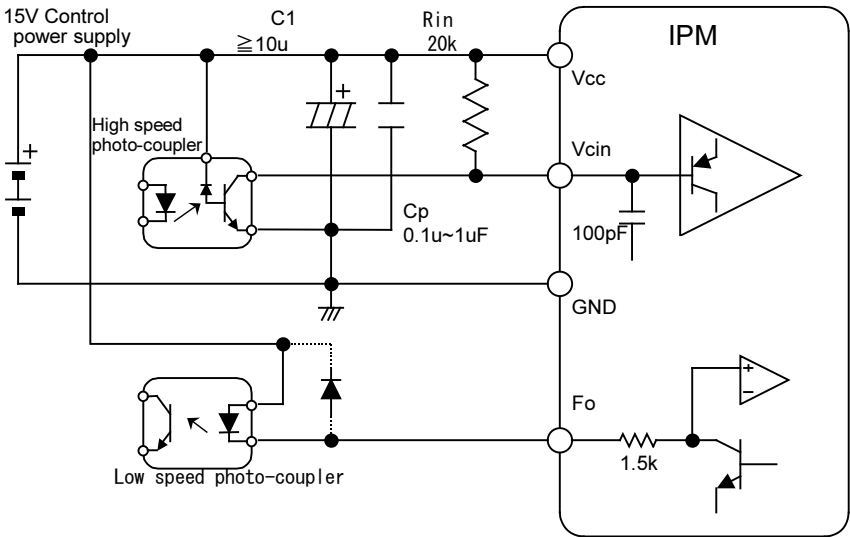
- (1) Circuit and circuit constant of the IPM interface circuit
The parts of connecting IPM and controller (CPU) are required to use following parts.

- Input terminal ① High speed photo-coupler ,② Pull-up resistor
- ③ Condenser (Ceramic condenser for the ripple removal and electrolytic condenser for the power stabilization)
- Fo terminal ④ Low(high) speed photo-coupler
- Control power supply ⑤ The mutually insulated stabilized power source of +15 V (The negative power as it uses in IGBT-MOD is unnecessary.)

Example of constant value of the IPM interface circuit

Symbol	Name	Recommend Value	Note
Rin	Pull-up resistor	20kΩ	All input terminal (include Br)
C1	Smoothing capacitor	≥ 10uF	It is necessary that the charge and discharge electric current and the dv/dt electric current to IPM(IGBT gate) can be sufficiently absorbed. ex.) PS9613
Cp	Bypass condenser	0.1 ~ 1uF	
PC	Photo-coupler	High CMR, CTR	

- (2) IPM Internal circuit diagram and interface circuit



- (3) IPM Control terminals

The IGBT power switches in the IPM are controlled by a low level input signal. The active low control input will keep the power devices off when it is held high. Typically the input pin of the IPM is pulled high with a resistor connected to the positive side of the control power supply. An ON signal is then generated by pulling the control input low.

The recommended value of the pull-up resistor is 20 kΩ but it can be smaller for the noise countermeasure and so on. However, if the pull-up resistor is set too small, it will affect the lifetime of the photo-coupler, please confirm the characteristics with lifetime and so on in the photo-coupler manufacturer.

The inside of the control input terminal is connected to the comparator and is with high impedance. When IPM (IGBT) is turn-off, the output impedance of the photo-coupler becomes high. Total impedance of the circuit which connect the interface circuit is equal to a resistance of about 20K Ω .

The most important consideration in interface circuit design is layout. Shielding and careful routing of printed circuit wiring is necessary in order to avoid coupling of dv/dt noise into control circuits. Parasitic capacitance between high side interface circuits, high and low side interface circuits, or primary and secondary sides of the isolating devices can cause noise problems. Careful layout of control power supply and isolating circuit wiring is necessary. In layout, it is important not to make wiring of the photo-coupler primary side and secondly side cross each other. Also, pattern should be made shortest and not to be crowded around and the magnetic field make the inside of the current-loop not cross. Place condenser with good frequency response between the power - GND of the photo coupler.

Depending on the pattern layout, sometimes a ringing as shown below occurs. In this case, the output current of the photo-coupler doesn't change so much than the corrugation at normal. However, the ringing problem increases the IPM switching loss, results possibly the IPM heat destruction. It is necessary to check in design.

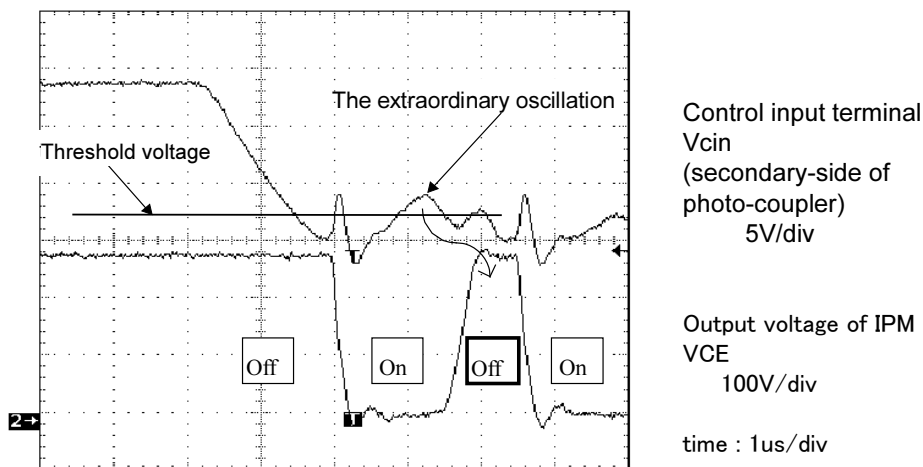


Fig.9.1 The example of the oscillation waveform A of the photo-coupler

In the following example, the oscillation happens at the timing of both after on and off. When the oscillation after turn off continues over the dead time, it falls in the period when the opposite arm becomes on then cause an arm short failure. The protection circuit works and IPM outputs Fo. This phenomenon sometimes happens under the condition of no-load. It is easily confused with the malfunction on the side of IPM and the cause investigation takes time. As a countermeasure, reducing the power supply impedance of the photo-coupler and the photo-coupler use by IPM compatible is effective.

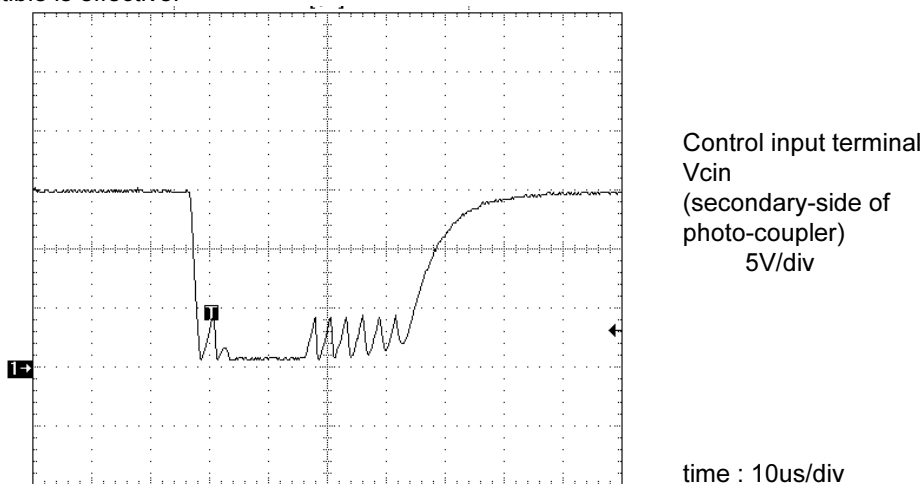


Fig.9.2 The example of the oscillation waveform B of the photo-coupler

(4) Fo terminal of IPM

Fo is the output which shows the abnormal condition of IPM.

The extraordinary modes are overheating(OT), load (the arm) short circuit(SC), and control supply under voltage(UV). Fo does not distinguish these kinds of failures.

The fault output is open collector type with its maximum sink current internally limited. When a fault condition occurs the open collector device turns on allowing the fault terminal to sink current from the positive side of the control supply. The inside of the Fo terminal is the open-collector composition which connected resistance (1.5K Ω) in series.

Note)

If Fo is not used, the malfunction being able to be detected on the side of the system, passing away, it isn't possible to do a protection-coordination with the system. For example, if Fo on the P-side is not used, then a earth-short failure will not be able to protect in the system, and the earth-short occurs continuously. Because IPM sometimes destroys when this condition continues, it is recommended to use all Fo terminals.

Fo terminal is connected with the comparator input circuit inside IPM. When leave this terminal open, there is possibility that the noise invades from this terminal and cause malfunctions of the circuit inside IPM. In this case, inserting a high frequency type condenser of about 0.1 μ F between the Fo terminal and GND is effective. Also, when not use Fo, in order not to undergo influence by the noise, connect it to 15 V control source.

Depending on the pattern layout of Fo, surge voltage over 20V is sometimes observed at the Fo terminal. Due to this surge voltage, the electric strength is exaggerated and the LED part of the photo-coupler destroys. Be careful of the pattern layout. If the surge voltage is difficult to be reduced, add a diode in the converse and parallel(It refers to p1). To make low-impedance is important.

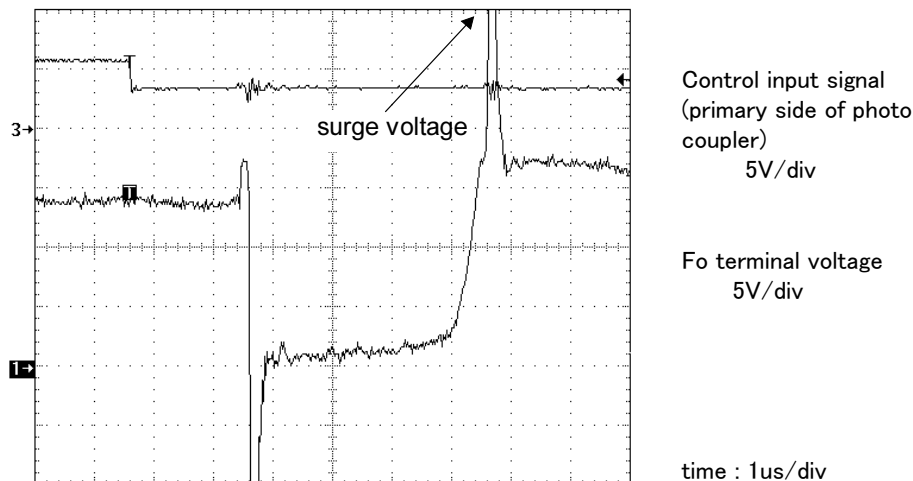


Fig.9.3 The example of the extraordinary waveform of the Fo terminal

(5) Example of photo coupler

The example of the photo-coupler recommended for IPM is shown below.

High speed photo coupler

High speed photo couplers are connected to the control input terminals of IPM.

When choosing photo coupler, pay attention to the parameters of response time (tpLH,tpHL) and CMR.

Choose the photo coupler that the value of tpLH,tpHL is less than 0.8us, and with high CMR.

Especially, ensure that the phenomena such as the ringing not occur.

For example)

PS9613 (NEC)

TLP559(IGM) (Toshiba)

The photo-coupler manufacturer sometimes has the IPM exclusive-goods (another form name) which sorted out a characteristic. Please inquire the photo-coupler of IPM compatible for the malfunction prevention when order.

Low speed photo coupler

Low speed photo coupler is connected Fo terminal of IPM.

When choosing photo coupler, pay attention to the parameter of CTR.

Choose the photo coupler that the value of CTR is equal to or more than 100 %.

For example)

TLP-521 (Toshiba)

PS2502 (NEC)

Please inquire the manufacturer that the photo-coupler has or has not problem when work under your environmental condition.

Words and terms)

CTR (Current Transfer Ratio) : The ratio of the output current to the input current

CMR (Common Mode Rejection) : The maximum rise ratio of common mode voltage

t_{pLH}, t_{pHL} : The Propagation delay time L→H ,H→L

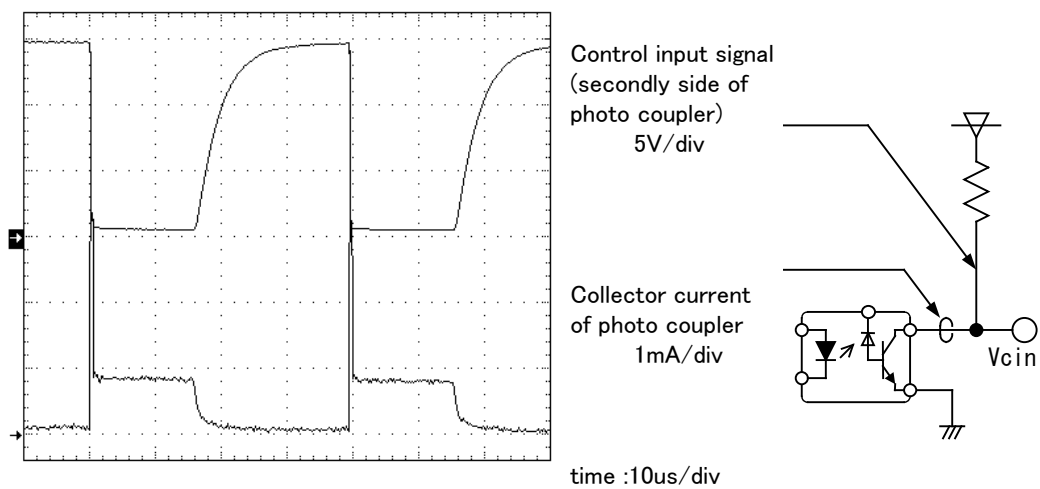


Fig.9.4 The example of the input/output waveform of the control input terminal(photo coupler output).

(6) Notice of using photo coupler

The photo coupler can isolate the primary side and secondary side. But, this is not correct at the high frequency. Because, photo coupler have a parasitic capacity between primary side and secondary side. When high dv/dt is impressed, the pulse electric current flows from the primary side to the secondary side via the parasitic capacity of photo coupler. This current sometimes turn on the photo coupler.

Therefore, it is important to design a circuit so that the LED will not turn on erroneously by this dv/dt .

When the input signal is OFF, make sure the circuit that the LED of primary side of photo coupler is with low-impedance.

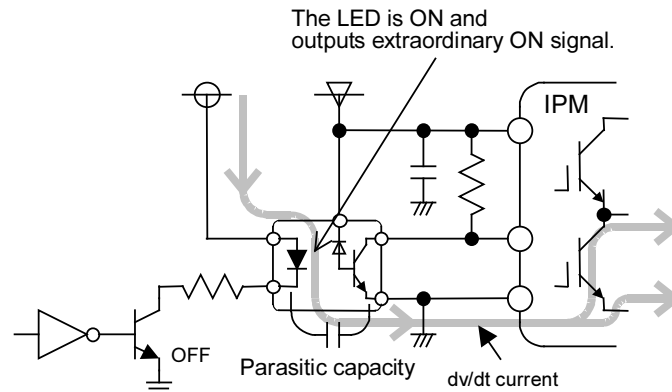


Fig.9.5 The example of the circuit which isn't good

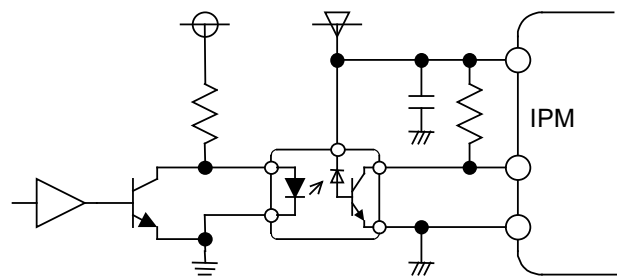


Fig.9.6. The example of the circuit to recommend

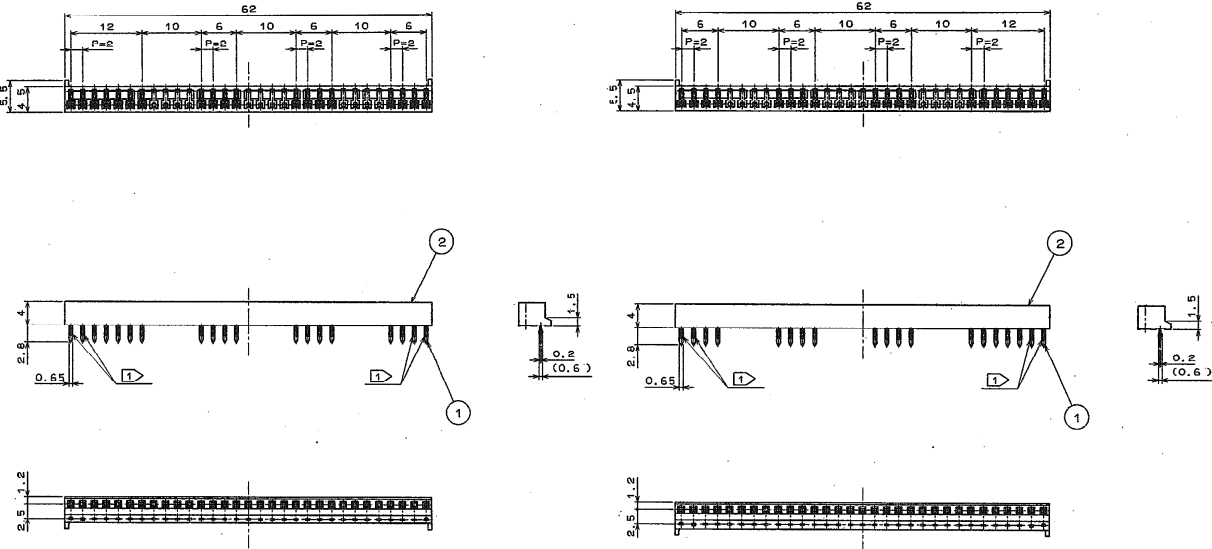
The recommended circuit doesn't make malfunction (LED of primary side of photo coupler is ON) because the dv/dt current can not turn ON the LED of primary side of photo coupler.

Please consult the application-note of the photo coupler for the detailed instruction of the circuit around the photo coupler.

Using IPM

(7) Connector for control terminal of IPM

We use the connector from "HIROSE ELECTRIC CO., LTD" in our test of IPM. The following connector is recommended. The pitch of this connector is 2.00 mm. It is the special connector of IPM which secured an electrical clearance among the terminals(U-V,V-W,W-U of P-side and N) The terminal with gold plate is recommended from the viewpoint of contact reliability.



Type name :DF10-31S-2DSA(68)

Type name :DF10-31S-2DSA(62)

The details of the connector inquire of the manufacturer (HIROSE ELECTRIC CO., LTD.).

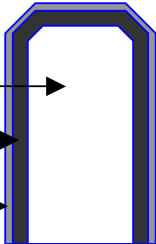
Note)

In the B4LB/B5LB/B6LB type, installation by solder is being recommended by the printed circuit board and the input and main terminal.

(8) The material of control terminal of IPM (B4LA / B5LA / B6LA type)

As a reference of the connector selection, the material and the metal finishing of the control terminal on the side of IPM are shown below.

Main material	Brass		
The specification of the plating	substrate	Nickel (Ni)	Thickness = 1 ~ 5μm
	surface	Gold(Au)	Thickness = 0.05 ~ 0.2μm



(9) The guide pin of IPM

The guide pin on both sides of the control terminal of IPM is metal. The guide pin is molded by plastic, and isolated.

In the B4LB / B5LB / B6LB type, installation by solder is being recommended, the plating of control terminal for these types are Sn

9-3 Control Power supply of IPM

- (1) The control power supply
The voltage range including ripples should meet the specification.

Control supply voltage V_D (V)	Operation behavior
0~4.0	It is almost the same as no power supply. External noise may cause IPM malfunction (turns ON). Supply under-voltage protection will not operate and no Fo signal will be asserted.
4.0~12.5	Even if control input signals are applied, IGBT does not work Supply under-voltage protection starts operation and outputs Fo signals.
12.5~13.5	Switching operation works. However, this value is below the recommended one, $V_{CE(sat)}$ and switching time will be out of the specified values, it may increase collector dissipation and junction temperature.
13.5~16.5	Recommended values.
16.5~20	Switching operation works. This range, however, is over the recommended value, thus, too fast switching speed might cause the chips to be damaged
20.0~	The control circuit will be destroyed.

Specifications for Ripple Noise

High frequency noise super imposed on the control IC supply line might cause IC malfunction and cause an Fo signal output, and results IPM stop (interrupt gates). To avoid such malfunction, the supply circuit should be designed such that the noise fluctuation is smaller than +/- 5V/us, and the ripple voltage is less than 2V.

$$\text{Specification : } \frac{dv}{dt} \leq \pm 5V / us \quad , \quad V_{\text{ripple}} \leq 2V_{p-p}$$

When the noise on the power supply line is a high frequency(pulse-width<about 50ns, pulse-vibration<about 5V) which does not cause an Fo output from IPM, the noise can be ignored. The power supply should be a low impedance, be careful of the pattern layout. Connect a bypass condenser with good frequency response and a smoothing condenser close to the terminals of IPM. It is effective for the prevention of the malfunction.

Control Supply Starting up and Shutting Down Sequence

Control supply V_D should be started up prior to the main supply (P-N supply).
Control supply V_D should be shut down after the main supply (P-N supply).

If the main supply had been started up before the control supply, or if the main supply remains after control supply was shut down, external noise might cause the IPM malfunction.

As for the P-side , use the control power supply which was insulated in each of all of the 2 aspects.
As for the N-side , because the GND in 2 aspects and the converter part is common, a common power can be used for the three control sources in amount.

(2) The circuit current of control power supply of IPM

The circuit current of control power supply of IPM is shown below.
This current is average of DC and $f_c=20\text{kHz}$.

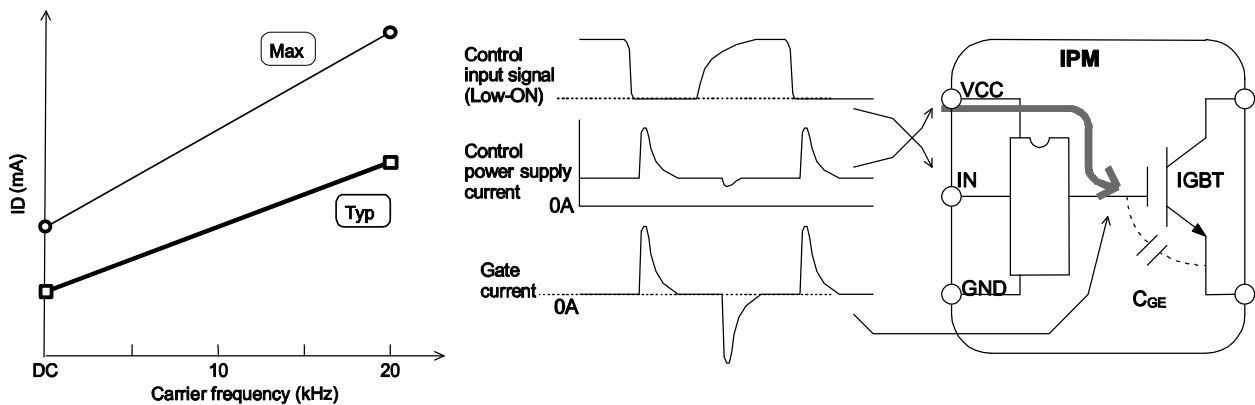
Condition : $V_D=15\text{V}$, $T_j=25\text{ deg C}$, Unit : mA

PV-IPM	N-side				P-side			
	DC		20kHz		DC		20kHz	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max
PM 50B4LA/LB060	10	20	28	38	5	10	12	17
PM 50B5LA/LB060	15	25	34	46	5	10	12	17
PM 50B6LA/LB060	20	30	41	56	5	10	12	17
PM 75B4LA/LB060	15	25	46	62	6	12	16	22
PM 75B5LA/LB060	20	30	56	76	6	12	16	22
PM 75B6LA/LB060	24	34	65	88	6	12	16	22

The circuit current of the IPM control power supply at other frequency

The circuit current of control power supply of IPM increases with the carrier frequency.

The carrier frequency dependence of the circuit current of the IPM control power supply can be approximated as a straight line like the following figure.



The gate of IGBT used in IPM has an input-capacitance($C_{ies}=C_{GE}+C_{CG}$).

The current to be charged and discharged by flowing through the gate at the timing of gate on and off.
There is IPM that this current becomes 1~2 A.

When IPM is turn-off, the dv/dt current from the collector of IGBT flows into the side of the control power supply. Design a control power supply in the low impedance so that this dv/dt current can be absorbed. Otherwise, The control IC of IPM might make malfunction and On signal is activated by this current resulting arm short circuit.

The control power supply circuit needs a capacity that it can supply and absorb these current.

Usually, such problems(maximum current, impedance) can be avoided by power supply circuit and also bypass ,smoothing condenser. But, the effect of the condenser is influenced by the inductance of the wiring pattern. Determine the condenser capacity after verifying the substrate and the equipment.

9-4 Fault Signal of IPM

IPM (Intelligent Power Modules) have sophisticated built-in protection circuits that prevent the power devices from being damaged should the system malfunction or be over stressed. Control supply under-voltage(UV), over temperature(OT), and short-circuit(SC) protection are all provided by the IPM's internal gate control circuits. A fault output signal is provided to alert the system controller if any of the protection circuits are activated. Following Fig.9.7 is a block diagram showing the IPM's internally integrated functions.

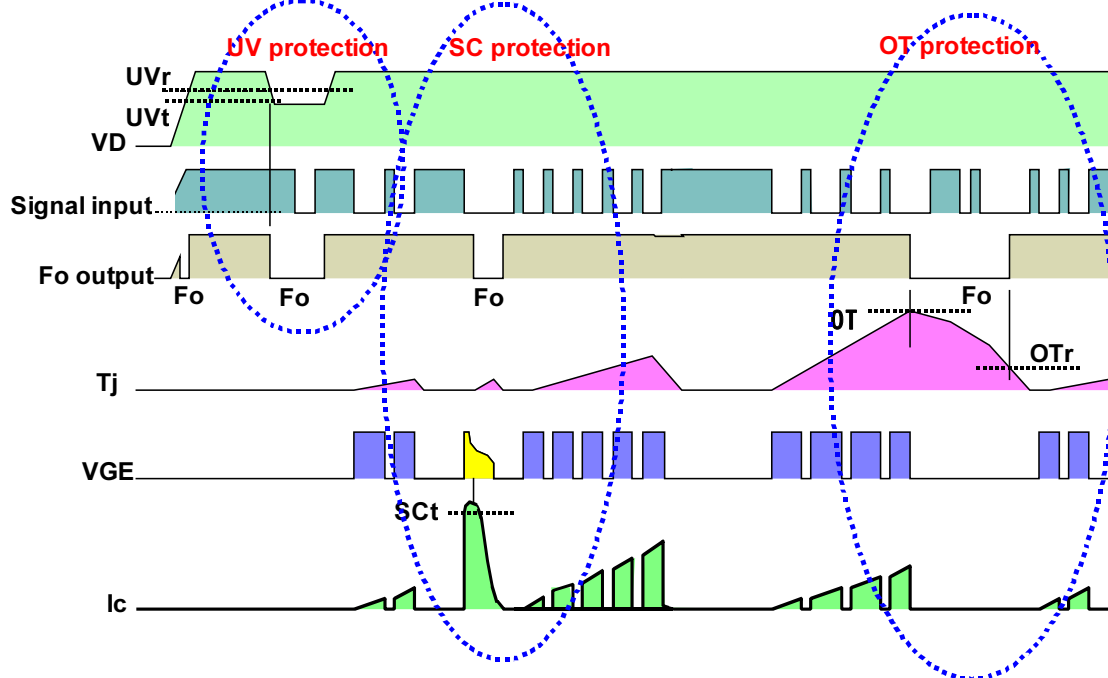


Fig.9.7 Timing chart of Control and protection of IPM

Control Supply Under-Voltage (UV)

The IPM's internal control circuits operate from an isolated 15V DC supply. If, for any reason, the voltage of this supply drops below the specified under-voltage trip level (UVt), the power devices will be turned off and a fault signal will be generated. Small glitches less than the specified $t_{dUV} (< 10\mu s)$ in length will not affect the operation of the control circuitry and will be ignored by the under voltage protection circuit. In order for normal operation to resume, the supply voltage must exceed the under voltage reset level (UVr). Operation of the under-voltage protection circuit will also occur during power up and power down of the control supply. This operation is normal and the system controller's program should take the fault output delay (tfo) into account.

Note)

1. Application of the main bus voltage at a rate greater than 20V/ms before the control power supply is on and stabilized may cause destruction of the power devices.
2. Voltage ripple on the control power supply with dv/dt in excess of 5V/us may cause a false trip of the UV lock-out.

Over Temperature (OT)

The IPM has a temperature sensor mounted on surface of IGBT chips. If the temperature of the IGBT chips exceeds the over temperature trip level (OT) the IPM's internal control circuit will protect the power devices by disabling the gate drive and ignoring the control input signal until the over temperature condition has subsided. The fault output will remain as long as the over temperature condition exists. When the temperature falls below the over temperature reset level (OTr), and the control input is high (offstate) the power device will be enabled and normal operation will resume at the next low (on) input signal.

Note)

1. Tripping of the over-temperature protection is an indication of stressful operation. Repetitive tripping should be avoided.

Short Circuit (SC)

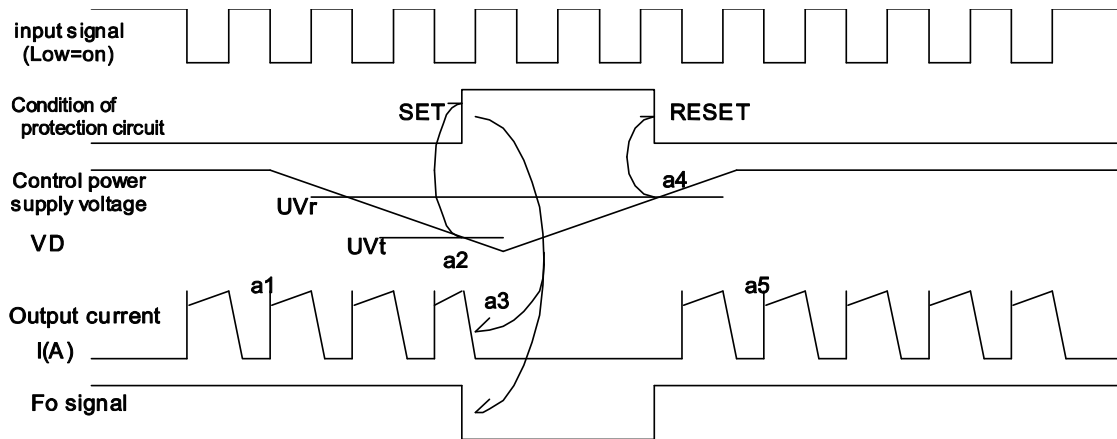
If a load short circuit occurs or the system controller malfunctions causing a shoot through, the IPMs built in short circuit protection will prevent the IGBTs from being damaged. When the current, through the IGBT exceeds the short circuit trip level (SC), an immediate controlled shutdown is initiated and a fault output is generated.

Note)

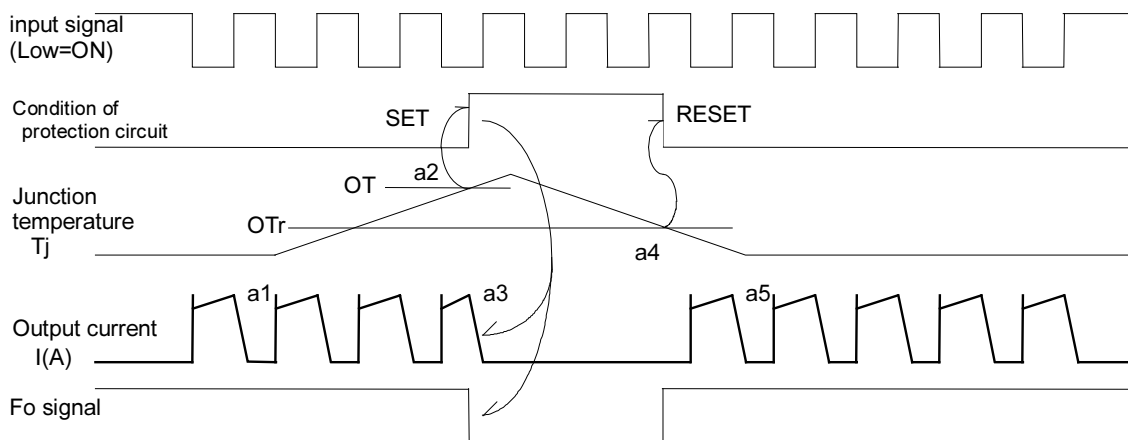
1. Tripping of the over current and short circuit protection indicates stressful operation of the IGBT. Repetitive tripping should be avoided.
2. High surge voltages may occur during emergency shutdown. Low inductance buswork and snubbers are recommended.

The operating-sequence of the UV protection

- a1 : The normal operation=IGBT ON
- a2 : The decline of control power supply voltage (UVt)
- a3 : IGBT OFF (Even if the input signal is in on state)
- a4 : The rise of control power supply (UVr)
- a5 : The normal operation=IGBT ON

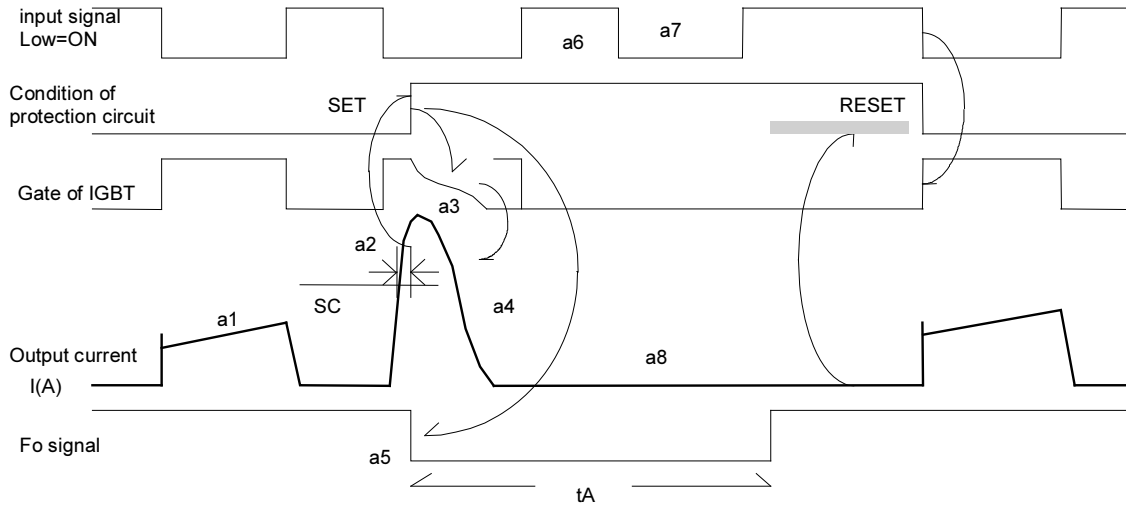
**The operating-sequence of the OT protection**

- a1 : The normal operation=IGBT ON
- a2 : The overheating detection (OTt)
- a3 : IGBT OFF (Even if it makes an input signal to be on)
- a4 : The overheating detection reset (OTr)
- a5 : The normal operation=IGBT ON



The operating-sequence of the SC protection

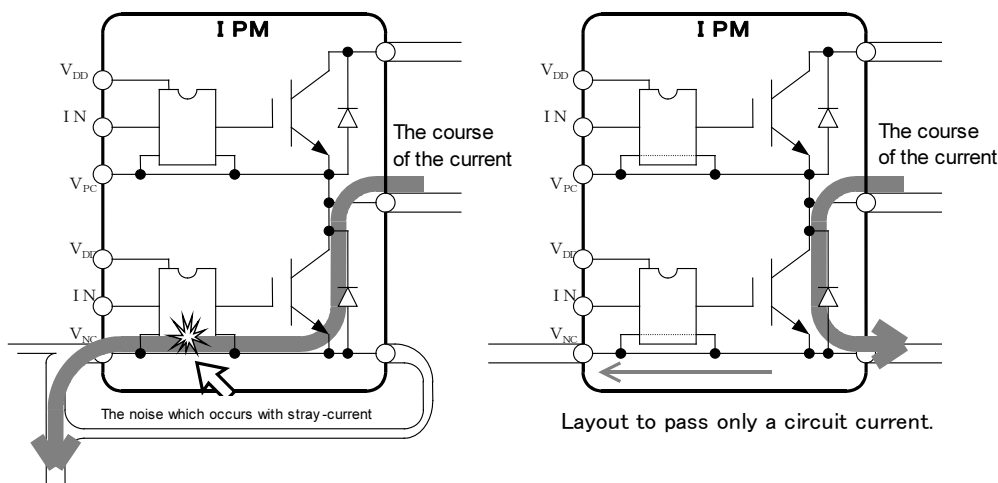
- a1 : The normal operation=IGBT ON
- a2 : Short current detection (SCt)
- a3 : IGBT gate is blocked softly.
- a4 : IGBT turn off gradually.
- a5 : Fo timer start ($t_{Fo}=1.8\text{ms typ.}$)
- a6 : Input signal "H"=OFF
- a7 : Input signal "L"=ON
- a8 : IGBT maintains off. (When a6~a7 occurs at the time which is shorter than t_A)



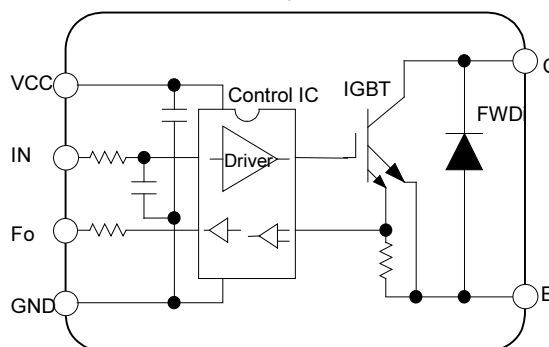
Although IPM has internal protection circuit, it is recommended to ensure the stress which exceeds a maximum rating does not happen repeatedly. Therefore, if received Fo signal, please stop the control signal and stop the operation of IPM. Because IPM doesn't exclude extraordinary cause, it has to be stopped by the system.

9-5 Other notice of using IPM

- (1) The treatment of the terminal not to use
 Type B4LA,B4LB have B and W terminal. Type B5LA,B5LB have B terminal. These terminal aren't connected to the circuit. The pattern can be connected with this terminal. However, pay attention to the wiring. When connecting a pattern with these terminals, the noise might invades IPM via the terminals. Please just leave these terminals open.
 If any phase of the IPM is not used, the corresponded control power supply in the circuit will not use. Please pull-up the corresponded input terminals and make IGBT off. This is to prevent the erroneous turn on of the circuit by noise.
- (2) The connection of the control side GND(V_{NC}/V_{PC}) and output emitter GND (N or U/V/W)
 Do not connect the control side GND and the output emitter GND on the printed circuit board. Otherwise it will be easy to undergo influence by the noise. V_{NC} and the N terminal are connected inside IPM. If connecting V_{NC} and N terminal, the current which should flow through N sometimes flows to V_{NC} . Then, the electric potential difference occurs between N and V_{NC} by parasitic inductance inside and might cause IC malfunction.



- (3) The circuit structure inside
 The IPM is built up with IGBT chip ,FWDi chip, Control IC and the other discreet parts(R,C). Gate of IGBT chip is MOS structure. However, The gate of IGBT chip doesn't directly connect to the control terminal of IPM. VD, Input, Fo and GND terminal are connected to the control IC. It is possible to consider the terminal of IPM to be a bipolar structure. The countermeasure against static electricity like conventional IC with MOS structure is unnecessary to IPM.
 (The handling of IPM is equal to that of a bipolar IC.)



- (4) The parallel operation
 The IPM is not recommended for parallel operation.
 Because the balance of the switching time and the current are not identical, the IPM with larger loss might be thermally damaged because it isn't possible to do the protection-coordination of each IPM.

Power Loss and Junction Temperature

10. Power Loss and Junction Temperature

Junction temperature can be used as an indication of IGBT module situation. This section will discuss how to calculate junction temperature and give an example based on waveform shown in Fig.10.1. Here, only power loss of IGBT part is given. The power loss of Diode can be obtained by using the same method as IGBT part. Moreover, junction temperature must never be outside of the maximum allowable value. It also has impact on the power cycle life.



Fig.10.1

a. Power Loss

In order to estimate junction temperature for thermal design, it is necessary to compute total power loss. The first step is the calculation of power loss per pulse.

Two most important sources of power dissipation that must be considered are conduction losses and switching losses. (Fig.10.2)

(1) Conduction Losses

The total power dissipation during conduction is computed by multiplying the on-state saturation voltage by the on-state current.

$$E_{(sat)} = \frac{I_{c1} \times V_{CE(sat)1} + I_{c2} \times V_{CE(sat)2}}{2} \times t_{w1} \quad (J)$$

Note) The above equation is a simplification of the below one

$$E_{(sat)} = \int_0^{t_{w1}} I_c(t) \cdot V_{CE}(t) dt$$

V_{CE(sat)} VS. I_c characteristics at T_j=125°C is used in power loss calculation.

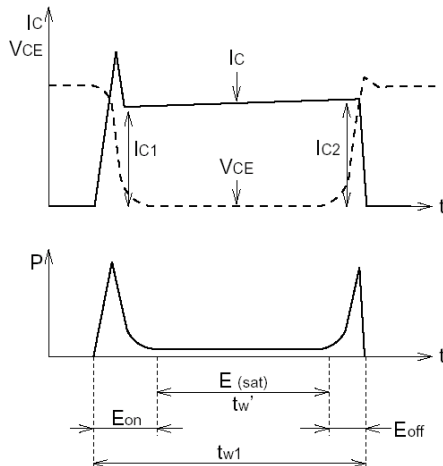


Fig.10.2

(2) Switching Losses

The most accurate method of determining switching losses is to plot the I_c and V_{CE} waveforms during the switching transition. Multiply the waveforms point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy expressed in watt-seconds/pulse or J/pulse.

$$E_{on} = \int_{t_a}^{t_b} I_c(t) \cdot V_{CE}(t) dt = \frac{1}{n} \sum_{n=1}^n P_n \times (t_b - t_a)$$

n: number of partitions

(divide interval between t_a and t_b equally into n parts, compute average power loss for each interval.) Calculation of E_{off} has the same method.

The total power loss of one pulse is the sum of (1) and (2).

$$E_1 = E_{(sat)} + E_{on} + E_{off}$$

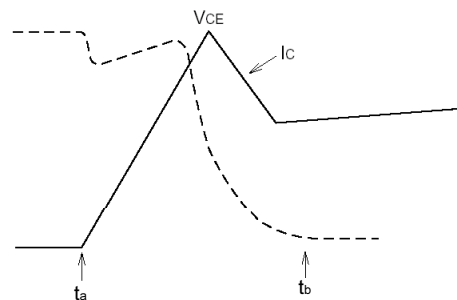


Fig.10.3

Power Loss and Junction Temperature

(3) Average Power Loss

The average power loss per pulse is

$$P_1 = \frac{E_1}{t_{w1}} \quad (\text{W})$$

Fig.10.4 is approximation of Fig.10.1 by using rectangle wave.



Fig.10.4

Average power loss during period of t_{w2} is (See Fig.10.5)

$$P_{av} = \frac{E_1}{t_{w2}} \times N \quad (\text{W})$$

N : pulse numbers in t_{w2} period

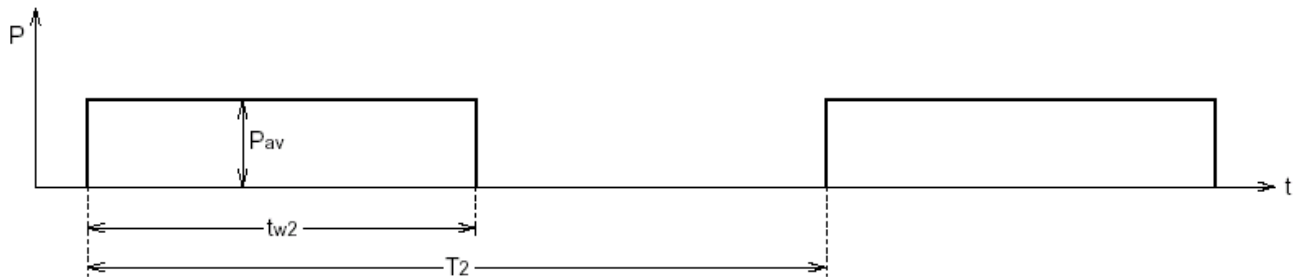


Fig.10.5

Total average power loss is (See Fig.10.6)

$$P_{AV} = P_{av} \times \frac{t_{w2}}{T_2} \quad (\text{W})$$

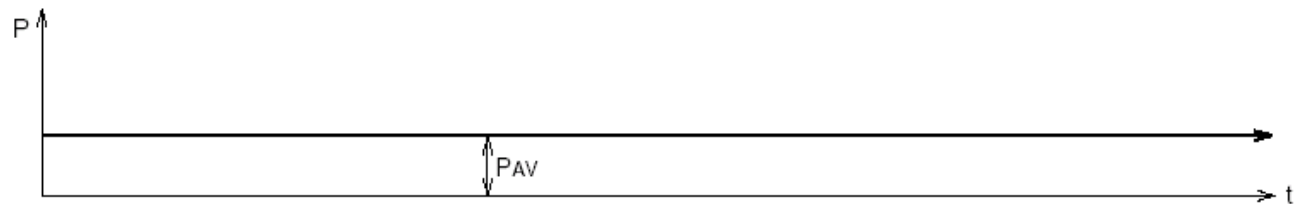


Fig.10.6

b. Junction Temperature Calculation

Junction temperature can be calculated by using P_1 , P_{av} , and P_{AV} that has been obtained so far. Three cases should be considered according to pulse width.

- (1) t_{w1} is short ($t_{w1} \ll 1\text{ms}$)
- (2) Both of t_{w1} and t_{w2} are long ($1\text{ms} < t_{w1} < t_{w2} < 1\text{s}$)
- (3) t_{w2} is longer than 1s. ($t_{w2} > 1\text{s}$)

Power Loss and Junction Temperature

(1) $tw1 \ll 1ms$

In case of short on interval or low duty as in Fig.10.5, Junction temperatures rise to the highest value at the turn-off moment of $tw2$ while the case temperature is stationary. (See Fig.10.7)

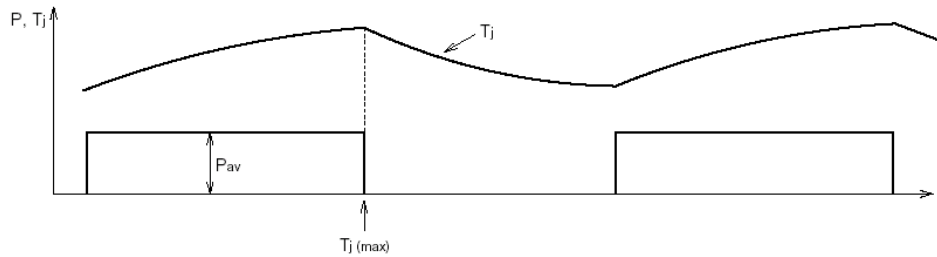


Fig.10.7

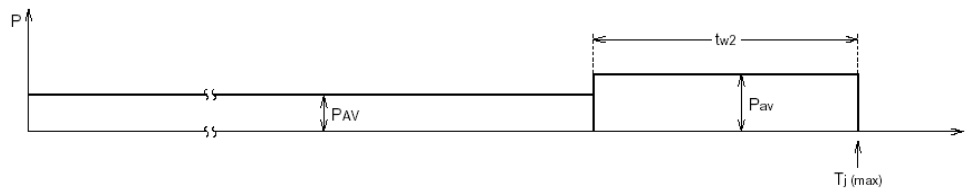


Fig.10.8

Temperature difference between junction and case can be calculated by using the following formula.

$$\Delta T(j-c) = R_{th(j-c)} \times P_{AV} - Z_{th(j-c)(tw2)} \times P_{AV} + Z_{th(j-c)(tw2)} \times P_{av} = R_{th(j-c)} \times P_{AV} + (P_{av} - P_{AV}) \times Z_{th(j-c)(tw2)}$$

$R_{th(j-c)}$ thermal resistance between junction and case

$Z_{th(j-c)(tw2)}$ thermal impedance between junction and case at $tw2$ moment

$$\therefore T_j = T_c + \Delta T(j-c) \quad (T_c \text{ is measured by thermo-couple.})$$

$T_j(max) = 150^\circ C$, therefore the allowable case temperature $T_c(max)$ is, $T_c(max) = 150 - \Delta T(j-c)$.

(2) $1ms < tw1 < tw2 < 1s$

In this case, ripple should be considered in calculation of average power loss $P1$.

Using approximation similar to (1) Fig.10.9 is obtained for calculation.

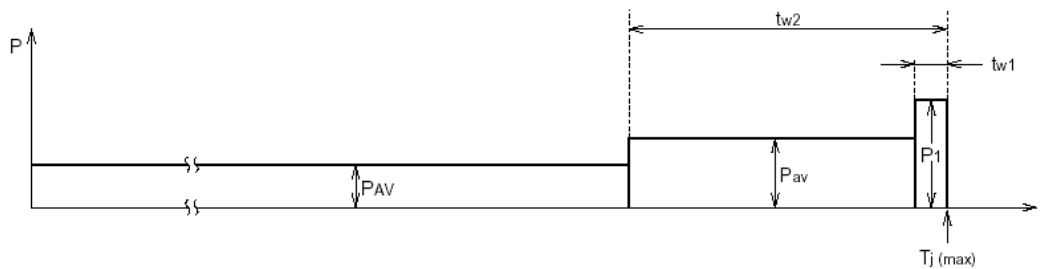


Fig.10.9

$$\Delta T(j-c) = R_{th(j-c)} \times P_{AV} - Z_{th(j-c)(tw2)} \times P_{AV} + Z_{th(j-c)(tw2)} \times P_{av} - Z_{th(j-c)(tw1)} \times P_{av} + Z_{th(j-c)(tw1)} \times P1$$

$$= R_{th(j-c)} \times P_{AV} + (P_{av} - P_{AV}) \times Z_{th(j-c)(tw2)} + (P1 - P_{av}) \times Z_{th(j-c)(tw1)}$$

$R_{th(j-c)}$ thermal resistance between junction and case

$Z_{th(j-c)(tw2)}$ thermal impedance between junction and case at $tw2$ moment

$Z_{th(j-c)(tw1)}$ thermal impedance between junction and case at $tw1$ moment

$$\therefore T_j = T_c + \Delta T(j-c) \quad (T_c \text{ is measured by thermo-couple.})$$

$$T_c(max) = 150 - \Delta T(j-c)$$

Power Loss and Junction Temperature

(3) $tw_2 > 1s$

In a similar way to (2), temperature change of heatsink should be taken into consideration as well. It is necessary to know the transient heat impedance of the heatsink. (Fig.10.9)

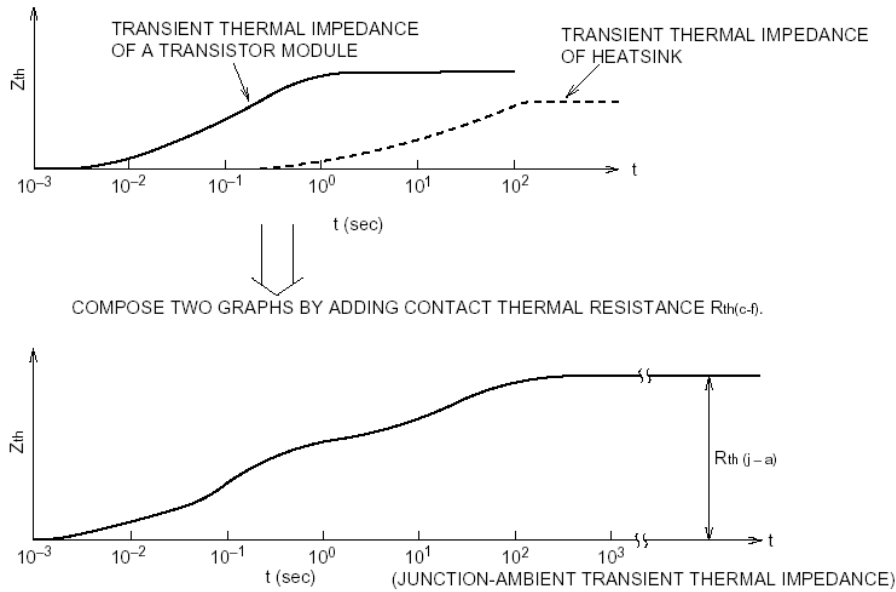


Fig.10.9

Similarly, the temperature difference between junction and ambient can be calculated by using the following formula.

$$\begin{aligned} \Delta T(j-a) &= R_{th(j-a)} \times P_{AV} - Z_{th(j-a)(tw_2)} \times P_{AV} + Z_{th(j-a)(tw_2)} \times P_{av} - Z_{th(j-a)(tw_1)} \times P_{av} + Z_{th(j-a)(tw_1)} \times P_1 \\ &= R_{th(j-a)} \times P_{AV} + (P_{av} - P_{AV}) \times Z_{th(j-c)(tw_2)} + (P_1 - P_{av}) \times Z_{th(j-c)(tw_1)} \\ \therefore T_j &= T_a + \Delta T(j-a) \quad (T_a \text{ is measured by a thermometer.}) \end{aligned}$$

c. Heatsink Selection

Fig.10.10 shows the thermal equivalent circuit when two or more modules are mounted on one heat sink.

According to this equivalent circuit, the temperature of the heat sink is

$$T_f = T_a + (P_{T(AV)} + P_{D(AV)}) \times N \times R_{th(f-a)}$$

T_a : Ambient temperature

$P_{T(AV)}$: Average power loss of IGBT

$P_{D(AV)}$: Average power loss of FWDi

N : Arm number

$R_{th(f-a)}$: The heatsink to ambient thermal resistance

The case temperature T_c is,

$$T_c = T_f + (P_{T(AV)} + P_{D(AV)}) \times R_{th(c-f)}$$

$R_{th(c-f)}$: The case to heatsink thermal resistance

$T_c(\max)$ can be calculated by using the below formula.

$$\therefore T_c(\max) = T_a + (P_{T(AV)} + P_{D(AV)}) \times N \times R_{th(f-a)} + (P_{T(AV)} + P_{D(AV)}) \times R_{th(c-f)}$$

Therefore, the heatsink to ambient thermal resistance can be computed as

$$R_{th(f-a)} = \frac{T_c(\max) - T_a - (P_{T(AV)} + P_{D(AV)}) \times R_{th(c-f)}}{(P_{T(AV)} + P_{D(AV)}) \times N}$$

Moreover, power loss of FWDi should be considered as well. In thermal design, the allowable case temperature $T_c(\max)$ is up to the smaller one of IGBT power loss and FWDi part.

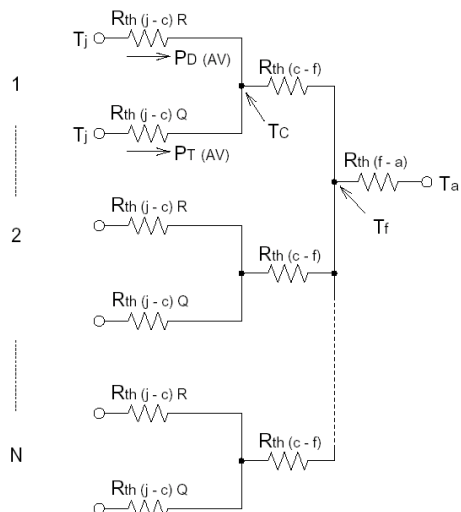


Fig.10.10 Thermal Calculation Model

Average Power Loss Simplified Calculation

11. Average Power Loss Simplified Calculation

(1) VWF Inverter

■Applicability Range

It is applicable to total power loss calculation for selection of IGBTs used in VWF inverters.
It is not applicable in the thermal design of the device (limit design).

■Assumption Condition

- ① PWM modulation used to synthesize sinusoidal output currents in VWF inverters
- ② PWM signal generated by comparing sinusoidal wave to triangular wave
- ③ Duty cycle of PWM among the rank of $\frac{1-D}{2} \sim \frac{1+D}{2}$ (% / 100) D : modulation rate
- ④ Output current of $I_{CP} \cdot \sin x$ without ripple
- ⑤ With inductive load rate of $\cos \theta$

■Calculation Equation

Duty cycle of PWM is constantly changing and its value equal to time $x \frac{1+D \times \sin x}{2}$ at the corresponding moment.

The output current corresponds to the output voltage change and this relationship is represented by power factor $\cos \theta$.
Therefore, the duty cycle of PWM corresponding to output current at arbitrary phase x is

$$\text{Output current} = I_{CP} \times \sin x$$

$$\text{PWM Duty} = \frac{1 + D \times \sin(x + \theta)}{2}$$

$V_{CE(sat)}$ and V_{EC} at this moment are

$$V_{ce(sat)} = V_{ce(sat)}(@ I_{CP} \times \sin x)$$

$$V_{ec} = V_{ec}(@ (-1) \times I_{CP} (= I_{CP}) \times \sin x)$$

Static power loss of IGBT is

$$\frac{1}{2\pi} \int_0^{\pi} (I_{CP} \times \sin x) \times V_{ce(sat)}(@ I_{CP} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \cdot dx$$

Similarly, static power loss of FWDi is

$$\frac{1}{2\pi} \int_{\pi}^{2\pi} ((-1) \times I_{CP} \times \sin x) \times (V_{ec}(@ (-1) \times I_{CP} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2}) \cdot dx$$

On the other hand, dynamic power loss of IGBT is not dependent on the PWM duty and can be expressed as the following formula.

$$\frac{1}{2\pi} \int_0^{\pi} (P_{sw(on)}(@ I_{CP} \times \sin x) + P_{sw(off)}(@ I_{CP} \times \sin x)) \times fc \cdot dx$$

As for dynamic power loss of free-wheeling diode, calculation is given by an example of ideal diode shown in Fig.11.1.

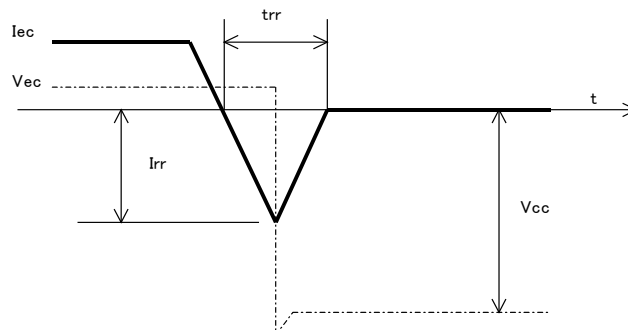


Fig.11.1 Dynamic Power Loss of FWDi

Average Power Loss Simplified Calculation

$$P_{sw} = \frac{I_{rr} \times V_{cc} \times trr}{4}$$

Because reverse recovery of free-wheeling diodes occurs in half cycle of the output current, the dynamic power loss of FWDi is

$$\begin{aligned} & \frac{1}{2} \int_{\pi}^{2\pi} \frac{I_{rr}(@I_{cp} \times \sin x) \times V_{cc} \times trr(@I_{cp} \times \sin x)}{4} \times fc \bullet dx \\ &= \frac{1}{8} \int_{\pi}^{2\pi} I_{rr}(@I_{cp} \times \sin x) \times V_{cc} \times trr(@I_{cp} \times \sin x) \times fc \bullet dx \end{aligned}$$

■ Inverter Loss Calculation Notes

- Divide one cycle of output current into many equal intervals, then calculate actual "PWM duty", "Output current", and " $V_{CE(sat)}$ ", V_{EC} , and P_{sw} responding to the current" in each interval. The power loss during one cycle is the sum of each interval.
- The PWM duty depends on the method of generating the signal.
- The output current waveform and the relationship between output current and PWM duty cycle are dependent on signal generator, load and other factors. Therefore, calculation should always be done with actual waveforms.
- $V_{CE(sat)}$ uses the value of $T_j=125^{\circ}\text{C}$.
- P_{sw} uses the value under half bridge operating case at $T_j=125^{\circ}\text{C}$.

■ Thermal Design Notes

- ① It is necessary to examine the worst switching condition.
- ② Consideration of temperature variation due to current cycle should be given in thermal design.
(Temperature variation rate is 30% to 35% for 60Hz case. When the output current of several Hz switches for a few seconds, it almost has equal temperature to a direct current with the same peak value continuously flowing.)
- ③ Temperature ripple caused by switching operation should be considered especially when switching frequency is much lower than 10kHz.

Notice for safe Designs and when Using This Specification

12. Notice for safe Designs and when Using This Specification

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