

<HVIC>

# M81734FP

600V HIGH VOLTAGE HALF BRIDGE DRIVER

## DESCRIPTION

M81734FP is high voltage Power MOSFET and IGBT gate driver for half bridge applications.

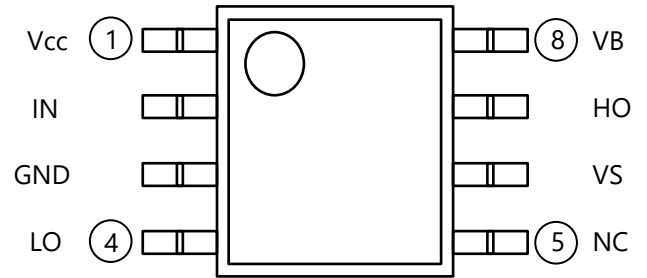
## FEATURES

- FLOATING SUPPLY VOLTAGE .....600V
- OUTPUT CURRENT .....±500mA
- SINGLE INPUT TYPE
- INTERNALLY SET DEADTIME
- HALF BRIDGE DRIVER
- UNDERVOLTAGE LOCKOUT
- SOP-8 PACKAGE

## APPLICATIONS

MOSFET and IGBT module inverter driver for PDP, HID lamp, refrigerator, air-conditioner, washing machine, AC servomotor and general purpose.

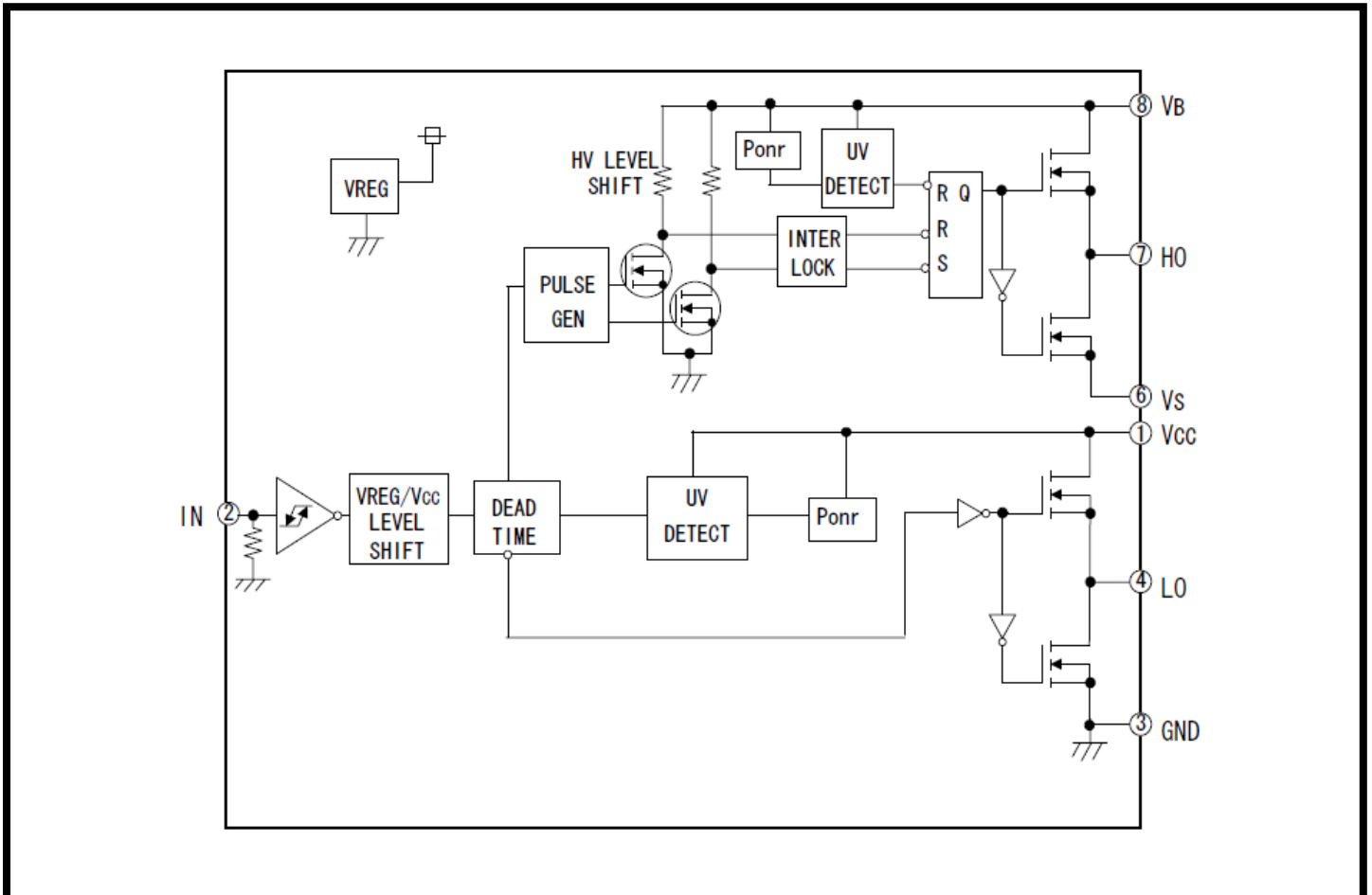
## PIN CONFIGURATION (TOP VIEW)



Outline: SOP8

NC: NO CONNECTION

## BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS (Ta = 25°C unless otherwise specified)

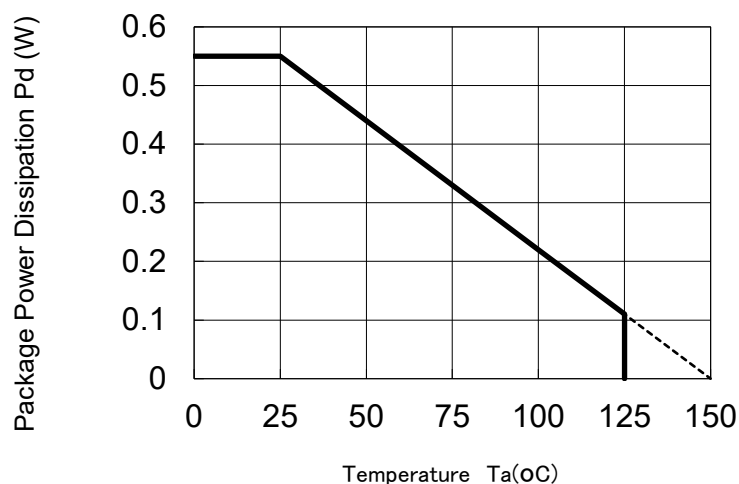
Symbol	Parameter	Test conditions	Ratings	Unit
V <sub>B</sub>	High Side Floating Supply Absolute Voltage		-0.5 ~ 624	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage		V <sub>B</sub> -24 ~ V <sub>B</sub> +0.5	V
V <sub>BS</sub>	High Side Floating Supply Voltage	V <sub>BS</sub> =V <sub>B</sub> -V <sub>S</sub>	-0.5 ~ 24	V
V <sub>HO</sub>	High Side Output Voltage		V <sub>S</sub> -0.5 ~ V <sub>B</sub> +0.5	V
V <sub>CC</sub>	Low Side Fixed Supply Voltage		-0.5 ~ 24	V
V <sub>LO</sub>	Low Side Output Voltage		-0.5 ~ V <sub>CC</sub> +0.5	V
V <sub>IN</sub>	Logic Input Voltage		-0.5 ~ V <sub>CC</sub> +0.5	V
dV <sub>S</sub> /dt	Allowable Offset Voltage Transient		±50	V/ns
P <sub>d</sub>	Package Power Dissipation	Ta= 25 °C ,On Board	0.55	W
Kθ	Linear Derating Factor	Ta> 25 °C ,On Board	4.4	mW/°C
R <sub>th(j-c)</sub>	Junction-Case Thermal Resistance		50	°C/W
T <sub>j</sub>	Junction Temperature		-20 ~ +150	°C
T <sub>opr</sub>	Operation Temperature		-20 ~ +125	°C
T <sub>stg</sub>	Storage Temperature	On Board	-40 ~ +150	°C
TL	Solder Heatproof	RoHS Correspondence	255:10s,max 260	°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>B</sub>	High Side Floating Supply Absolute Voltage		V <sub>S</sub> +10	—	V <sub>S</sub> +20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	V <sub>B</sub> >10V	0	—	500	V
V <sub>BS</sub>	High Side Floating Supply Voltage	V <sub>BS</sub> =V <sub>B</sub> -V <sub>S</sub>	10	—	20	V
V <sub>HO</sub>	High Side Output Voltage		V <sub>S</sub>	—	V <sub>B</sub>	V
V <sub>CC</sub>	Low Side Fixed Supply Voltage		10	—	20	V
V <sub>LO</sub>	Low Side Output Voltage		0	—	V <sub>CC</sub>	V
V <sub>IN</sub>	Logic Input Voltage		0	—	V <sub>CC</sub>	V

Note: For proper operation, the device should be used within the recommended conditions

## THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)



# M81734FP

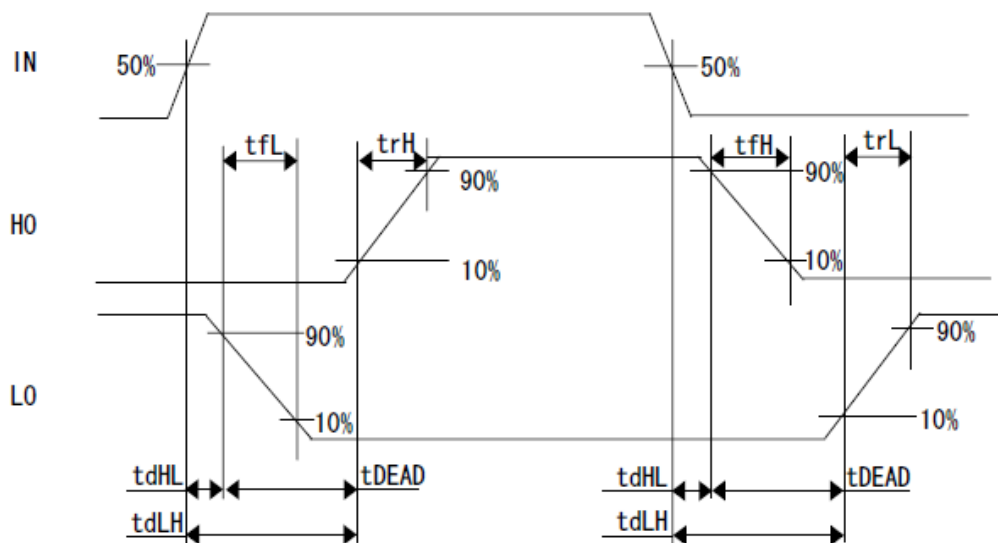
600V HIGH VOLTAGE HALF BRIDGE DRIVER

## ELECTRICAL CHARACTERISTICS (Ta=25°C, VCC=VBS (=VB-VS)=15V, unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
I <sub>FS</sub>	Floating Supply Leakage Current	V <sub>B</sub> = V <sub>S</sub> = 600V	—	—	1.0	uA
I <sub>BS</sub>	V <sub>BS</sub> Standby Current	I <sub>N</sub> = 0V	—	0.2	0.5	mA
I <sub>CC</sub>	V <sub>CC</sub> Standby Current	I <sub>N</sub> = 0V	0.2	0.5	0.75	mA
V <sub>OH</sub>	High Level Output Voltage	I <sub>O</sub> = 0mA, LO, HO	13.8	14.4	—	V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>O</sub> = 0mA, LO, HO	—	—	0.1	V
V <sub>IH</sub>	High Level Input Threshold Voltage		1.6	2.2	2.7	V
V <sub>IL</sub>	Low Level Input Threshold Voltage		0.8	1.55	2.1	V
I <sub>IH</sub>	High Level Input Bias Current	V <sub>IN</sub> = 3V	—	15	45	uA
I <sub>IL</sub>	Low Level Input Bias Current	V <sub>IN</sub> = 0V	—	—	1	uA
V <sub>BSuvr</sub>	V <sub>BS</sub> Supply UV Reset Voltage		7.0	8.4	9.8	V
V <sub>BSuvh</sub>	V <sub>BS</sub> Supply UV Hysteresis Voltage		0.3	0.5	—	V
t <sub>VBSuv</sub>	V <sub>BS</sub> Supply UV Filter Time		—	7.5	—	us
V <sub>CCuvr</sub>	V <sub>CC</sub> Supply UV Reset Voltage		7.0	8.4	9.8	V
V <sub>CCuvh</sub>	V <sub>CC</sub> Supply UV Hysteresis Voltage		0.3	0.5	—	V
t <sub>VCCuv</sub>	V <sub>CC</sub> Supply UV Filter Time		—	7.5	—	us
I <sub>OH</sub>	Output High Level Short Circuit Pulsed Current	V <sub>O</sub> = 0V, PW < 10us	—	-500	—	mA
I <sub>OL</sub>	Output Low Level Short Circuit Pulsed Current	V <sub>O</sub> = 15V, PW < 10us	—	500	—	mA
R <sub>OH</sub>	Output High Level On Resistance	I <sub>O</sub> = -200mA, R <sub>OH</sub> = (V <sub>OH</sub> -V <sub>O</sub> )/I <sub>O</sub>	—	30	—	W
R <sub>OL</sub>	Output Low Level On Resistance	I <sub>O</sub> = 200mA, R <sub>OL</sub> = V <sub>O</sub> /I <sub>O</sub>	—	12	—	W
t <sub>DEAD</sub>	Dead Time LO Turn-Off to HO Turn-On & HO Turn-Off to LO Turn-On	CL = 1000pF between HO-V <sub>S</sub> , LO-GND, V <sub>IN</sub> = 0~3V	0.5	—	1.00	us
V <sub>Ponr</sub>	Power On Reset Voltage		—	—	6	V
t <sub>Ponr(FIL)</sub>	Power On Reset Filter Time		300	—	—	ns
t <sub>dLH</sub>	Turn-On Propagation Delay	CL = 1000pF between HO-V <sub>S</sub> , LO-GND, V <sub>IN</sub> = 0~3V	0.6	0.9	1.2	us
t <sub>dHL</sub>	Turn-Off Propagation Delay	CL = 1000pF between HO-V <sub>S</sub> , LO-GND, V <sub>IN</sub> = 0~3V	0.1	0.15	0.25	us
t <sub>rH</sub>	High Side Turn-On Rise Time	CL = 1000pF between HO-V <sub>S</sub>	—	75	180	ns
t <sub>fH</sub>	High Side Turn-Off Fall Time	CL = 1000pF between HO-V <sub>S</sub>	—	75	180	ns
t <sub>rL</sub>	Low Side Turn-On Rise Time	CL = 1000pF between LO-GND	—	75	180	ns
t <sub>fL</sub>	Low Side Turn-Off Fall Time	CL = 1000pF between LO-GND	—	75	180	ns

\*1 Typ. is not specified.

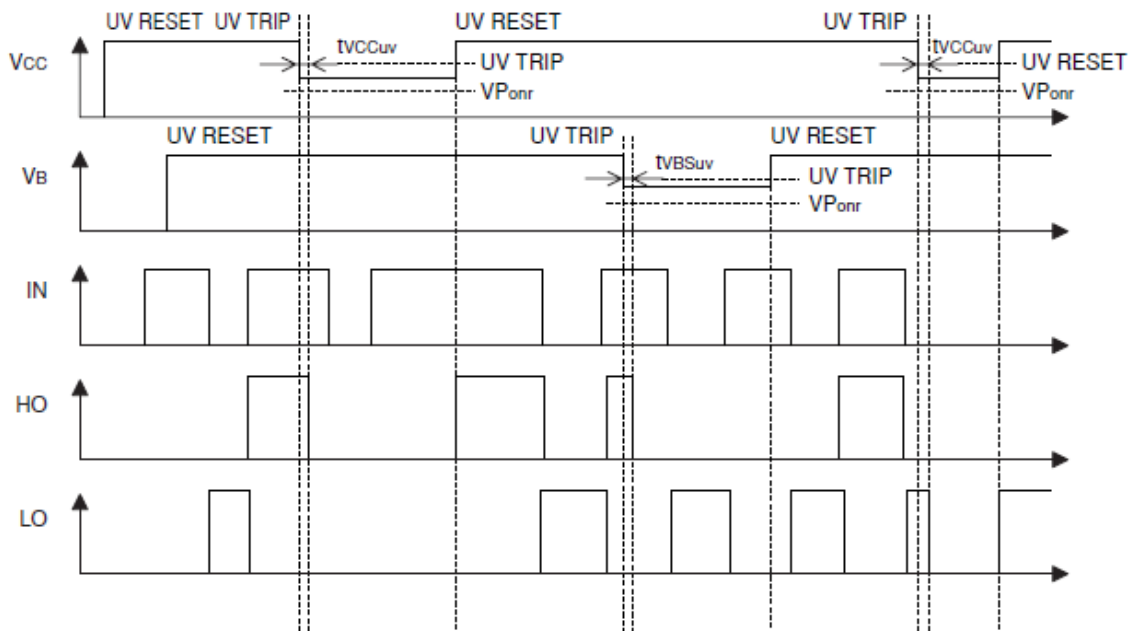
## INPUT/OUTPUT TIMING DIAGRAM



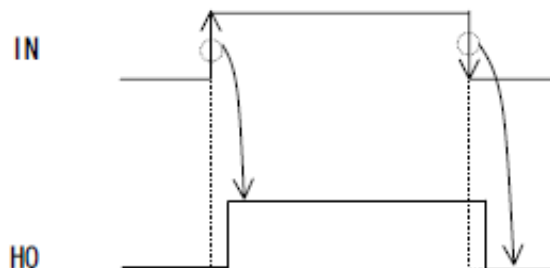
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## FUNCTION TIMING DIAGRAM



1. HO has positive logic with reference to IN. LO has negative logic with reference to IN.
2. Output signal (HO) is triggered by the edge of input signal.



### 3. Logic During UV( $V_{CC}$ , $V_{BS}$ ) Error

Error Signal	HO	LO
UV error ( $V_{CC}$ )	HO is locked at "L" level as long as UV error for $V_{CC}$ is detected. After $V_{CC}$ UV reset level, the lock for HO is removed following an "L" state of the IN signal, and then HO responds to the input. ( $V_{CC} > V_{BS}$ )	LO is locked at "L" level as long as UV error for $V_{CC}$ is detected. After $V_{CC}$ exceeds $V_{CC}$ UV reset level, the lock for LO is removed and responds to IN signal.
UV error ( $V_{BS}$ )	HO is locked at "L" level as long as UV error for $V_{BS}$ is detected. After $V_{BS}$ UV reset level, the lock for HO is removed following an "L" state of the IN signal, and then HO responds to the input.	LO is independent of $V_{BS}$ to respond to IN.

\*If UV error for  $V_{CC}$  is detected when HO is in "H" level and the falling speed of  $V_{CC}$  is exceeds  $0.03V/\mu s$ , the off signal for HO might not be transmitted from low side to high side and then HO stays "H".

\*If supply voltage drops lower than  $V_{Ponr}$ , output becomes "L" not after  $t_{VCCuv}$  or  $t_{VBSuv}$  but after  $t_{Ponr}(FIL)$ .

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### 4. Supply start up sequence

Please start up  $V_{CC}$  supply and  $V_{BS}$  supply in that order, and, please shut down  $V_{BS}$  supply and  $V_{CC}$  supply in that order. Please start up  $V_{CC}$  supply and  $V_{BS}$  supply with gentle slope. If you start up supply with sharp slope, there is some possibility that HO or LO outputs "H" for a moment.

If  $V_{CC}$  supply is less than 10V(outside of RECOMMENDED OPERATING CONDITIONS), there is some possibility that output does not change in response to input. Please evaluate carefully about supply start up or restart after shut down in your application systems.

### ENVIRONMENTAL CONSCIOUSNESS

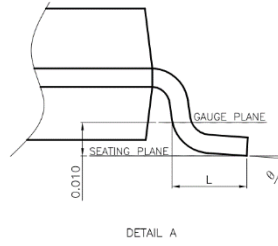
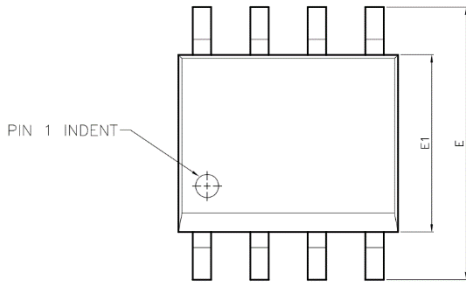
M81734FP is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU+(EU)2015/863.

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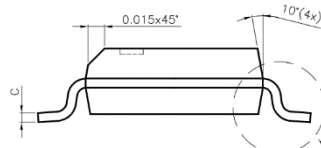
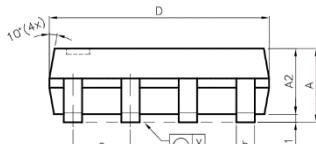
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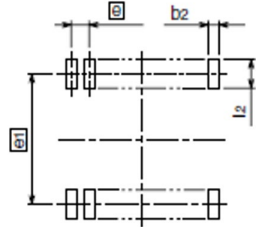
## PACKAGE OUTLINE



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.47	1.60	1.73
A1	0.10	—	0.25
A2	—	1.45	—
b	0.33	0.41	0.51
C	0.19	0.20	0.25
D	4.80	4.85	4.95
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	—	1.27	—
L	0.40	0.71	1.27
y	—	—	0.076
φ	0°	—	8°



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
e1	—	5.23	—
l2	1.27	—	—
e	—	1.27	—
b2	—	0.76	—



Recommended Mount Pad

The above is one example.  
Please design the mount pad with your evaluation.



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