

<Full SiC Power Modules>

FMF400DY-24B

HIGH POWER SWITCHING USE
INSULATED TYPE



Dual switch (Half-Bridge)

Drain current I_D **400 A**
 Drain-Source voltage V_{DSX} **1200 V**
 Maximum junction temperature T_{vjmax} **175 °C**

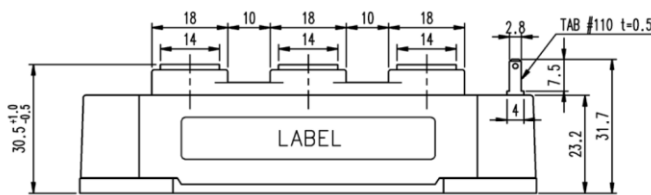
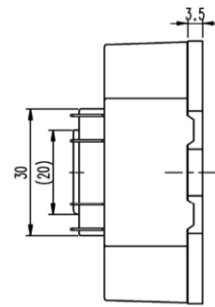
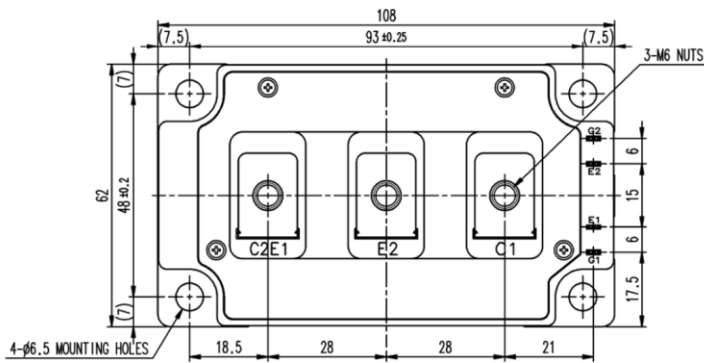
- Silicon Carbide MOSFET + Silicon Carbide Schottky Barrier Diode
- Flat base Type
- Copper base plate
- RoHS Directive compliant
- Recognized under UL1557, File E323585

APPLICATION

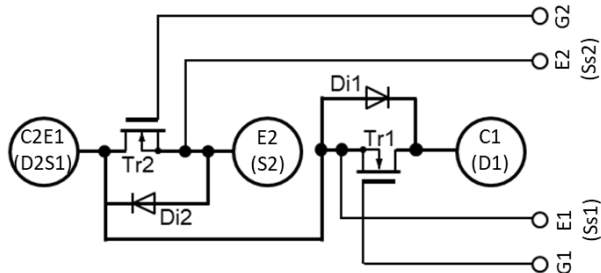
Power supply, etc.

OUTLINE DRAWING & INTERNAL CONNECTION

Dimension in mm



INTERNAL CONNECTION



Tolerance otherwise specified

Division of Dimension	Tolerance
0.5 to 3	±0.2
over 3 to 6	±0.3
over 6 to 30	±0.5
over 30 to 120	±0.8
over 120 to 400	±1.2

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MAXIMUM RATINGS ($T_{vj}=25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Item	Conditions	Rating	Unit
V_{DSX}	Drain-source voltage	$V_{GS}=-15\text{ V}$	1200	V
V_{GSS}	Gate-source voltage	D-S short-circuited	± 20	V
I_D	Drain current	DC, $T_C=36\text{ }^{\circ}\text{C}$ (Note.2)	400	A
I_{DRM}		Pulse, Repetitive (Note.3)	800	
P_{tot}	Total power dissipation	$T_C=25\text{ }^{\circ}\text{C}$ (Note.2)	1360	W
I_S (Note.1)	Source current	DC	400	A
I_{SRM} (Note.1)		Pulse, Repetitive (Note.3)	800	
V_{iso1}	Isolation voltage	Terminals to base plate, RMS, $f=60\text{ Hz}$, AC 1 min	4000	V
T_{vjmax}	Maximum junction temperature	Instantaneous event (overload) (Note.9)	175	$^{\circ}\text{C}$
T_{vjop}	Operating junction temperature	Continuous operation (under switching) (Note.9)	$-40\sim+150$	$^{\circ}\text{C}$
T_{cmax}	Maximum case temperature	(Note.2,9)	125	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-	$-40\sim+125$	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{vj}=25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Item	Conditions (note. 8)	Limits			Unit	
			Min.	Typ.	Max.		
I_{DSX}	Drain-source cut-off current	$V_{DS}=V_{DSX}$, $V_{GS}=-15\text{ V}$	-	-	4	mA	
		$V_{DS}=800\text{ V}$, $V_{GS}=-15\text{ V}$	-	-	0.4		
$V_{GS(th)}$	Gate-source threshold voltage	$I_D=107\text{ mA}$, $V_{DS}=10\text{ V}$	1.8	2.5	3.2	V	
I_{GSS}	Gate-source leakage current	$V_{GS}=V_{GSS}$, D-S short-circuited	-	-	0.5	μA	
$V_{DS(on)}$ (terminal)	Drain-source on-state voltage	$I_D=400\text{ A}$, $V_{GS}=15\text{ V}$ (Note.6)	$T_{vj}=25\text{ }^{\circ}\text{C}$	-	1.75	2.45	V
			$T_{vj}=125\text{ }^{\circ}\text{C}$	-	2.25	-	
			$T_{vj}=150\text{ }^{\circ}\text{C}$	-	2.35	-	
$V_{DS(on)}$ (chip)	Drain-source on-state voltage	$I_D=400\text{ A}$, $V_{GS}=15\text{ V}$ (Note.6)	$T_{vj}=25\text{ }^{\circ}\text{C}$	-	1.45	-	V
			$T_{vj}=125\text{ }^{\circ}\text{C}$	-	1.95	-	
			$T_{vj}=150\text{ }^{\circ}\text{C}$	-	2.05	-	
$r_{DS(on)}$ (chip)	Drain-source on-state resistance	$I_D=400\text{ A}$, $V_{GS}=15\text{ V}$ (Note.6)	$T_{vj}=25\text{ }^{\circ}\text{C}$	-	3.6	-	m Ω
			$T_{vj}=125\text{ }^{\circ}\text{C}$	-	4.9	-	
			$T_{vj}=150\text{ }^{\circ}\text{C}$	-	5.1	-	
C_{iss}	Input capacitance	$V_{DS}=10\text{ V}$, $V_{GS}=0\text{ V}$	-	32	-	nF	
C_{oss}	Output capacitance		-	23	-		
C_{rss}	Reverse transfer capacitance		-	1.6	-		
Q_G	Gate charge	$V_{DD}=600\text{ V}$, $I_D=400\text{ A}$, $V_{GS}=0\rightarrow 15\text{ V}$	-	914	-	nC	
$t_{d(on)}$	Turn-on delay time	$V_{DD}=600\text{ V}$, $I_D=400\text{ A}$, $V_{GS}=\pm 15\text{ V}$, $T_{vj}=150\text{ }^{\circ}\text{C}$, $R_{G(on)}=1.5\Omega$, $R_{G(off)}=2.2\Omega$, $L_{s_ext}=25\text{ nH}$, Inductive load, per pulse	-	140	-	ns	
t_r	Rise time		-	65	-		
$t_{d(off)}$	Turn-off delay time		-	185	-		
t_f	Fall time		-	40	-		
E_{on}	Turn-on switching energy		-	12	-		mJ
E_{off}	Turn-off switching energy		-	9	-		
Q_C	Drain-source charge		-	3	-		μC
V_{SD} (Note.1) (terminal)	Source-drain voltage	$I_S=400\text{ A}$ (Note.6) $V_{GS}=-15\text{ V}$	$T_{vj}=25\text{ }^{\circ}\text{C}$	-	1.95	2.60	V
			$T_{vj}=125\text{ }^{\circ}\text{C}$	-	2.80	-	
			$T_{vj}=150\text{ }^{\circ}\text{C}$	-	3.00	-	
V_{SD} (Note.1) (chip)	Source-drain voltage	$I_S=400\text{ A}$ (Note.6) $V_{GS}=-15\text{ V}$	$T_{vj}=25\text{ }^{\circ}\text{C}$	-	1.65	-	V
			$T_{vj}=125\text{ }^{\circ}\text{C}$	-	2.50	-	
			$T_{vj}=150\text{ }^{\circ}\text{C}$	-	2.70	-	
$R_{DD'+SS'}$	Internal lead resistance	D1-Ss1, D2S1-Ss2 terminals, per switch	-	0.75	-	m Ω	
L_s	Internal stray inductance	Across P-N terminals	-	21	-	nH	
r_g	Internal gate resistance	Per switch	-	2.5	-	Ω	

Caution: Short-circuit capability is not designed.

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THERMAL RESISTANCE CHARACTERISTICS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal resistance ^(Note. 2)	Junction to case, per inverter switch	-	-	110	K/kW
$R_{th(j-c)D}$		Junction to case, per inverter FWD	-	-	150	
$R_{th(c-s)}$	Contact thermal resistance ^(Note.2)	Case to heat sink, per 1 module, Thermal grease applied ^(Note.7, 9)	-	10	-	K/kW

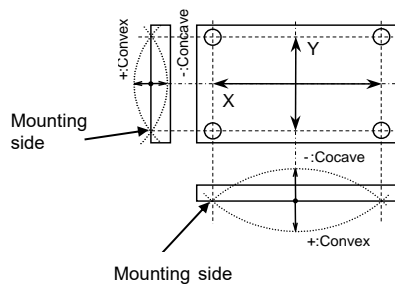
MECHANICAL CHARACTERISTICS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
M_t	Mounting torque	Main terminals M 6 screw	3.5	4.0	4.5	N·m
M_s		Mounting to heat sink M 6 screw	3.5	3.0	4.5	
m	mass	-	-	400	-	g
d_a	Clearance	Terminal to terminal	11	-	-	mm
		Terminal to base plate	29	-	-	
d_s	Creepage distance	Terminal to terminal	20	-	-	mm
		Terminal to base plate	37	-	-	
e_c	Flatness of base plate	On the centerline X, Y ^(Note.5)	-100	-	100	μm

*: This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU and (EU)2015/863.

Note1. Represent ratings and characteristics of the anti-parallel, source-drain free wheeling diode (FWD).

- Case temperature (T_c) and heat sink temperature (T_s) are defined on the each surface (mounting side) of base plate and heat sink just under the chips. Refer to the figure of chip location.
- Pulse width and repetition rate should be such that the device junction temperature (T_{vj}) does not exceed T_{vjmax} rating.
- Junction temperature (T_{vj}) should not increase beyond T_{vjmax} rating.
- The base plate (mounting side) flatness measurement points (X, Y) are as follows of the following figure.



- Pulse width and repetition rate should be such as to cause negligible temperature rise.
- Typical value is by thermally conductive grease of $\lambda=0.9 \text{ W/(m}\cdot\text{K)}/D_{(c-s)}=100\mu\text{m}$.
- Per switch
- Long term performance related to thermal conductive grease (including but not limited to aspects such as the increase of thermal resistance due to pumping out, etc.) should be verified under your specific application conditions. Each temperature condition (T_{vjmax} , T_{vjop} , T_{Cmax}) must be maintained below the maximum rated temperature throughout consideration of the temperature rise even for long term usage.

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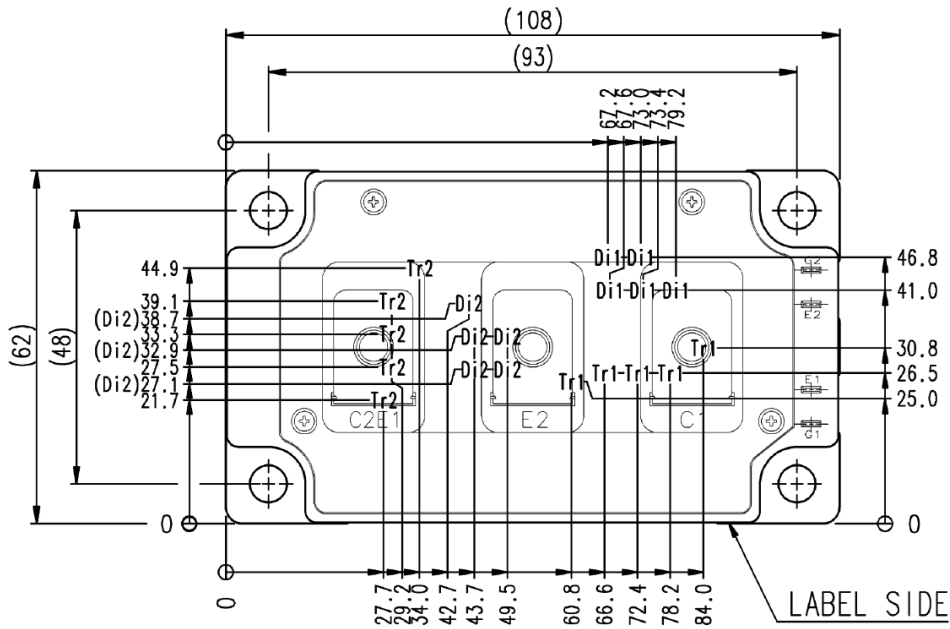
RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Conditions	Limits			Unit	
			Min.	Typ.	Max.		
V_{DD}	(DC) Supply voltage	Applied across D1-S2 terminals	-	600	850	V	
$V_{GS(+)}$	Gate-Source positive drive voltage	Applied across G1-Ss1, G2-Ss2 terminals	13.5	15.0	16.5	V	
$V_{GS(-)}$	Gate-Source negative drive voltage	Applied across G1-Ss1, G2-Ss2 terminals	-16.5	-15.0	-7.0	V	
$R_{G(on)}$	External gate resistance (Note.10)	Per switch	1.5	-	7.5	Ω	
$R_{G(off)}$			2.2	-	11.0		
f_c	Switching frequency	$V_{GS(+)}=15V, R_{G(on)}=1.5\Omega, R_{G(off)}=2.2\Omega$ $V_{DD}=600V, T_{vj}=150^\circ C$	$V_{GS(-)} < -10V$	-	-	50	kHz
			$V_{GS(-)} \geq -10V$	-	-	100	

Note 10. The value of external gate resistance should be considered the surge voltage not to exceed the rating voltage in the worst system condition.

CHIP LOCATION (Top view)

Dimension in mm, tolerance: ± 1 mm

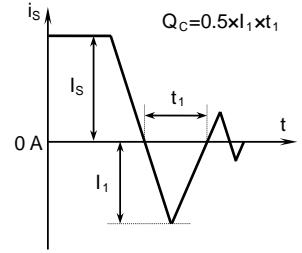
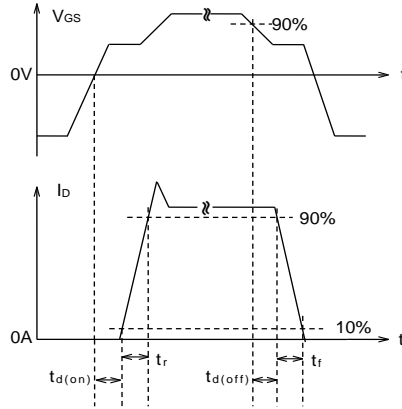
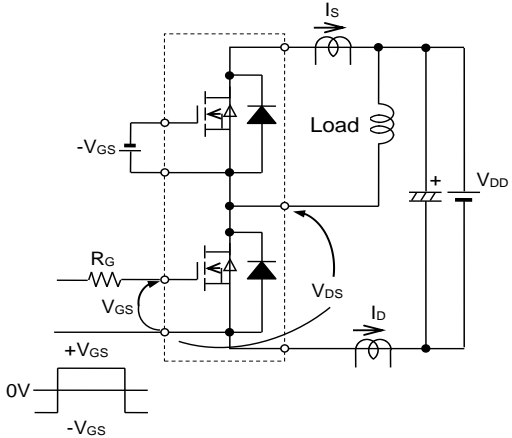


Tr1,Tr2: SiC-MOSFET, Di1,Di2: SiC-SBD

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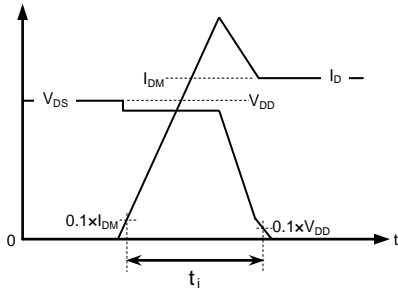
HIGH POWER SWITCHING USE
INSULATED TYPE

TEST CIRCUIT AND WAVEFORMS

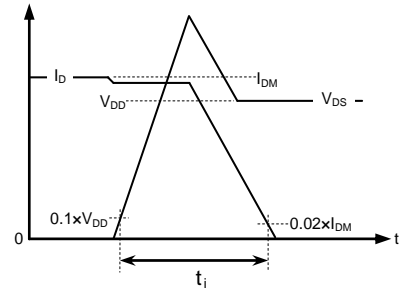


Switching characteristics test circuit and waveforms

Q_C test waveform



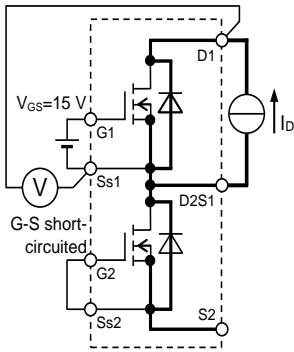
MOSFET Turn-on switching energy



MOSFET Turn-off switching energy

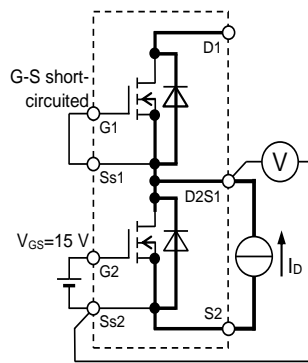
Turn-on / Turn-off switching energy test waveforms (Integral time instruction drawing)

TEST CIRCUIT

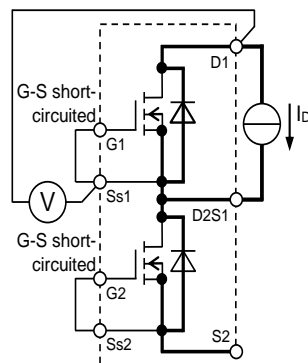


Tr1

$V_{DS(on)}$ test circuit

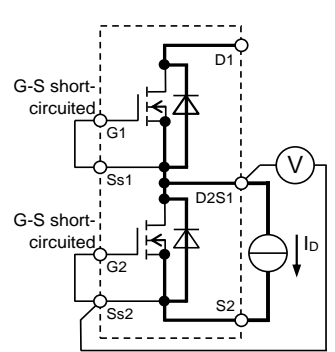


Tr2



Di1

V_{SD} test circuit



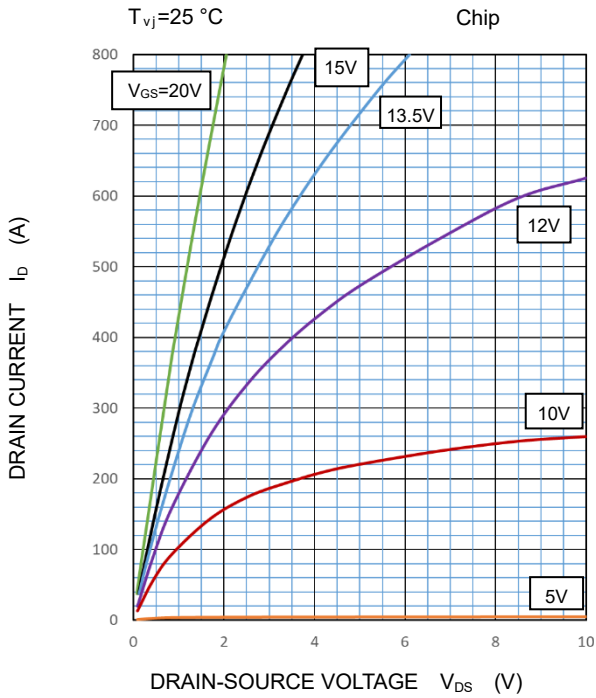
Di2

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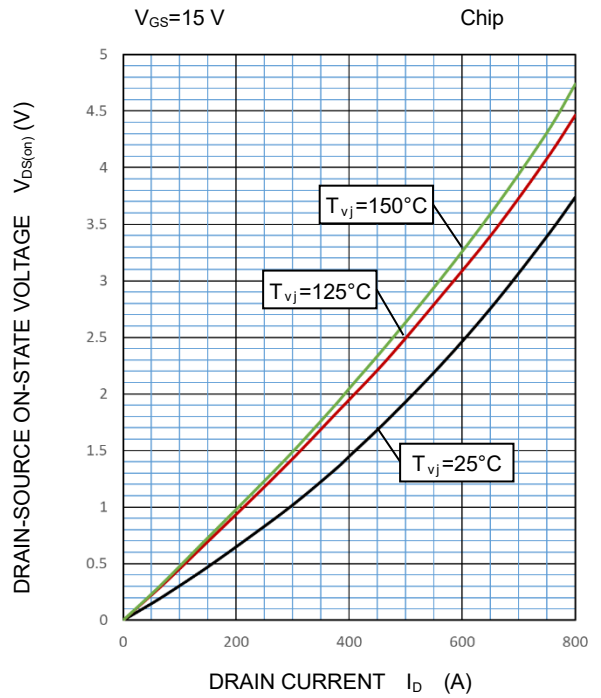
HIGH POWER SWITCHING USE
INSULATED TYPE

PERFORMANCE CURVES

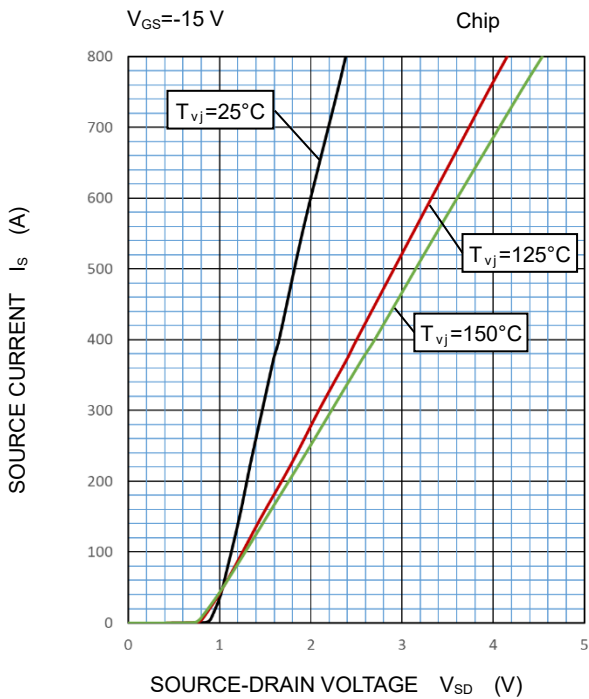
OUTPUT CHARACTERISTICS (TYPICAL)



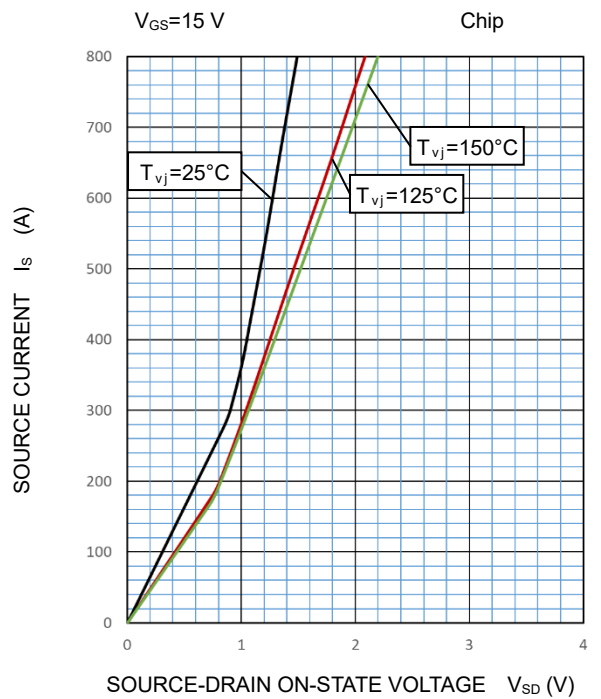
DRAIN-SOURCE ON STATE VOLTAGE CHARACTERISTICS (TYPICAL)



FREE WHEELING DIODE FORWARD CHARACTERISTICS (TYPICAL)



SOURCE-DRAIN ON STATE VOLTAGE CHARACTERISTICS (TYPICAL)



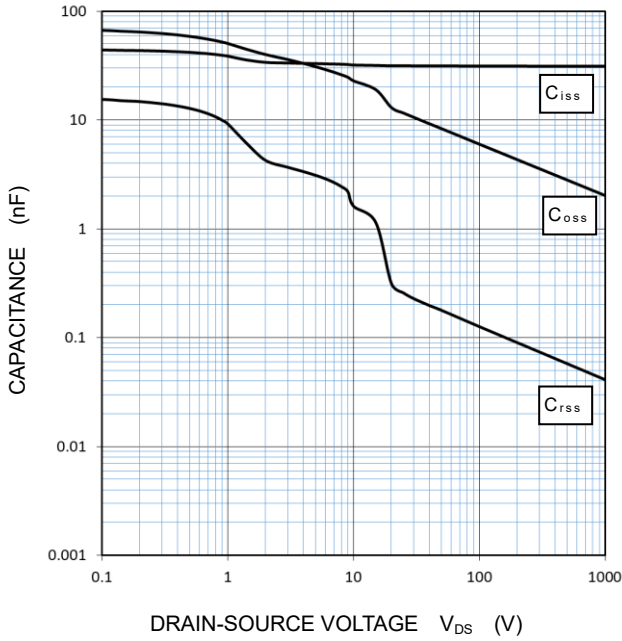
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PERFORMANCE CURVES

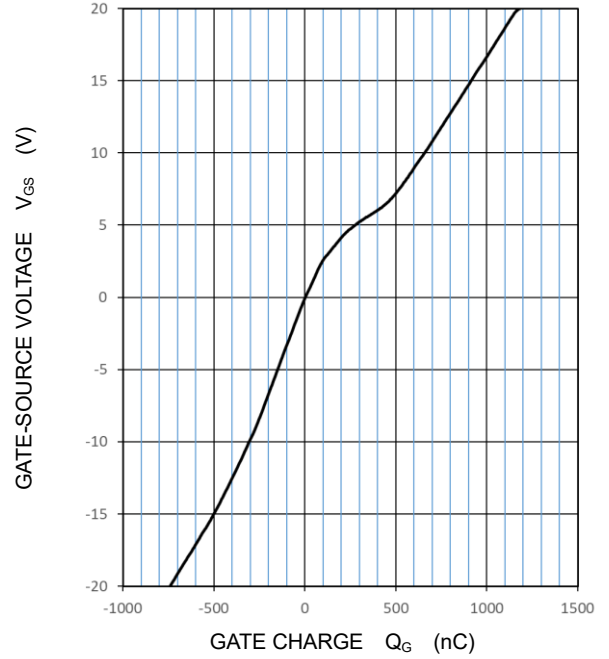
CAPACITANCE CHARACTERISTICS (TYPICAL)

$V_{GS}=0V, T_{vj}=25\text{ }^{\circ}C$



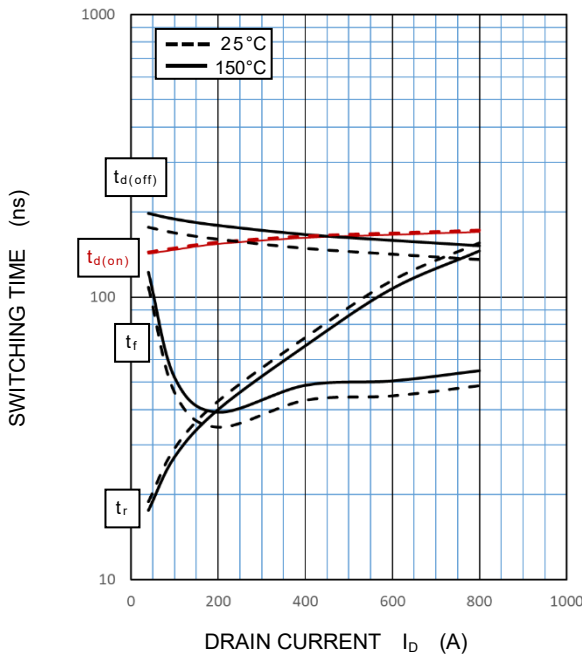
GATE CHARGE CHARACTERISTICS (TYPICAL)

$V_{DD}=600V, I_D=400A, T_{vj}=25\text{ }^{\circ}C$



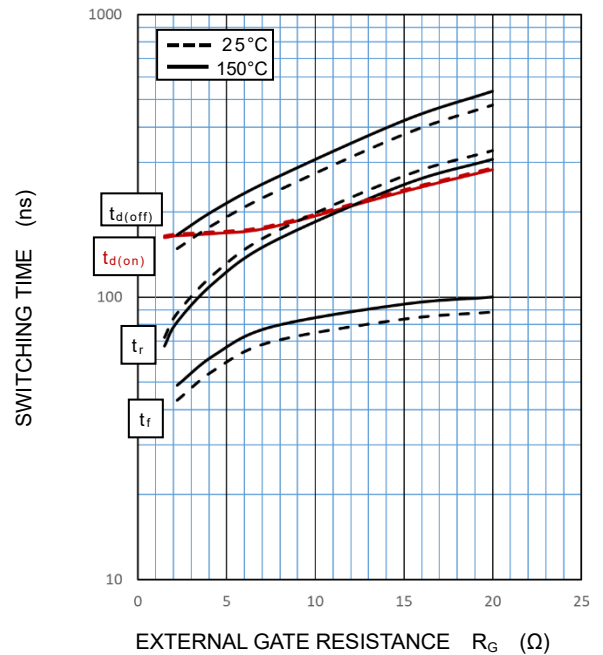
HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)

$V_{DD}=600V, V_{GS}=\pm 15V, R_{G(on)}=1.5\Omega, R_{G(off)}=2.2\Omega, L_{s_ext}=25nH$
INDUCTIVE LOAD



HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)

$V_{DD}=600V, V_{GS}=\pm 15V, I_D=400A, L_{s_ext}=25nH$
INDUCTIVE LOAD



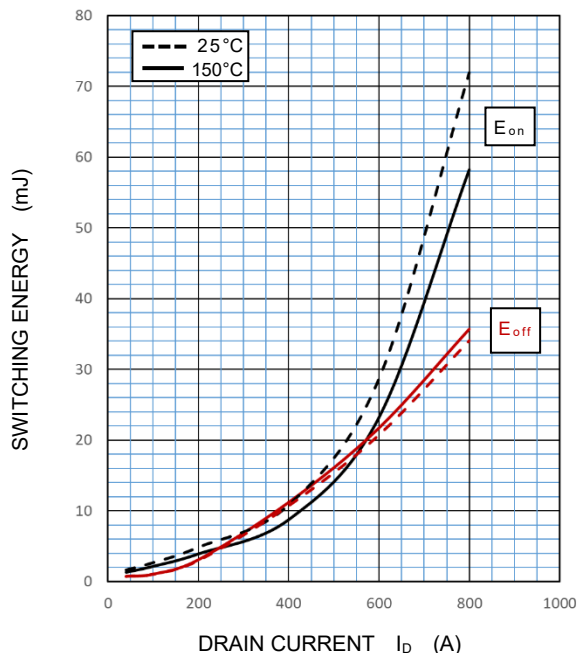
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PERFORMANCE CURVES

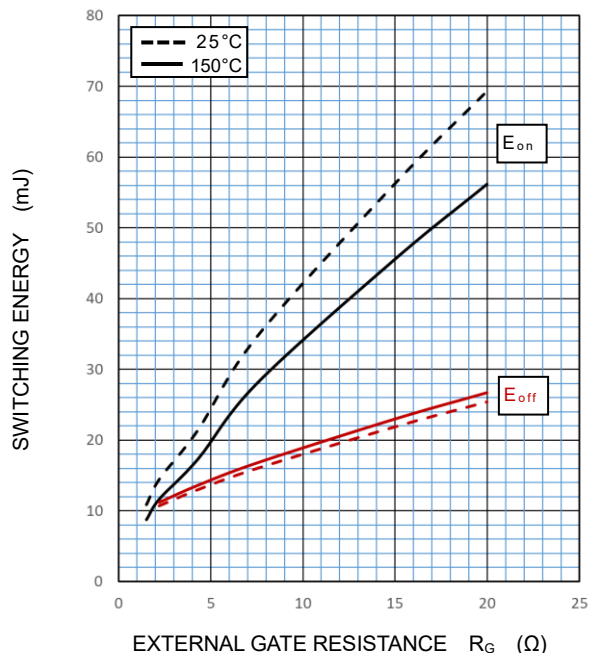
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

$V_{DD}=600\text{ V}$, $V_{GS}=\pm 15\text{ V}$, $R_{G(on)}=1.5\Omega$, $R_{G(off)}=2.2\Omega$, $L_{s_ext}=25\text{ nH}$
INDUCTIVE LOAD, PER PULSE



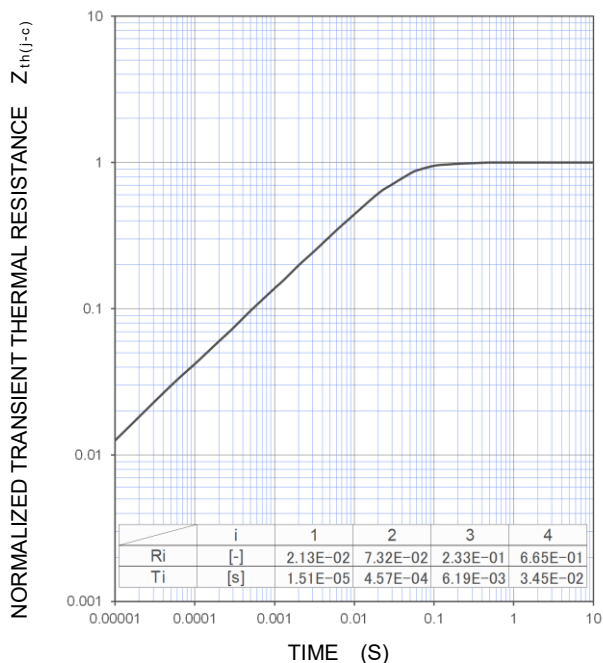
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

$V_{DD}=600\text{ V}$, $V_{GS}=\pm 15\text{ V}$, $I_D=400\text{ A}$, $L_{s_ext}=25\text{ nH}$
INDUCTIVE LOAD, PER PULSE



TRANSIENT THERMAL IMPEDANCE
CHARACTERISTICS
(MAXIMUM)

Single pulse, $T_c=25\text{ °C}$
 $R_{th(j-c)Q}=110\text{ K/kW}$, $R_{th(j-c)D}=150\text{ K/kW}$



Note: The characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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